Linear Circuits Data Book

TEXAS INSTRUMENTS

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INTRODUCTION

The rapid advance in high-tech digital processing creates new demands for microprocessor-compatible circuits that can sense, amplify, and convert analog signals or provide regulated power to a system. In this volume, Texas Instruments presents specifications and technical information on our broad line of integrated circuits designed for applications that involve analogue signal conditioning. That product line includes:

- Operational amplifiers
- Voltage comparators
- Regulators
- Power supply monitors
- Switching-mode power supply circuits
- Current mirrors
- Floppy-disk circuits for control, reading, or writing
- Timers
- A/D converters
- Video amplifiers
- Analog switches
- D/A converters

These circuits span the recent rapid development of integrated circuit technology from classical bipolar through BIFET™ and BIDFET™ to TI's new LinCMOS™ processing that provides a step-function improvement in input impedance, power dissipation, and threshold stability. New surface-mount packages include both plastic and ceramic chip carriers and the small-outline packages that increase board density with little impact on power handling capability.

Ordering information and mechanical data are in the Appendix. Section 1 contains an alphanumeric index that lists page numbers for all the device types included, and each data sheet section provides a functional selection guide to the devices in that section.

While this volume offers design and specification data only for Linear components, complete technical data for any TI semiconductor product is available from your nearest TI sales office.
A listing can be found at the back of this data book.

CONTENTS – continued

CONTENTS

VOLUME 1

CONTENTS – continued

VOLUME 2

CONTENTS – continued

General Information

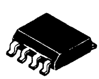
THERMAL RESISTANCE

PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$ (°C/W)	JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$ (°C/W)
D plastic dual-in-line	8	51	172
	14, 16	33	131
FK ceramic chip carrier	20	35	91
FN plastic chip carrier	20	37	114
J ceramic dual-in-line (glass-mounted chips)	14 thru 20	60	122
J ceramic dual-in-line† (alloy-mounted chips)	14 thru 20	29†	91†
JG ceramic dual-in-line (glass-mounted chips)	8	58	151
JG ceramic dual-in-line† (alloy-mounted chips)	8	26†	119†
KC Standard lead frame	3	6	62.5
LP plastic plug-in	3	40	160
N plastic dual-in-line	14 thru 20	72	143
	28	45	100
	40	40	100
P plastic dual-in-line	8	79	172
U ceramic flat	10, 14	55	185
W ceramic flat	14, 16	60	125

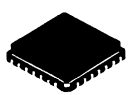
† In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM," or a suffix of "/883B" have alloy-mounted chips.

† This package no longer available.

D PACKAGE



FK PACKAGE



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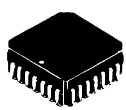
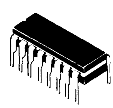
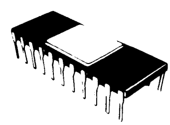


J PACKAGE



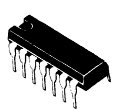
JD PACKAGE



JG PACKAGE

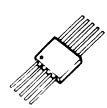
LP PACKAGE

N PACKAGE



P PACKAGE

U PACKAGE

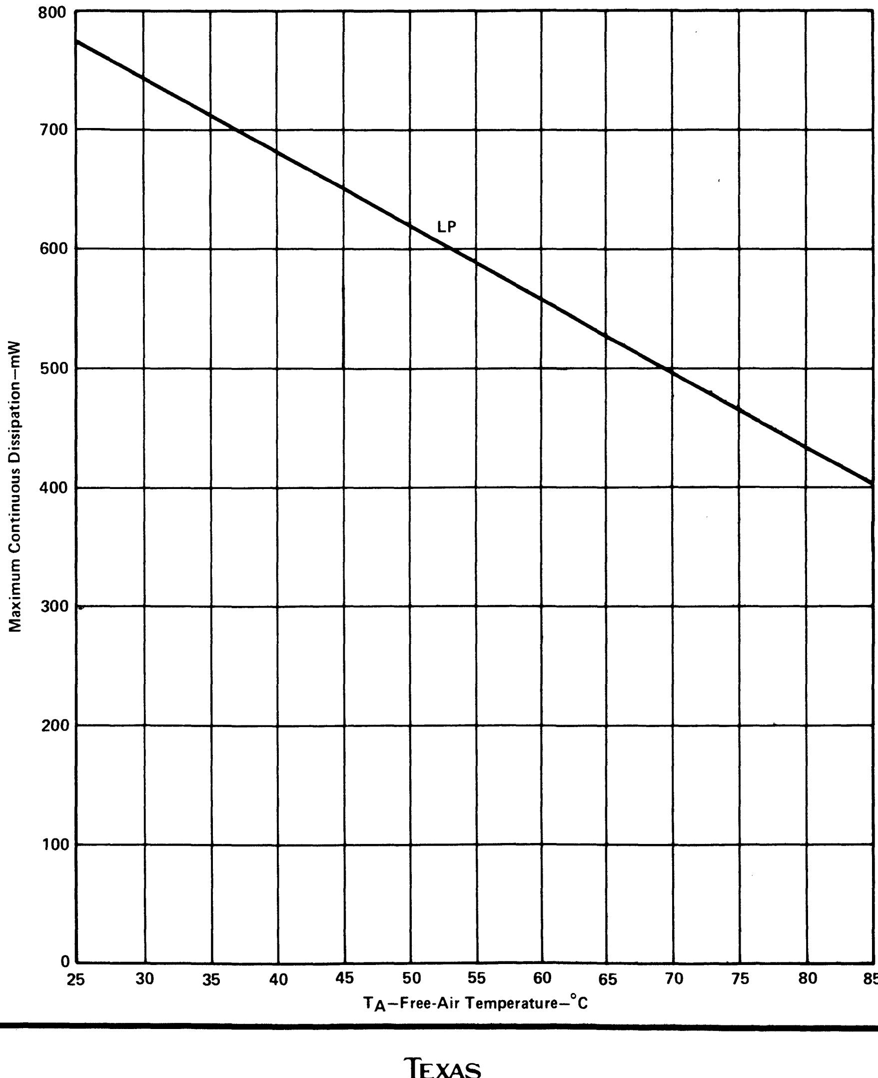


W PACKAGE

PLASTIC PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

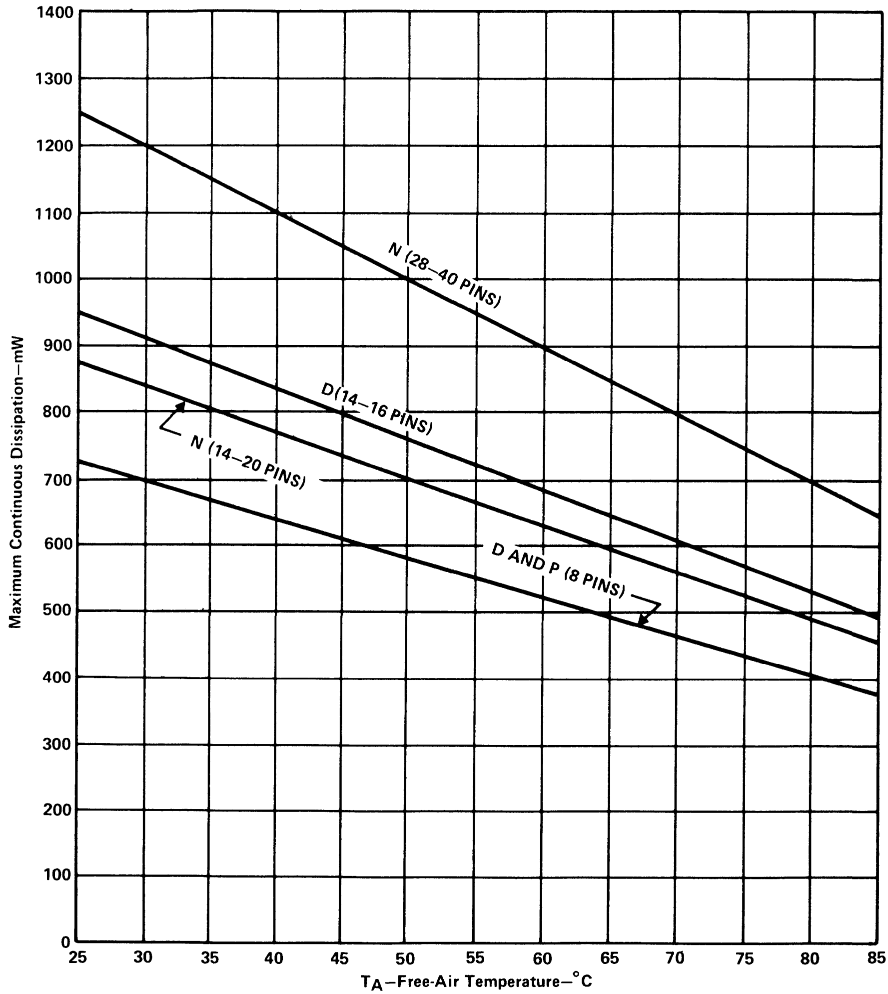
DISSIPATION DERATING CURVE



PLASTIC PACKAGES (CONTINUED)

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

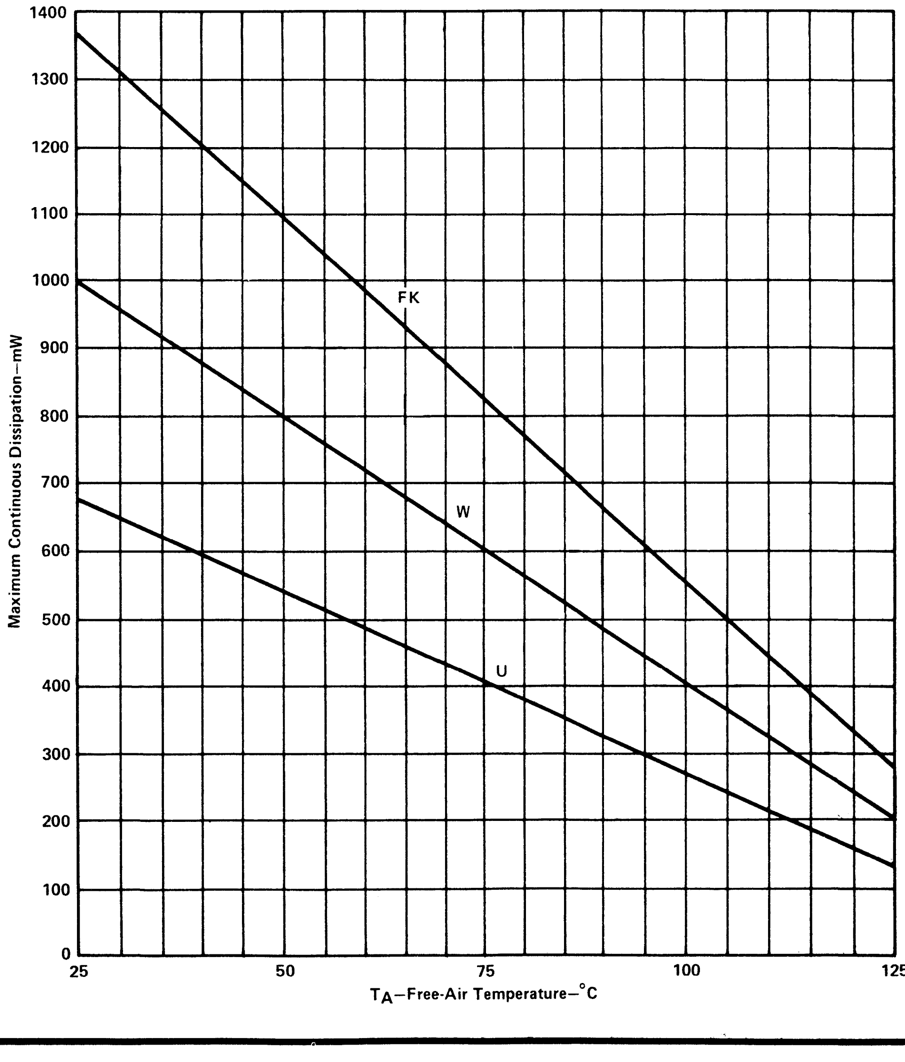
DISSIPATION DERATING CURVE



FLAT PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

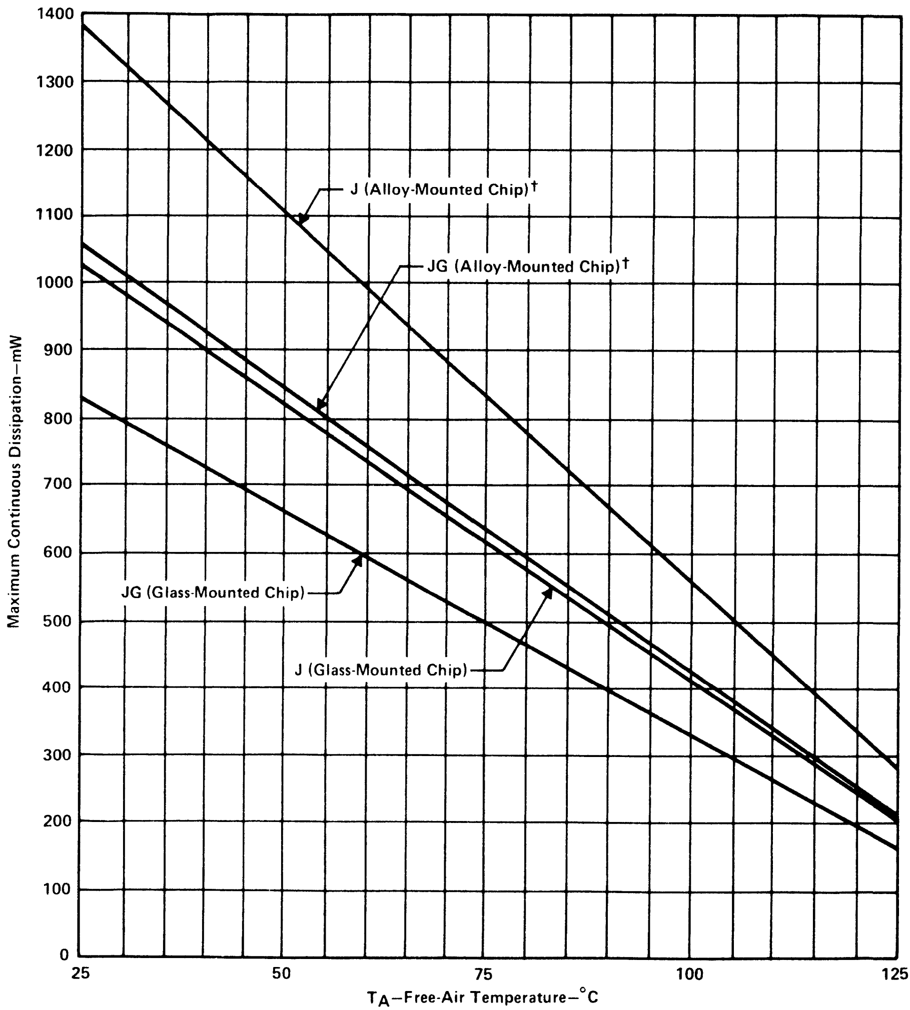
DISSIPATION DERATING CURVE



CERAMIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



† In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883B" have alloy-mounted chips.

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TEXAS INSTRUMENTS

CONTENTS

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to zero or other level, if specified.

Average Temperature Coefficient of Input Offset Voltage (αV_{IO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha V_{IO} = \left[\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient of Input Offset Current (αI_{IO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha I_{IO} = \left[\frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Maximum Peak Output Voltage Swing (V_{OM})

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP})

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Voltage Amplification (A_V)

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output voltage to the change in differential input voltage producing it.

Maximum-Output-Swing Bandwidth (B_{OM})

The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1)

The range of frequencies within which the open-loop voltage amplification is greater than unity.

Phase Margin (ϕ_m)

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

Gain Margin (A_m)

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Input Resistance (r_i)

The resistance between the input terminals with either input grounded.

Differential Input Resistance (r_{id})

The small-signal resistance between the two ungrounded input terminals.

Output Resistance (r_o)

The resistance between the output terminal and ground.

Input Capacitance (C_i)

The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic})

The parallel sum of the small-signal impedance between each input terminal and ground.

Output Impedance (z_o)

The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Sensitivity (k_{SVS}, $\Delta V_{IO}/\Delta V_{CC}$)

The absolute value of the ratio of the change in input offset voltage to the change in supply voltages producing it.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage rejection ratio.

Supply Voltage Rejection Ratio (k_{SVR}, $\Delta V_{CC}/\Delta V_{IO}$)

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

Equivalent Input Noise Voltage (V_n)

The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Equivalent Input Noise Current (I_n)

The current of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

Average Noise Figure ($\overline{F}$)

The ratio of (1) the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature, T_O, at all frequencies to (2) that part of (1) caused by the noise temperature of the designated signal-input termination within a designated signal-input frequency band.

Short-Circuit Output Current (I_{OS})

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.

Supply Current (I_{CC})

The current into the V_{CC} or V_{CC+} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Crosstalk Attenuation (V_{o1}/V_{o2})

The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel.

Rise Time (t_r)

The time required for an output voltage step to change from 10% to 90% of its final value.

Total Response Time (Settling Time) (t_{tot})

The time between a step-function change of the input signal level and the instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm\epsilon$) containing the final output signal level.

Overshoot Factor

The ratio of (1) the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal, to (2) the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

Slew Rate (SR)

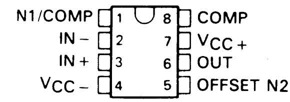
The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

TYPES LM101A, LM201A, LM301A HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

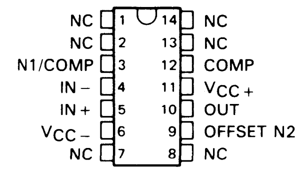
D961, OCTOBER 1979—REVISED AUGUST 1983

- **Low Input Currents**
- **Low Input Offset Parameters**
- **Frequency and Transient Response Characteristics Adjustable**
- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **No Latch-Up**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Same Pin Assignments as uA709**
- **Designed to be Interchangeable with National Semiconductor LM101A and LM301A**

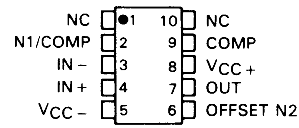
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



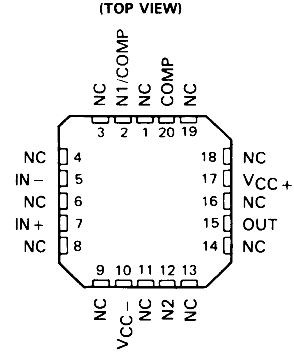
W FLAT PACKAGE
(TOP VIEW)



LM101A
U FLAT PACKAGE
(TOP VIEW)



LM101A
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



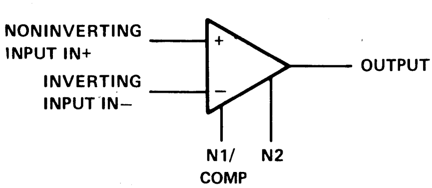
NC—No internal connection

description

The LM101A, LM201A, and LM301A are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices. The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are protected to withstand short-circuits at the output. The external compensation of these amplifiers allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 7, to null out the offset voltage.

The LM101A is characterized for operation over the full military temperature range of −55°C to 125°C, the LM201A is characterized for operation from −25°C to 85°C, and the LM301A is characterized for operation from 0°C to 70°C.

symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM101A	LM201A	LM301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	500	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, JG, U, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM101A only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM201A only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG packages, LM101A chips are alloy-mounted; LM201A and LM301A chips are glass-mounted.

electrical characteristics at specified free-air temperature, C_C = 30 pF (see Note 6)

PARAMETER		TEST CONDITIONS†		LM101A, LM201A			LM301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0 V	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}*	Average temperature coefficient of input offset voltage	V_O = 0 V	Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}*	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 2 kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i*	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No Load, V_O = 0 V, See Note 7	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM101A is −55°C to 125°C, for LM201A is −25°C to 85°C, and for LM301A is 0°C to 70°C.

NOTES: 6. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for LM101A and LM201A, and $V_{CC\pm}$ = ±5 V to ±15 V for LM301A. All typical values are at $V_{CC\pm}$ = ±15 V.

7. For LM101A and LM201A, $V_{CC\pm}$ = ±20 V. For LM301A, $V_{CC\pm}$ = ±15 V.

*For LM101A these parameters are guaranteed but not tested.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

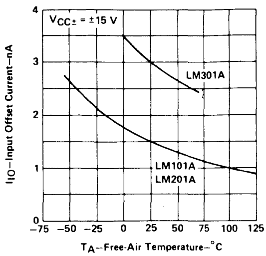


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

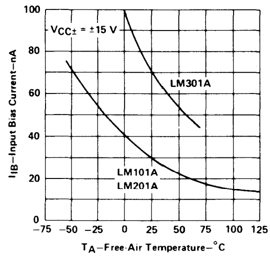


FIGURE 2

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (WITH
SINGLE-POLE COMPENSATION)
vs FREQUENCY

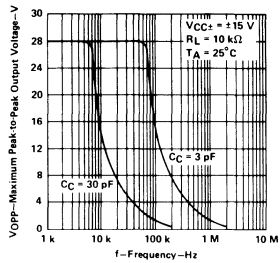


FIGURE 3

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

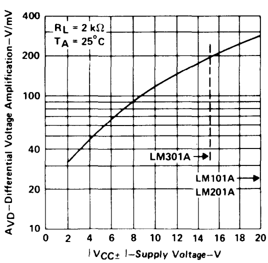


FIGURE 4

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

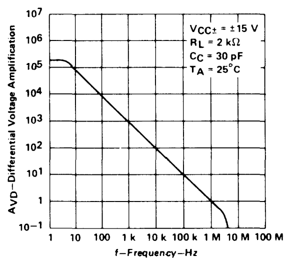


FIGURE 5

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

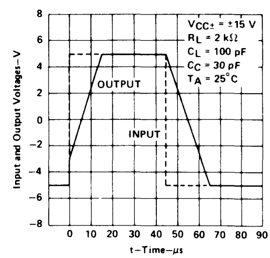
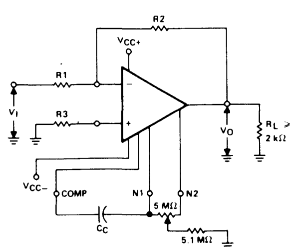


FIGURE 6

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ pF}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 7– INVERTING CIRCUIT WITH ADJUSTABLE GAIN, SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

3 Operational Amplifiers

883

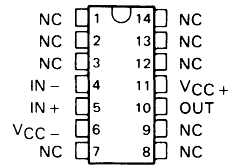
TEXAS INSTRUMENTS

TYPES LM107, LM207, LM307
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

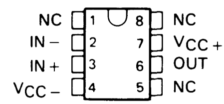
D962, DECEMBER 1970—REVISED AUGUST 1983

- **Low Input Currents**
- **No Frequency Compensation Required**
- **Low Input Offset Parameters**
- **Short-Circuit Protection**
- **No Latch-Up**
- **Wide Common-Mode and Differential Voltage Ranges**

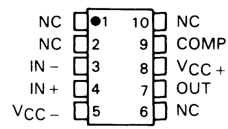
LM107 . . . J OR W PACKAGE
LM207, LM307 . . . W PACKAGE
(TOP VIEW)



LM107 . . . JG PACKAGE
LM207, LM307 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LM107 . . . U FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

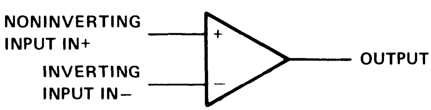
description

The LM107, LM207, and LM307 are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The LM107 is characterized for operation over the full military temperature range of −55 °C to 125 °C, the LM207 is characterized for operation from −25 °C to 85 °C, and the LM307 is characterized for operation from 0 °C to 70 °C.

symbol



	LM107	LM207	LM307	UNIT
Supply voltage V_{CC+} (see Note 1)	22	22	18	V
Supply voltage V_{CC-} (see Note 1)	−22	−22	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short-circuit (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	500	500	500	mW
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds JG, U, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM207 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature (see Note 6)

PARAMETER		TEST CONDITIONS†		LM107, LM207 MIN	LM107, LM207 TYP	LM107, LM207 MAX	LM307 MIN	LM307 TYP	LM307 MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}*	Average temperature coefficient of input offset voltage	$V_O = 0$	Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}*	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L = 10$ kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm} = \pm 15$ V, $R_L = 2$ kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i*	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No Load, $V_O = 0$, See Note 7	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM107 is −55°C to 125°C, for LM207 is −25°C to 85°C, and for LM307 is 0°C to 70°C.

NOTES: 6. Unless otherwise noted $V_{CC\pm} = \pm 5$ V to ± 20 V for LM107 and LM207, and $V_{CC\pm} = \pm 5$ V to ± 15 V for LM307. All typical values are at $V_{CC\pm} = \pm 15$ V.

7. For LM107 and LM207, $V_{CC\pm} = \pm 20$ V. For LM307, $V_{CC\pm} = \pm 15$ V.

*For LM107 these parameters are guaranteed but not tested.

MAY 1988

FEATURES

- 200pA max. input offset current
- 2nA max. input bias current
- 600μA max. supply current
- 0.5mV max. offset voltage
- 5μV/°C max. drift
- Wide supply voltage range: ± 2V to ± 18V

APPLICATIONS

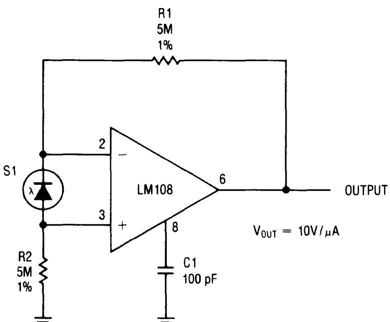
- Integrators
- Transducer amplifiers
- Analog memories
- Light meters

DESCRIPTION

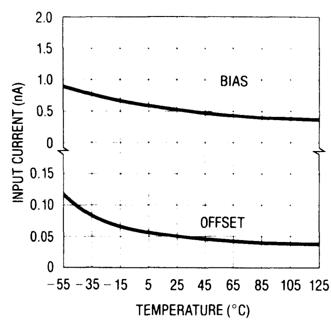
The LM108 series of precision operational amplifiers are particularly well-suited for high source impedance applications requiring low offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the offset and bias currents of the LM108 do not change significantly with temperature variations. Advanced design, processing and testing techniques make Linear's LM108 a superior choice over previous devices.

A photodiode sensor application is shown below. For applications requiring higher performance, see the LT1008, and LT1012.

Amplifier For Photodiode Sensor



Input Currents



TEXAS INSTRUMENTS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LM108A/LM108 .... ±20V
- LM308A/LM308 .... ±18V

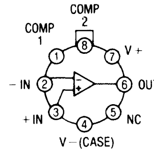
Differential Input Current (Note 1)......... ±10mA
Input Voltage (Note 2).................. ±15V
Output Short Circuit Duration........... Indefinite
Operating Temperature Range
- LM108A/LM108 .... −55°C to 125°C
- LM308A/LM308 .... 0°C to 70°C

Storage Temperature Range
- All Devices................. −65°C to 150°C

Lead Temperature (Soldering, 10 sec.)...... 300°C

PACKAGE/ORDER INFORMATION

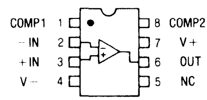
TOP VIEW



METAL CAN L PACKAGE

ORDER PART NO.
LM108AL
LM108L
LM308AL
LM308L

TOP VIEW



PLASTIC DIP P PACKAGE

ORDER PART NO.
LM308AP
LM308P

ELECTRICAL CHARACTERISTICS ±5V ≤ V_s ≤ ±20V and −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LM108A MIN	LM108A TYP	LM108A MAX	LM108 MIN	LM108 TYP	LM108 MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			0.3	0.5		0.7	2.0	mV
			●			1.0			3.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		●		1.0	5.0		3.0	15	µV/°C
I_{OS}	Input Offset Current	T_A = 25°C			0.05	0.2		0.05	0.2	nA
			●			0.4			0.4	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		●		0.5	2.5		0.5	2.5	pA/°C
I_B	Input Bias Current	T_A = 25°C			0.5	2.0		0.5	2.0	nA
			●			3.0			3.0	nA
A_{VOL}	Large Signal Voltage Gain	T_A = 25°C, V_S ± 15V,		80	300		50	300		V/mV
		V_{OUT} = ± 10V, R_L ≥ 10kΩ	●	40			25			V/mV
CMRR	Common Mode Rejection Ratio		●	96	110		85	100		dB
PSRR	Power Supply Rejection Ratio		●	96	110		80	96		dB
	Input Voltage Range	V_S = ± 15V	●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	V_S = ± 15V, R_L = 10kΩ	●	±13	±14		±13	±14		V
R_{IN}	Input Resistance	T_A = 25°C (Note 3)		30	70		30	70		MΩ
I_S	Supply Current	T_A = 25°C			0.3	0.6		0.3	0.6	mA
		T_A = 125°C			0.15	0.4		0.15	0.4	mA

TEXAS INSTRUMENTS

ELECTRICAL CHARACTERISTICS ±5V ≤ V_s ±15V and 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LM308A MIN	LM308A TYP	LM308A MAX	LM308 MIN	LM308 TYP	LM308 MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C	 ●		0.3	0.5 0.73		2.0	7.5 10	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		●		2.0	5.0		6.0	30	μV/°C
I_{OS}	Input Offset Current	T_A = 25°C	 ●		0.2	1.0 1.5		0.2	1.0 1.5	nA nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		●		2.0	10		2.0	10	pA/°C
I_B	Input Bias Current	T_A = 25°C	 ●		1.5	7.0 10		1.5	7.0 10	nA nA
A_{VOL}	Large Signal Voltage Gain	T_A = 25°C, V_S ± 15V, V_{OUT} = ± 10V, R_L ≥ 10kΩ	 ●	80 60	300		25 15	300		V/mV V/mV
CMRR	Common Mode Rejection Ratio		●	96	110		80	100		dB
PSRR	Power Supply Rejection Ratio		●	96	110		80	96		dB
	Input Voltage Range	V_S = ± 15V	●	± 14			± 14			V
V_{OUT}	Output Voltage Swing	V_S = ± 15V R_L = 10kΩ	●	± 13	± 14		± 13	± 14		V
R_{IN}	Input Resistance	T_A = 25°C (Note 3)		10	40		10	40		MΩ
I_S	Supply Current	T_A = 25°C			0.3	0.8		0.3	0.8	mA

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883 data sheet for test listing and parameters.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistance is used.

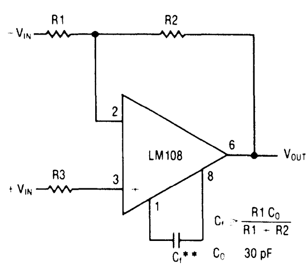
Note 2: For supply voltages less than ± 15V, the maximum input voltage is equal to the supply voltage.

Note 3: Characterized by design.

TYPICAL APPLICATIONS

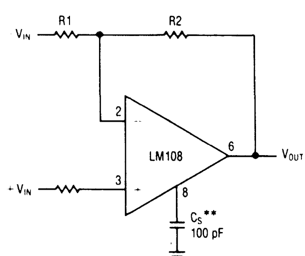
COMPENSATION CIRCUITS

Standard Compensation Circuit



** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO 1/C_f

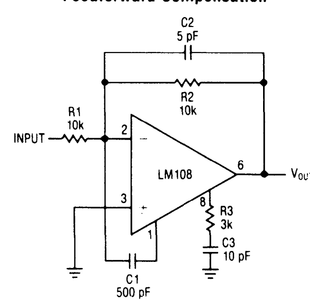
Alternate* Frequency Compensation



* IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN.

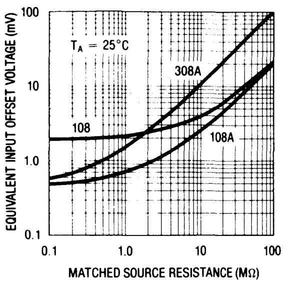
** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO 1/C_S

Feedforward Compensation

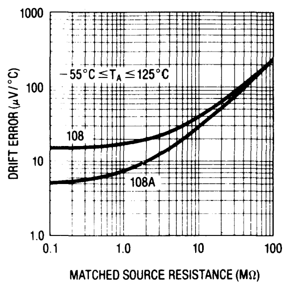


TYPICAL PERFORMANCE CHARACTERISTICS

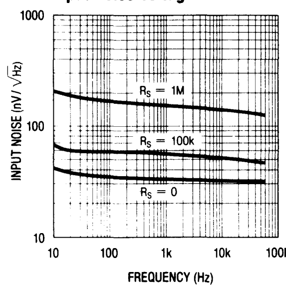
Offset Error



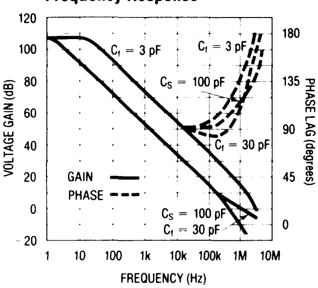
Drift Error



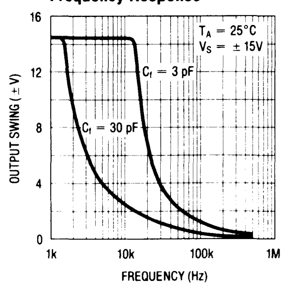
Input Noise Voltage



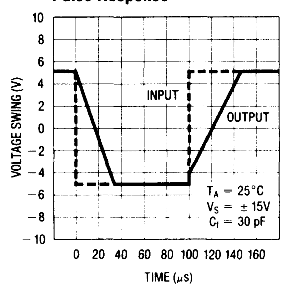
Open Loop Frequency Response



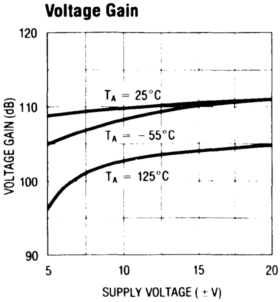
Large Signal Frequency Response



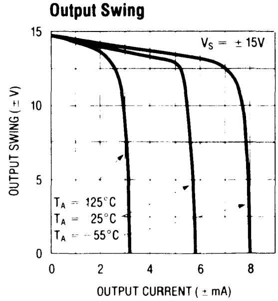
Voltage Follower Pulse Response



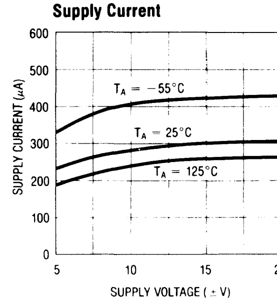
Voltage Gain



Output Swing



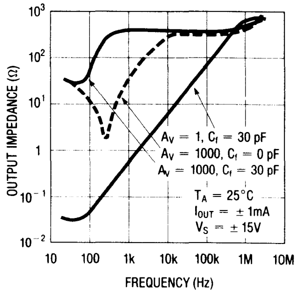
Supply Current



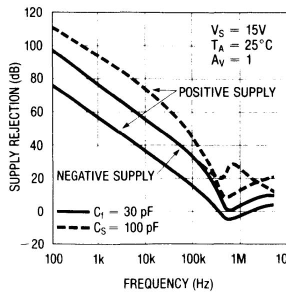
TEXAS INSTRUMENTS

TYPICAL PERFORMANCE CHARACTERISTICS

Closed Loop Output Impedance

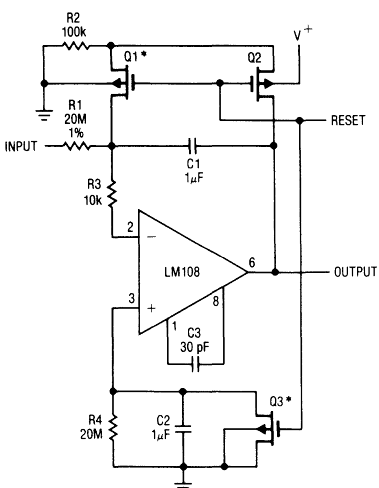


Power Supply Rejection



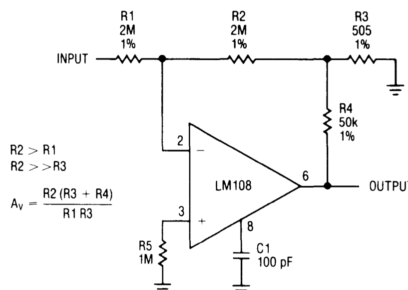
TYPICAL APPLICATIONS

Low Drift Integrator With Reset



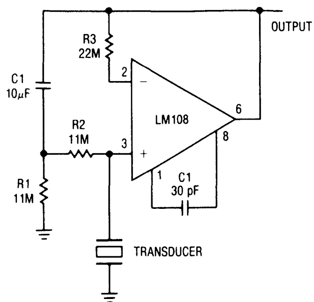
* Q1 AND Q3 SHOULD NOT HAVE INTERNAL GATE-PROTECTION DIODES.

Inverting Amplifier With High Input Resistance

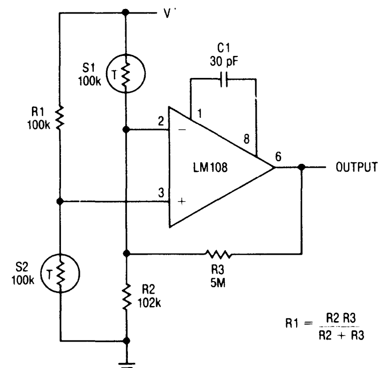


TYPICAL APPLICATIONS

Amplifier For Piezoelectric Transducers

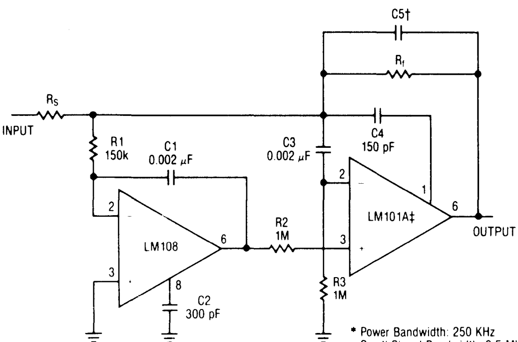


Amplifier For Bridge Transducers



$R1 = \frac{R2\,R3}{R2 + R3}$

Fast* Summing Amplifier

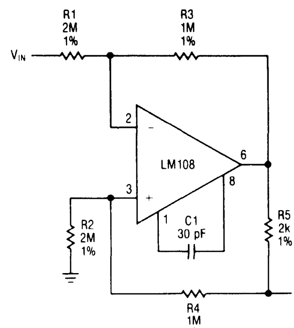


‡ In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

* Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μS

†C5 $\frac{6 \times 10^{-8}}{R_f}$

Bilateral Current Source

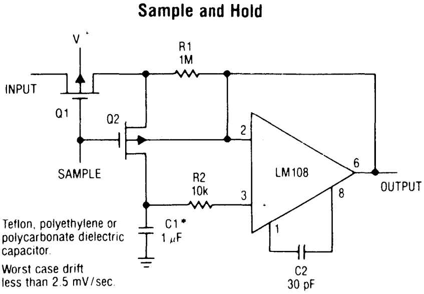


$I_{OUT} = \frac{R3\,V_{IN}}{R1\,R5}$

$R3 = R4 + R5$

$R1 = R2$

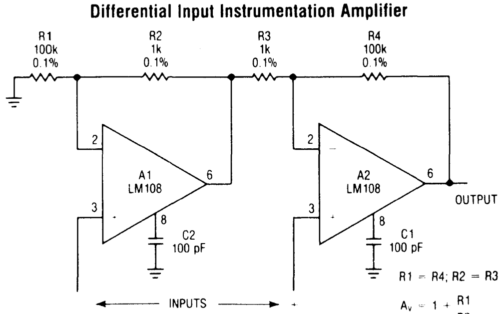
Sample and Hold



* Teflon, polyethylene or polycarbonate dielectric capacitor.

Worst case drift less than 2.5 mV/sec.

Differential Input Instrumentation Amplifier



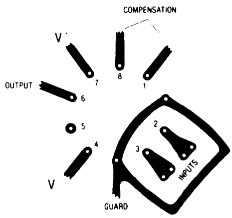
$R1 = R4;\ R2 = R3$

$A_V = 1 + \frac{R1}{R2}$

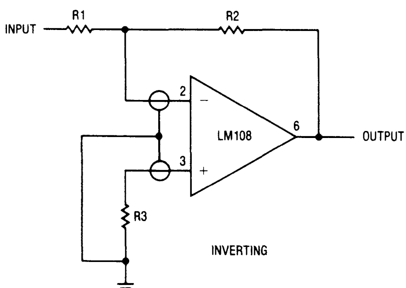
APPLICATIONS INFORMATION

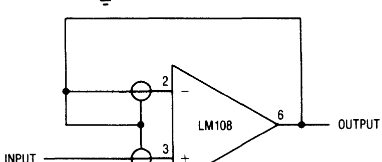
Input guarding

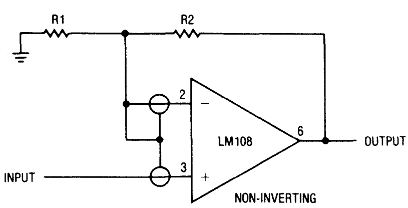
Input guarding is used to reduce surface leakage. Guarding both sides of the board is required. Bulk leakage reduction is less and depends on the guard ring width.



The guard ring is connected to a low impedance point at same potential as the sensitive input leads. Connections for various op amp configurations are shown below.

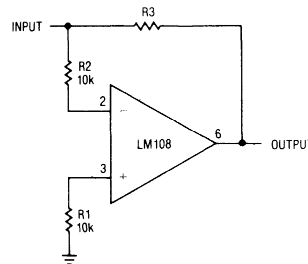




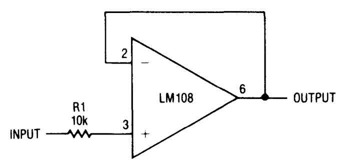


Input protection

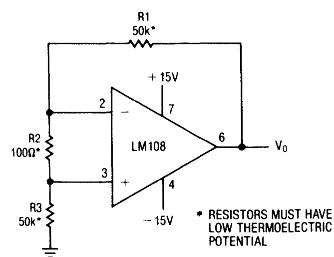
Current is limited by R2 even when input is connected to a voltage source outside the common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.



The input resistor controls the current when the input exceeds the supply voltages, when the power for the op amp is turned off, or when the output is shorted.



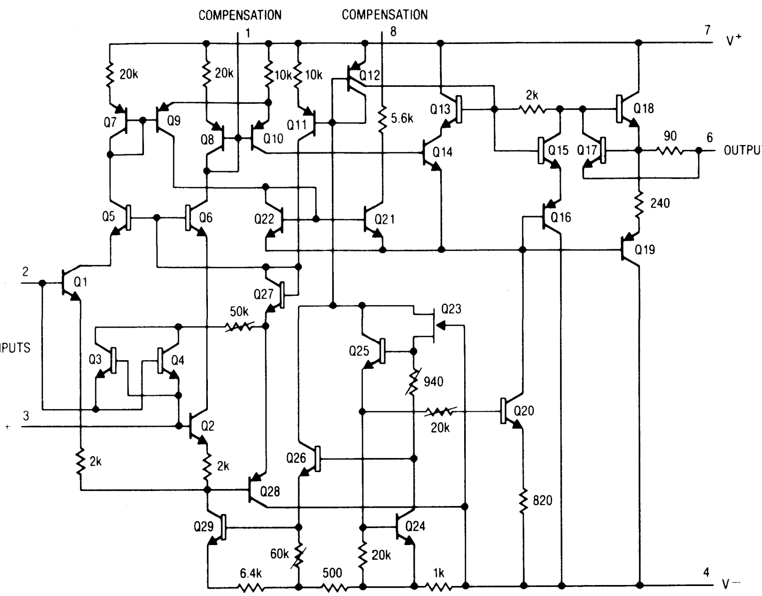
Offset Voltage Test Circuit†



$A_V = 1000$

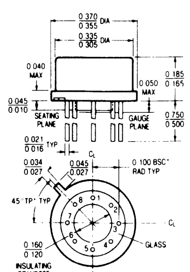
† THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION WITH SUPPLY VOLTAGES EQUAL TO ±20V, R1 = R3 = 10k, R2 = 200Ω, $A_V = 100$.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

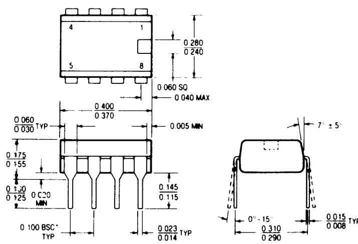
L Package
Metal Can



NOTE DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

P Package
8 Lead Plastic



NOTE DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
100°C	130°C/W

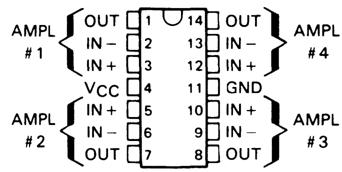
TEXAS INSTRUMENTS

TYPES LM124, LM224, LM224A, LM324, LM324A, LM2902 QUADRUPLE OPERATIONAL AMPLIFIERS

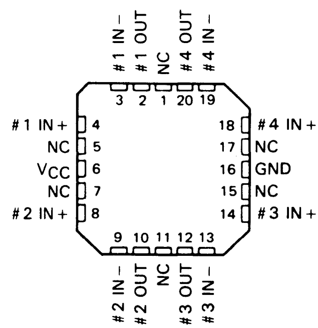
D1990, SEPTEMBER 1975—REVISED SEPTEMBER 1983

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2902 . . . 3 V to 26 V),
  or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 32 V (26 V for LM2902)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

D, J, OR N DUAL-IN-LINE PACKAGE, OR W FLAT PACKAGE (TOP VIEW)



LM124 FK CHIP CARRIER PACKAGE (TOP VIEW)



NC—No internal connection

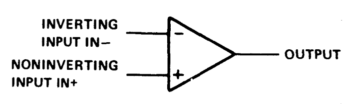
description

These devices consist of four independent, high-gain frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 30 volts (for the LM2902, 3 volts to 26 volts), and Pin 4 is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

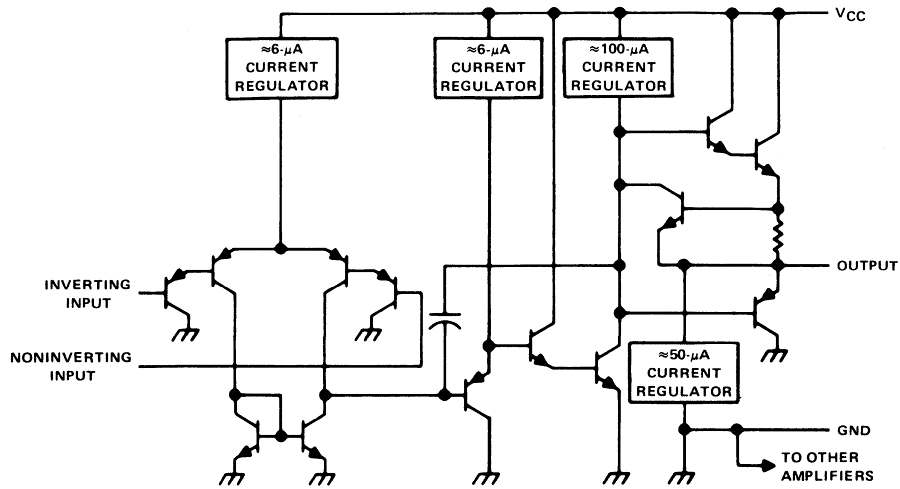
Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-volt supplies.

The LM124 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM2902 is characterized for operation from −40°C to 85°C, the LM224 and LM224A from −25°C to 85°C, and the LM324 and LM324A from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM124 LM224, LM224A, LM324, LM324A	LM2902	UNIT
Supply voltage, V_{CC} (see Note 1)		32	26	V
Differential voltage (see Note 2)		±32	±26	V
Input voltage range (either input)		−0.3 to 32	−0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature (V_{CC} ≤ 15 V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	D or J package	900	900	mW
	N package	875	875	
Operating free-air temperature range	LM124	−55 to 125		°C
	LM224, LM224A	−25 to 85		
	LM324, LM324A	0 to 70		
	LM2902		−40 to 85	
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to dissipation Derating Curves, Section 2. In the J package, LM124 chips are alloy-mounted; LM224, LM324, and LM2902 chips are glass-mounted.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM124, LM224			LM324			LM2902			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$						V
		R_L = 10 kΩ	25°C							$V_{CC}-1.5$			
		V_{CC} = MAX, R_L = 2 kΩ	Full range	26			26			22			
		V_{CC} = MAX, R_L = 10 kΩ	Full range	27	28		27	28		23	24		
V_{OL}*	Low-level output voltage	$R_l \le 10$ kΩ	Full range		5	20		5	20		5	100	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \ge 2$ kΩ	25°C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		50	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_o	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1.1	3		1.1	3		1.1	3	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2902, 30 V for the others. Full range is −55°C to 125°C for LM124, −25°C to 85°C for LM224, 0°C to 70°C for LM324, and −40°C to 85°C for LM2902.

*For LM124 this parameter is guaranteed but not tested.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM224A			LM324A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		2	3		2	3	mV
			Full range			4			5	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	15		2	30	nA
			Full range			30			75	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	−80		−15	−100	V
			Full range			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C		$V_{CC}-1.5$			$V_{CC}-1.5$		V
		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			
		V_{CC} = 30 V, R_L = 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	$R_l \le 10$ kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \ge 2$ kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
			25°C	5			5			
		V_{ID} = −1 V, V_O = 200 mV	Full range	12	30		12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	Full range		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1.1	3		1.1	3	

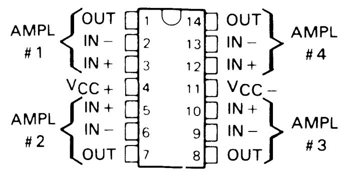
†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −25°C to 85°C for LM224A and 0°C to 70°C for LM324A.

TYPES LM148, LM248, LM348
QUADRUPLE OPERATIONAL AMPLIFIERS

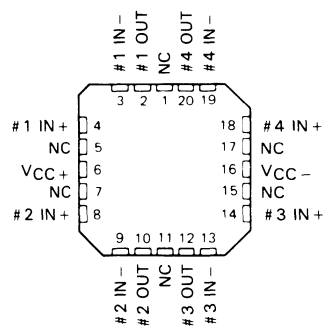
D2551, OCTOBER 1979—REVISED SEPTEMBER 1983

- uA741 Operating Characteristics
- Low Supply Current Drain . . . 0.6 mA Typ (per amplifier)
- Low Input Offset Voltage
- Low Input Offset Current
- Class AB Output Stage
- Input/Output Overload Protection
- Designed to be Interchangeable with National LM148, LM248, and LM348.

LM148 . . . J PACKAGE
LM248, LM348 . . . D, J, OR N PACKAGE
(TOP VIEW)



LM148 . . . FK PACKAGE
(TOP VIEW)



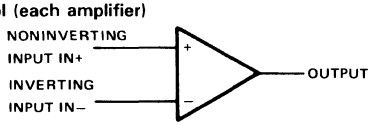
NC—No internal connection

description

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the uA741. These amplifiers exhibit low supply current drain, and input bias and offset currents that are much less than those of the uA741.

The LM148 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM248 is characterized for operation from −25°C to 85°C, and the LM348 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM148	LM248	LM348	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage (see Note 2)		44	36	36	V
Input voltage (either input, see Notes 1 and 3)		±22	±18	±18	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)	D, FK, or J package	900	900	900	mW
	N package		875	875	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, or J package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, LM148 chips are alloy mounted, LM248 and LM348 chips are glass mounted.

electrical characteristics, $V_{CC\pm} = \pm 15$ V

	PARAMETER	TEST CONDITIONS†		LM148 MIN	LM148 TYP	LM148 MAX	LM248 MIN	LM248 TYP	LM248 MAX	LM348 MIN	LM348 TYP	LM348 MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	25 °C		1	5		1	6		1	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	$V_O = 0$	25 °C		4	25		4	50		4	50	nA
			Full range			75			125			100	
I_{IB}	Input bias current	$V_O = 0$	25 °C		30	100		30	200		30	200	nA
			Full range			325			500			400	
V_{ICR}	Common-mode input voltage range		Full range	±12			±12			±12			V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25 °C	±12	±13		±12	±13		±12	±13		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			±12			
		$R_L = 2\ k\Omega$	25 °C	±10	±12		±10	±12		±10	±12		
		$R_L \geq 2\ k\Omega$	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25 °C	50	160		25	160		25	160		V/mV
			Full range	25			15			15			
r_i	Input resistance		25 °C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
B_1	Unity-gain bandwidth	$A_{VD} = 1$	25 °C		1			1			1		MHz
ϕ_M	Phase margin	$A_{VD} = 1$	25 °C		60°			60°			60°		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$	25 °C	70	90		70	90		70	90		dB
			Full range	70			70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25 °C	77	96		77	96		77	96		dB
			Full range	77			77			77			
I_{OS}	Short-circuit output current		25 °C		±25			±25			±25		mA
I_{CC}	Supply current (four amplifiers)	No load: $V_O = 0$ / $V_O = V_{OM+}$	25 °C		2.4	3.6		2.4	4.5		2.4	4.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 Hz to 20 kHz,	25 °C		120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55 °C to 125 °C for LM148, −25 °C to 85 °C for LM248, and 0 °C to 70 °C for LM348.

*For LM148 this parameter is guaranteed but not tested.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

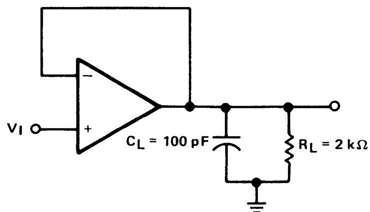


FIGURE 1—UNITY-GAIN AMPLIFIER

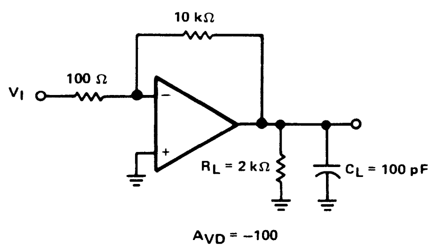


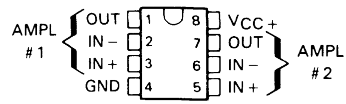
FIGURE 2—INVERTING AMPLIFIER

TYPES LM158, LM258, LM358 LM258A, LM358A, LM2904 DUAL OPERATIONAL AMPLIFIERS

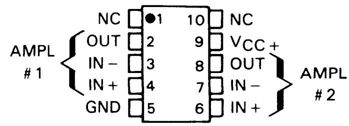
D2231, JUNE 1976 REVISED AUGUST 1983

- Wide Range of Supply Voltages:
  Single Supply . . . 3 V to 30 V
  (LM2904 . . . 3 V to 26 V),
  or Dual Supplies
- Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ
- Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground
- Low Input Bias and Offset Parameters:
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V (±26 V for LM2904)
- Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ
- Internal Frequency Compensation

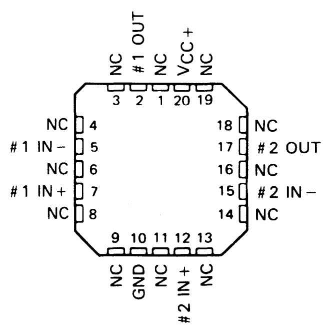
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



U FLAT PACKAGE
(TOP VIEW)



LM 158
FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

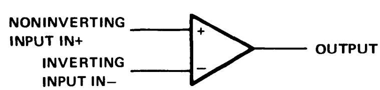
description

These devices consist of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 30 volts (3 volts to 26 volts for the LM2904), and the V_{CC} pin is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

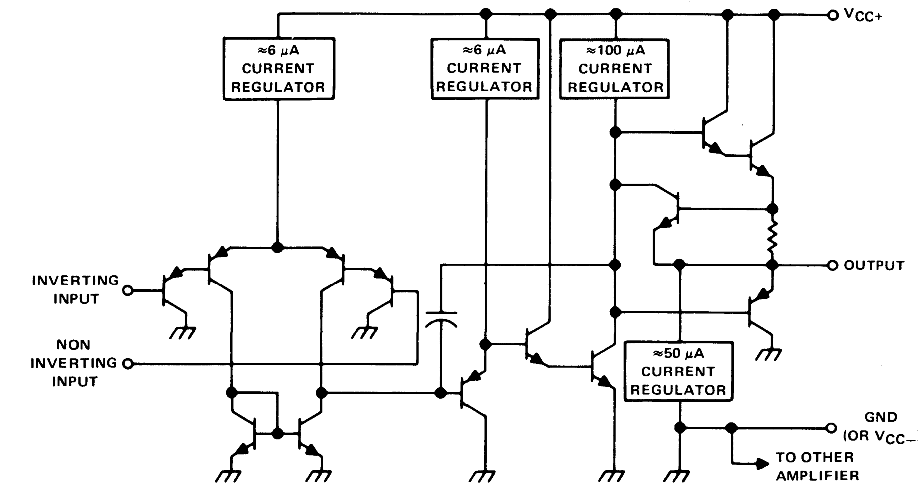
Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, these devices can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-volt supplies.

The LM158 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM258 and LM258A are characterized for operation from −25°C to 85°C, the LM358 and LM358A from 0° to 70°, and the LM2904 from −40°C to 85°C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM158, LM258, LM258A LM358, LM358A	LM2904	UNIT
Supply voltage, V_{CC} (see Note 1)		32	26	V
Differential voltage (see Note 2)		±32	±26	V
Input voltage range (either input)		−0.3 to 32	−0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature (V_{CC} ≤ 15 V) (see Note 3)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	D package	725	725	mW
	JG package (alloy-mounted chip)	1050		
	JG package (glass-mounted chip)	825	825	
	P package	725	725	
	U package	675	675	
Operating free-air temperature range	LM158	−55 to 125		°C
	LM258, LM258A	−25 to 85		
	LM358, LM358A	0 to 70		
	LM2904		−40 to 85	
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, JG, or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	°C

NOTES: 1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG package, LM158 chips are alloy-mounted; LM258, LM258A, LM358, LM358A, and LM2904 chips are glass-mounted.

electrical characteritics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM158, LM258			LM358			LM2904			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7			7			7		μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10			10			10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$			V
			Full range	0 to $V_{CC} - 2$			0 to $V_{CC} - 2$			0 to $V_{CC} - 2$			
V_{OH}	High-level output voltage	$R_L \geq 2\ k\Omega$	25°C	$V_{CC} - 1.5$			$V_{CC} - 1.5$						V
		$R_L \geq 10\ k\Omega$	25°C							$V_{CC} - 1.5$			
		V_{CC} = MAX, $R_L = 2\ k\Omega$,	Full range	26			26			22			
		V_{CC} = MAX, $R_L \geq 10\ k\Omega$	Full range	27	28		27	28		23	24		
V_{OL}*	Low-level output voltage	$R_L \leq 10\ k\Omega$	Full range		5	20		5	20		5	100	mV

*For LM158 this parameter is guaranteed but not tested.

A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25°C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to MAX	25°C	65	100		65	100		50	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30		−20	−30		−20	−30		mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 5 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1	2		1	2		1	2	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2904, 30 V for the others. Full range is 55°C to 125°C for LM158, 25°C to 85°C for LM258, 0°C to 70°C for LM358, and −40°C to 85°C for LM2904.

TEXAS INSTRUMENTS

electrical chararacteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM258A MIN	LM258A TYP	LM258A MAX	LM358A MIN	LM358A TYP	LM358A MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		2	3		2	3	mV
			Full range			4			5	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7	15		7	20	μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	15		2	30	nA
			Full range			30			75	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10	200		10	300	pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	−80		−15	−100	nA
			Full range			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} 30 V	25°C	0 to V_{CC} −1.5			0 to V_{CC} −1.5			V
			Full range	0 to V_{CC} −2			0 to V_{CC} −2			
V_{OH}	High-level output voltage	$R_L \geq 2\ k\Omega$	25°C	V_{CC} −1.5			V_{CC} −1.5			V
		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			
		V_{CC} = 30 V, $R_L \geq 10\ k\Omega$	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	$R_L \leq 10\ k\Omega$	Full range		5	20		5	20	mV

Operational Amplifiers 3

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A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25 °C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio		25 °C	70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25 °C	65	100		65	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25 °C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25 °C	20	30	60	20	30	60	mA
			Full range	10			10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25 °C	10	20		10	20		
			Full range	5			5			
		V_{ID} = −1 V, V_O = 200 mV	25 °C	12	30		12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25 °C		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1	2			2	

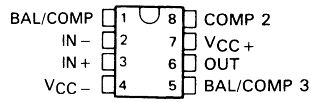
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −25 °C to 85 °C for LM258A and 0 °C to 70 °C for LM358A.

TYPES LM218, LM318 HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

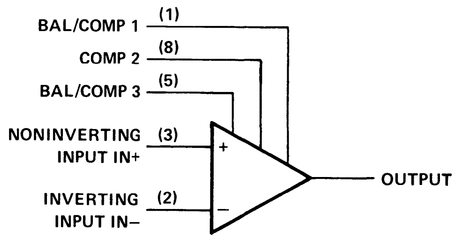
D2219, JUNE 1976—REVISED AUGUST 1983

- **Small-Signal Bandwidth . . . 15 MHz Typ**
- **Slew Rate . . . 50 V/μs Min**
- **Bias Current . . . 250 nA Max (LM218)**
- **Supply Voltage Range . . . ±5 V to ±20 V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protection**
- **Same Pin Assignments as General-Purpose Operational Amplifiers**

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



symbol



description

The LM218 and LM318 are precision, high-speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general purpose devices without sacrificing dc performance.

These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 150 V/μs and almost double the bandwidth. Overcompensation may be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor may be added to reduce the settling time for 0.1% error band to under 1 μs.

The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample and hold circuits, and general purpose amplifiers.

The LM218 is characterized for operation from −25°C to 85°C, and the LM318 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM218	LM318	UNIT
Supply voltage, V_{CC+} (see Note 1)		20	20	V
Supply voltage, V_{CC-} (see Note 1)		−20	−20	V
Input voltage (either input, see Notes 1 and 2)		±15	±15	V
Differential input current (see Note 3)		±10	±10	mA
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. For the LM218 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG package, LM218 and LM318 chips are glass-mounted.

electrical characteristics at specified free-air temperature (see Note 6)

PARAMETER		TEST CONDITIONS†		LM218			LM318			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		2	4		4	10	mV
			Full range			6			15	
I_{IO}	Input offset current	$V_O = 0$	25°C		6	50		30	200	nA
			Full range			100			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		120	250		150	250	nA
			Full range			500			750	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm} = \pm 15$ V	Full range	±11.5			±11.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L = 2$ kΩ	Full range	±12	±13		±12	±13		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			20			
B_1	Unity-gain bandwidth	$V_{CC\pm} = \pm 15$ V	25°C		15			15		MHz
r_i	Input resistance		25°C	1	3		0.5	3		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	Full range	80	100		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		Full range	70	80		65	80		dB
I_{CC}	Supply current	No load, $V_O = 0$	25°C		5	8		5	10	mA
			Full range		4.5	7				

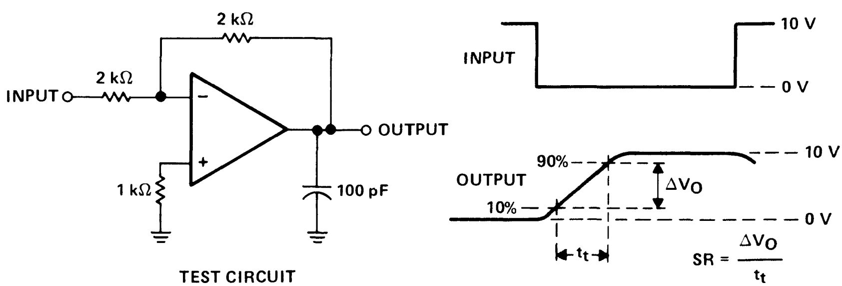
† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM218 is −25°C to 85°C and for LM318 is 0°C to 70°C.

NOTE 6: Unless otherwise noted, $V_{CC} = \pm 5$ V to ± 20 V. All typical values are at $V_{CC\pm} = \pm 15$ V.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$\Delta V_I = 10$ V,	$C_L = 10$ pF,	See Figure 1	50	70		V/μs

parameter measurement information

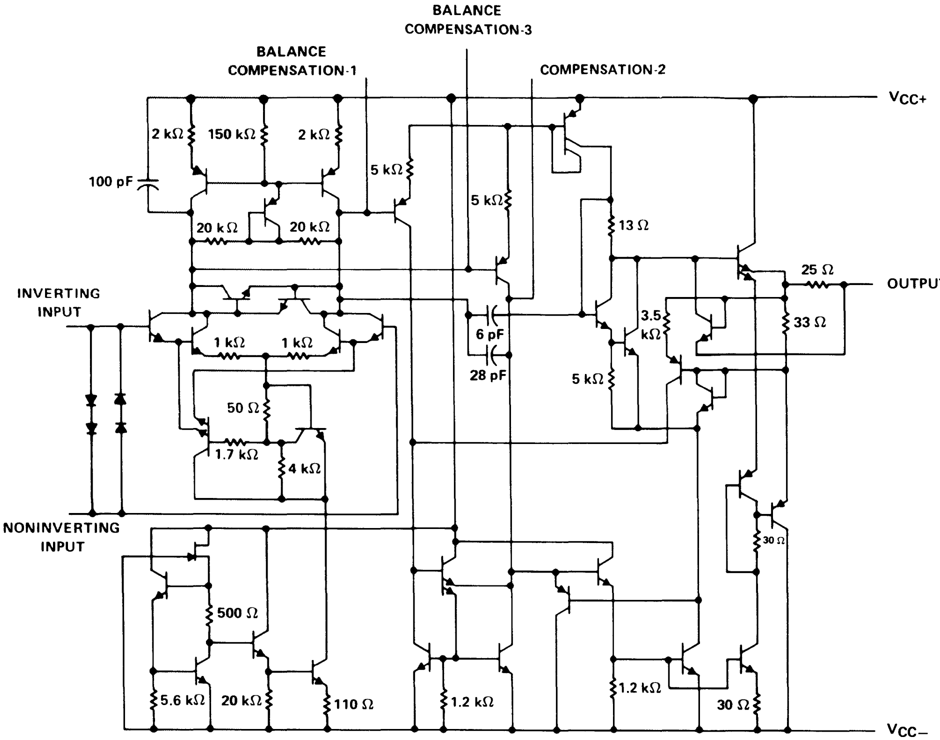


TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 1—SLEW RATE

schematic



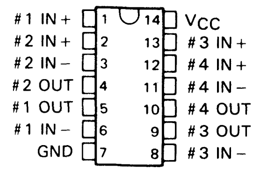
Component values shown are nominal.

TYPES LM2900, LM3900
QUADRUPLE OPERATIONAL AMPLIFIERS

D2531, JULY 1979—REVISED AUGUST 1983

- Wide Range of Supply Voltages, Single or Dual Supplies
- Wide Bandwidth
- Large Output Voltage Swing
- Output Short-Circuit Protection
- Internal Frequency Compensation
- Low Input Bias Current
- Designed to be Interchangeable with National Semiconductor LM2900 and LM3900, Respectively

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

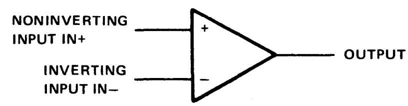


description

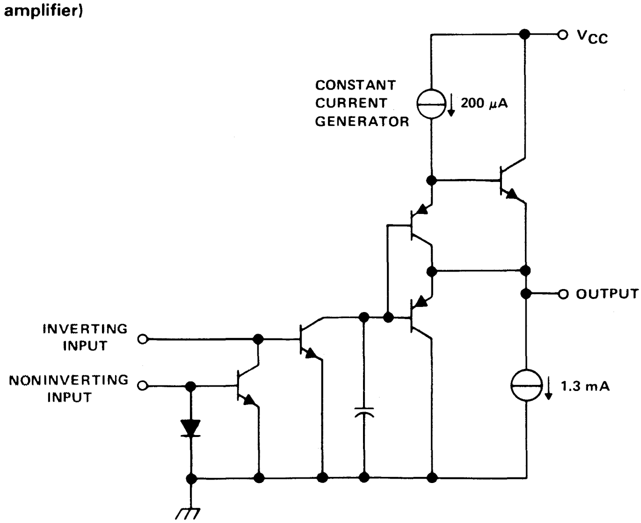
These devices consist of four independent, high-gain frequency-compensated Norton operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible. The low supply current drain is essentially independent of the magnitude of the supply voltage. These devices provide wide bandwidth and large output voltage swing.

The LM2900 is characterized for operation from −40°C to 85°C, and the LM3900 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM2900	LM3900	UNIT
Supply voltage, V_{CC} (see Note 1)		32	32	V
Input current		20	20	mA
Duration of output short circuit (one amplifier) to ground at (or below) 25 °C free-air temperature (see Note 2)		unlimited	unlimited	
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3)	J Package	1025	1025	mW
	N Package	875	875	
Operating free-air temperature range		−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J Package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N Package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, LM2900 and LM3900 chips are glass-mounted.

recommended operating comditions

	LM2900		LM3900		UNIT
	MIN	MAX	MIN	MAX	
Input current (see Note 4)		−1		−1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

NOTE 4: Clamp transistors are included that prevent the input voltages from swinging below ground more than approximately −0.3 volt. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately −1 mA. Negative input currents in excess of −4 mA will cause the output voltage to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode current biasing can be used to prevent negative input voltages.

electrical characteristics, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM2900 MIN	LM2900 TYP	LM2900 MAX	LM3900 MIN	LM3900 TYP	LM3900 MAX	UNIT
I_{IB}	Input bias current (inverting input)	$I_{I+} = 0$	T_A = 25°C		30	200		30	200	nA
			T_A = full range							
$\frac{I_{I-}}{I_{I+}}$	Mirror gain	I_{I+} = 20 μA to 200 μA, T_A = full range, See Note 5		0.9		1.1	0.9		1.1	μA/μA
	Change in mirror gain				2	5		2	15	%
	Mirror current	$V_{I+} = V_{I-}$, T_A = full range, See Note 5			10	500		10	500	μA
A_{VD}	Large-signal differential voltage amplification	V_O = 10 V, R_L = 10 kΩ, f = 100 Hz		1.2	2.8		1.2	2.8		V/mV
r_i	Input resistance (inverting input)				1			1		MΩ
r_o	Output resistance				8			8		kΩ
B_1	Unity-gain bandwidth (inverting input)				2.5			2.5		MHz
k_{SVR}	Supply voltage rejection ratio($\Delta V_{CC}/\Delta V_{IO}$)				70			70		dB
V_{OH}	High-level output voltage	$I_{I+} = 0$, $I_{I-} = 0$	R_L = 2 kΩ	13.5			13.5			V
			V_{CC} = 30 V, No load		29.5			29.5		
V_{OL}	Low-level output voltage	$I_{I+} = 0$, I_{I-} = 10 μA, R_L = 2 kΩ			0.09	0.2		0.09	0.2	V
I_{OHS}	Short-circuit output current (output internally high)	$I_{I+} = 0$, $I_{I-} = 0$, $V_O = 0$		−6	−18		−6	−10		mA
	Pull-down current			0.5	1.3		0.5	1.3		mA
I_{OL}	Low-level output current‡	I_{I-} = 5 μA, V_{OL} = 1 V			5			5		mA
I_{CC}	Supply current (four amplifiers)	No load			6.2	10		6.2	10	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for LM2900, and 0°C to 70°C for LM3900.

‡ The output current-sink capability can be increased for large-signal conditions by overdriving the inverting input.

NOTE 5: These parameters are measured with the output balanced midway between V_{CC} and ground.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	Low-to-high output	V_O = 10 V, C_L = 100 pF, R_L = 2 kΩ		0.5		V/μs
		High-to-low output			20		

3 Operational Amplifiers

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT (INVERTING INPUT)
vs
FREE-AIR TEMPERATURE

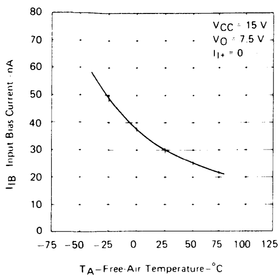


FIGURE 1

MIRROR GAIN
vs
FREE-AIR TEMPERATURE

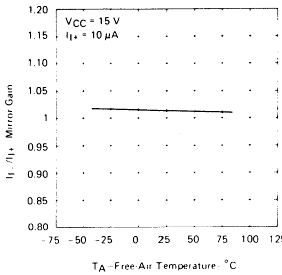


FIGURE 2

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

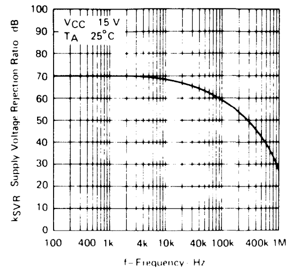


FIGURE 3

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

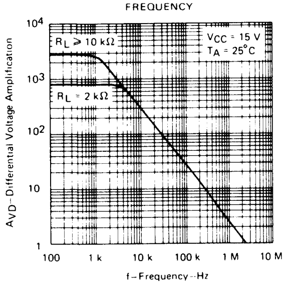


FIGURE 4

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

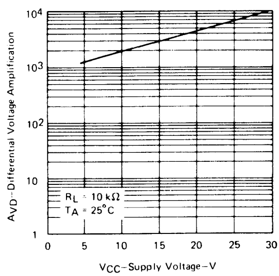


FIGURE 5

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

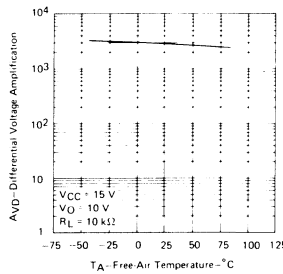


FIGURE 6

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

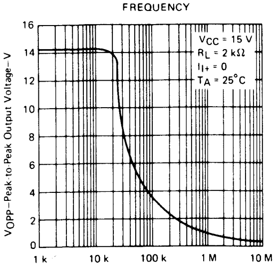


FIGURE 7

LM2900
SHORT-CIRCUIT OUTPUT CURRENT
(OUTPUT INTERNALLY HIGH)
vs
SUPPLY VOLTAGE

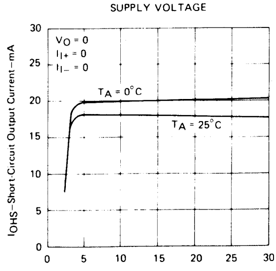


FIGURE 8

LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

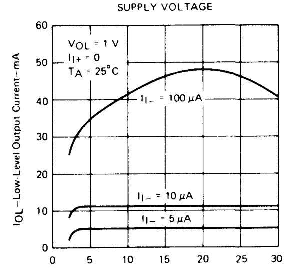


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PULL-DOWN CURRENT
vs
SUPPLY VOLTAGE

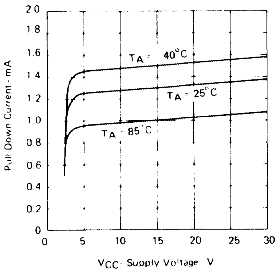


FIGURE 10

PULL-DOWN CURRENT
vs
FREE-AIR TEMPERATURE

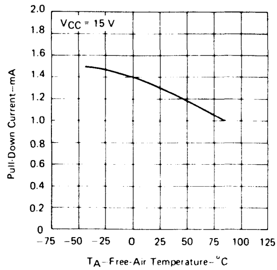


FIGURE 11

TOTAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE

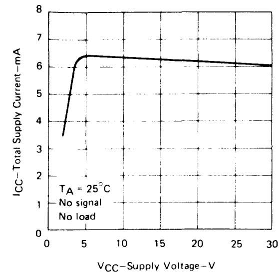


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

Norton (or current-differencing) amplifiers can be used in most standard general-purpose op-amp applications. Performance as a dc amplifier in a single-power-supply mode is not as precise as a standard integrated-circuit operational amplifier operating from dual supplies. Operation of the amplifier can best be understood by noting that input currents are differenced at the inverting input terminal and this current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near (or even below) ground.

Internal transistors clamp negative input voltages at pproximately −0.3 volt but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately −100 microamperes.

Noise immunity of a Norton amplifier is less than that of standard bipolar amplifiers. Circuit layout is more critical since coupling from the output to the noninverting input can cause oscillations. Care must also be exercised when driving either input from a low-impedance source. A limiting resistor should be placed in series with the input lead to limit the peak input current. Current up to 20 milliamperes will not damage the device but the current mirror on the noninverting input will saturate and cause a loss of mirror gain at higher current levels, especially at high operating temperatures.

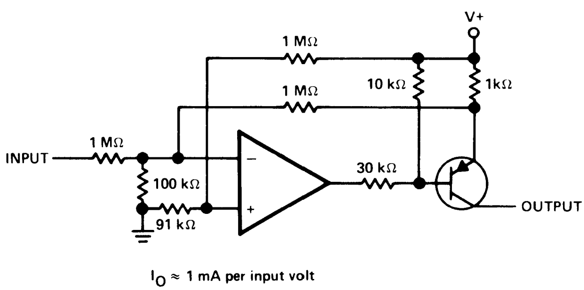


FIGURE 13—VOLTAGE-CONTROLLED CURRENT SOURCE

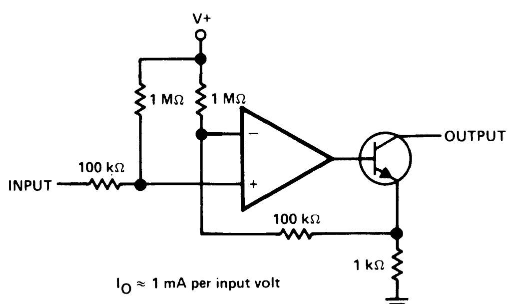


FIGURE 14—VOLTAGE-CONTROLLED CURRENT SINK

FEATURES

- Low Offset Voltage
  - LT1001AM 15μV max
  - LT1001C 60μV max
- Low Drift
  - LT1001AM 0.6μV/°C max
  - LT1001C 1.0μV/°C max
- Low Bias Current
  - LT1001AM 2nA max
  - LT1001C 4nA max
- CMRR
  - LT1001AM 114dB min
  - LT1001C 110dB min
- PSRR
  - LT1001AM 110dB min
  - LT1001C 106dB min
- Low Power Dissipation
  - LT1001AM 75mW max
  - LT1001C 80mW max
- Low Noise 0.3μV_{p-p}

APPLICATIONS

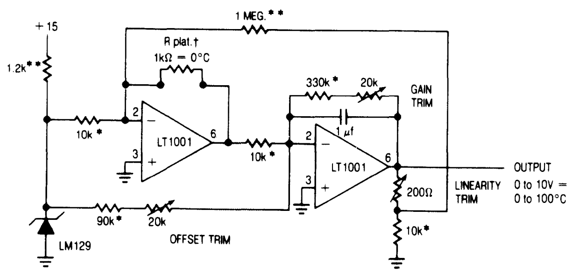
- Thermocouple amplifiers
- Strain gauge amplifiers
- Low level signal processing
- High accuracy data acquisition

DESCRIPTION

The LT1001 significantly advances the state-of-the-art of precision operational amplifiers. In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of the lowest cost, commercial temperature device, the LT1001C, have been dramatically improved when compared to equivalent grades of competing precision amplifiers.

Essentially, the input offset voltage of all units is less than 50μV (see distribution plot below). This allows the LT1001AM/883 to be specified at 15μV. Input bias and offset currents, common-mode and power supply rejection of the LT1001C offer performance which were previously attainable only with expensive, selected grades of other devices. Power dissipation is nearly halved compared to the most popular precision op amps, without adversely affecting noise or speed performance. A beneficial by-product of lower dissipation is decreased warm-up drift. Output drive capability of the LT1001 is also enhanced with voltage gain at 10 mA of load current. For similar performance in a dual precision op amp, with matching specifications, see the LT1002. Shown below is a platinum resistance thermometer application.

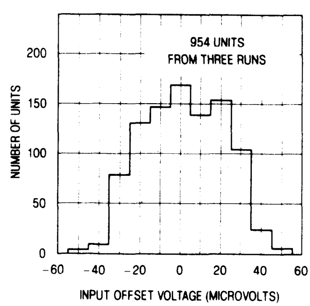
Linearized Platinum Resistance Thermometer with ±0.025°C Accuracy Over 0 to 100°C



* ULTRONIX 105A WIREWOUND
** 1% FILM
† PLATINUM RTD 118MF (ROSEMOUNT, INC.)

‡ Trim sequence: trim offset (0°C = 1000.0Ω), trim linearity (35°C = 1138.7Ω), trim gain (100°C = 1392.6Ω). Repeat until all three points are fixed with ± .025°C.

Typical Distribution of Offset Voltage $V_S = \pm 15V, T_A = 25°C$



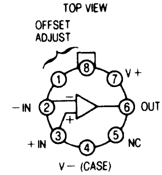
ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Differential Input Voltage .... ±30V
Input Voltage .... ±22V
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
  LT1001AM/LT1001M .... −55°C to 150°C
  LT1001AC/LT1001C .... 0°C to 125°C
  Storage: All Devices .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ...... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

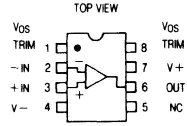


L PACKAGE
METAL CAN

ORDER PART NUMBER

LT1001AML/883
LT1001ML
LT1001ACL
LT1001CL

TOP VIEW



JG PACKAGE
8 PIN HERMETIC DIP

P PACKAGE
8 PIN PLASTIC DIP

LT1001AMJG/883
LT1001MJG
LT1001ACJG
LT1001CJG

LT1001ACP
LT1001CP

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883 LT1001AC MIN	TYP	MAX	LT1001M/LT1001C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Note 1 LT1001AM/883		7	15		18	60	μV
		LT1001AC		10	25				
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	Notes 2 and 3		0.2	1.0		0.3	1.5	μV/month
I_{OS}	Input Offset Current			0.3	2.0		0.4	3.8	nA
I_b	Input Bias Current			±0.5	±2.0		±0.7	±4.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.3	0.6		0.3	0.6	$\mu V_{p\text{-}p}$
e_n	Input Noise Voltage Density	f_o = 10Hz (Note 5) f_o = 1000Hz (Note 2)		10.3 9.6	18.0 11.0		10.5 9.8	18.0 11.0	$nV\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm12V$ $R_L \geq 1k\Omega$, $V_o = \pm10V$	450 300	800 500		400 250	800 500		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm13V$	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm3V$ to $\pm18V$	110	123		106	123		dB
R_{in}	Input Resistance Differential Mode	(Note 4)	30	100		15	80		MΩ
	Input Voltage Range		±13	±14		±13	±14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13 ±12	±14 ±13.5		±13 ±12	±14 ±13.5		V
S_R	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/μs
GBW	Gain-Bandwidth Product	(Note 4)	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation	No load No load, $V_s = \pm3V$		46 4	75 6		48 4	80 8	mW

See Notes on page 3.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AM/883 MIN	LT1001AM/883 TYP	LT1001AM/883 MAX	LT1001M MIN	LT1001M TYP	LT1001M MAX	UNITS
V_{OS}	Input Offset Voltage		●		30	60		45	160	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		0.8	4.0		1.2	7.6	nA
I_B	Input Bias Current		●		±1.0	±4.0		±1.5	±8.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	300	700		200	700		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	122		106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3$ to $\pm 18V$	●	104	117		100	117		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.5		±12.0	±13.5		V
P_d	Power Dissipation	No load	●		55	90		60	100	mW

$V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AC MIN	LT1001AC TYP	LT1001AC MAX	LT1001C MIN	LT1001C TYP	LT1001C MAX	UNITS
V_{OS}	Input Offset Voltage		●		20	60		30	110	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		0.5	3.5		0.6	5.3	nA
I_B	Input Bias Current		●		±0.7	±3.5		±1.0	±5.5	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	350	750		250	750		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	124		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	106	120		103	120		dB
	Input Voltage Range		●	±13	±14		±13	±14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.8		±12.5	±13.8		V
P_d	Power Dissipation	No load	●		50	85		55	90	mW

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage for the LT1001AM/883 and LT1001AC are measured after power is applied and the device is fully warmed up. All other grades are measured with high speed test equipment, approximately 1 second after power is applied. The LT1001AM/883 receives 168 hr. burn-in at 125°C. or equivalent.

Note 2: This parameter is tested on a sample basis only.

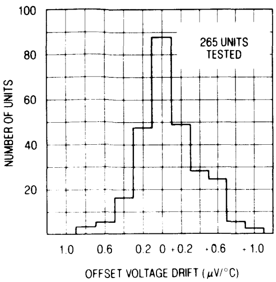
Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 4: Parameter is specified by design.

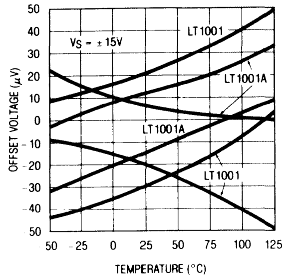
Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

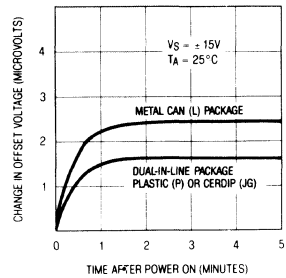
Typical Distribution of Offset Voltage Drift with Temperature



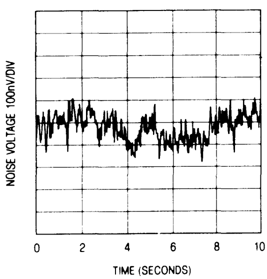
Offset Voltage Drift with Temperature of Representative Units



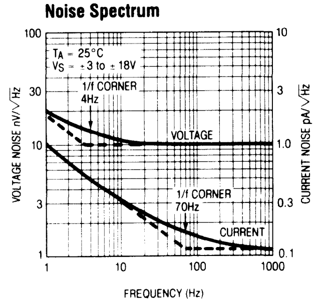
Warm-Up Drift



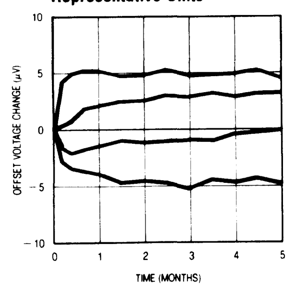
0.1Hz to 10Hz Noise



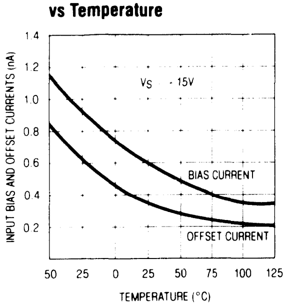
Noise Spectrum



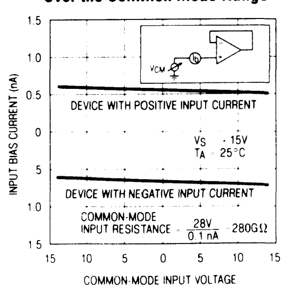
Long Term Stability of Four Representative Units



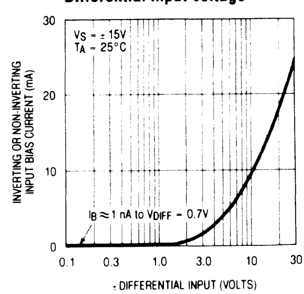
Input Bias and Offset Current vs Temperature



Input Bias Current Over the Common Mode Range

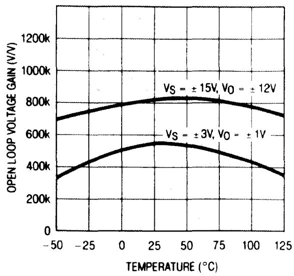


Input Bias Current vs. Differential Input Voltage

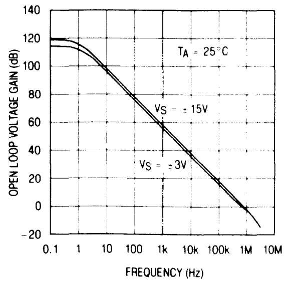


TYPICAL PERFORMANCE CHARACTERISTICS

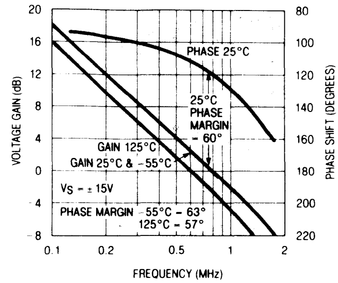
Open Loop Voltage Gain vs Temperature



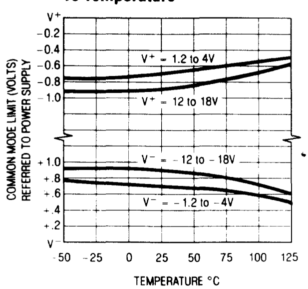
Open Loop Voltage Gain Frequency Response



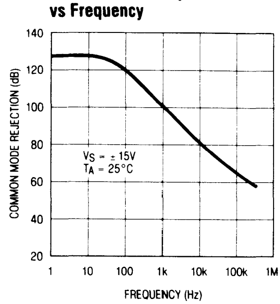
Gain, Phase Shift vs. Frequency



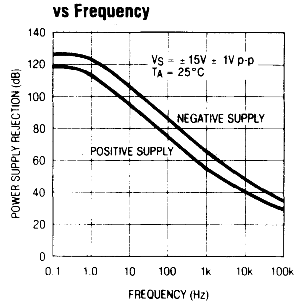
Common Mode Limit vs Temperature



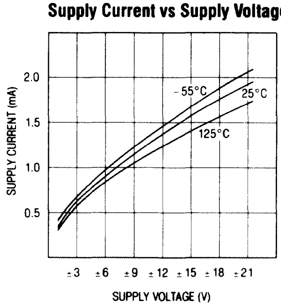
Common Mode Rejection Ratio vs Frequency



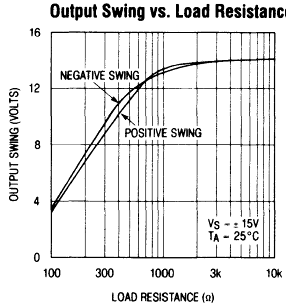
Power Supply Rejection Ratio vs Frequency



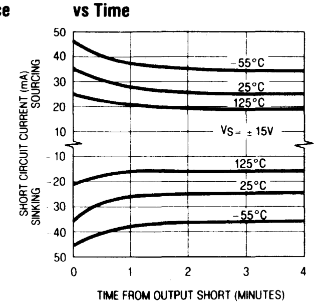
Supply Current vs Supply Voltage



Output Swing vs. Load Resistance



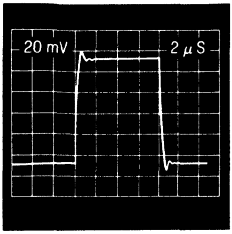
Output Short Circuit Current vs Time



3 Operational Amplifiers

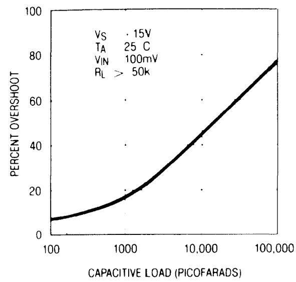
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Transient Response

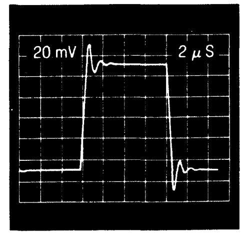


A_V = +1, C_L = 50pF

Voltage Follower Overshoot vs Capacitive Load

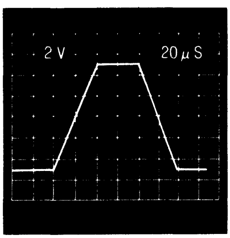


Small Signal Transient Response

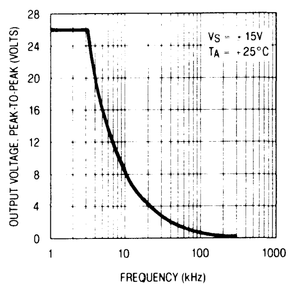


A_V = +1, C_L = 1000pF

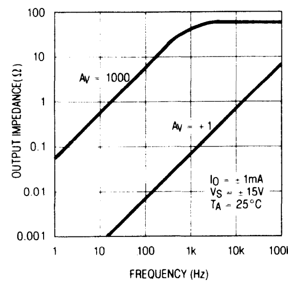
Large Signal Transient Response



Maximum Undistorted Output vs. Frequency



Closed Loop Output Impedance



APPLICATIONS INFORMATION

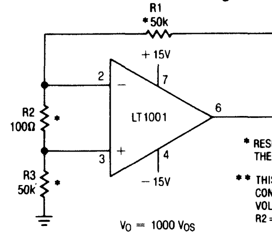
Application Notes and Test Circuits

The LT1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1001 is specified over a wide range of power supply voltages from ±3V to ±18V. Operation with lower supplies is possible down to ±1.2V (two Ni-Cad batteries). However, with ±1.2V supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature



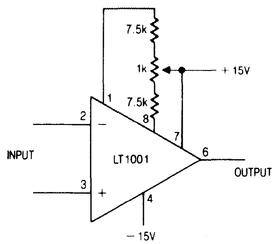
* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

** THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1001, WITH SUPPLY VOLTAGES INCREASED TO ±20V, R1 = R3 = 10k, R2 = 200Ω, A_V = 100.

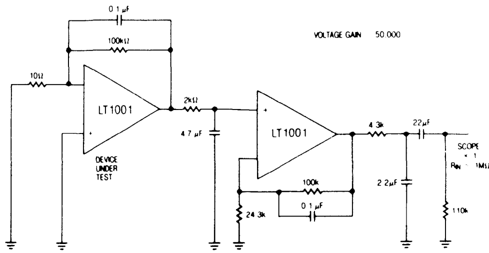
Offset Voltage Adjustment

The input offset voltage of the LT1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of Vos is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (Vos/300) μV/°C, e.g. if Vos is adjusted to 300 μV, the change in drift will be 1 μV/°C. The adjustment range with a 10k or 20k pot is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of ± 100 μV.

Improved Sensitivity Adjustment



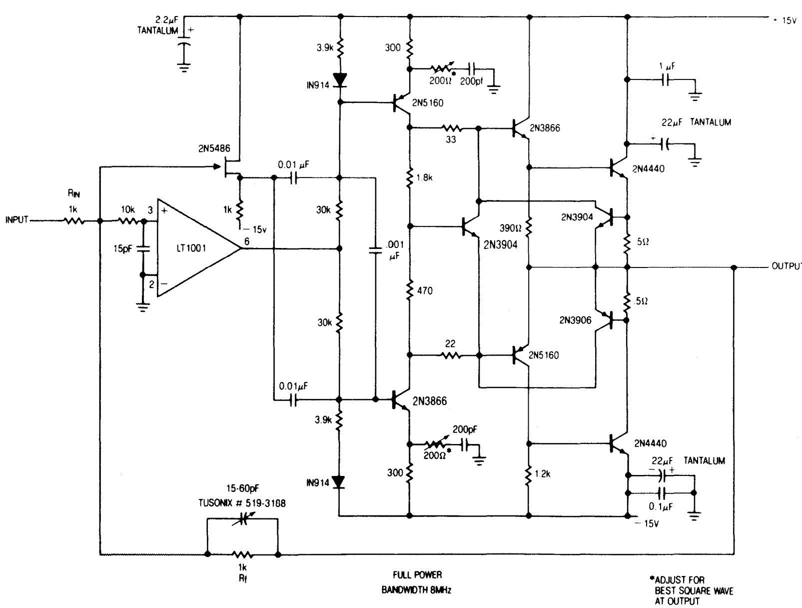
0.1Hz to 10Hz Noise Test Circuit



(Peak to Peak noise measured in 10 Sec interval)

The device under test should be warmed up for three minutes and shielded from air currents.

DC Stabilized 1000v/μsec Op Amp

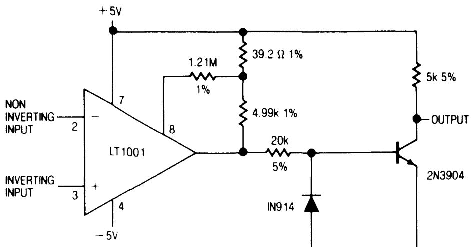


FULL POWER BANDWIDTH 8MHz

*ADJUST FOR BEST SQUARE WAVE AT OUTPUT

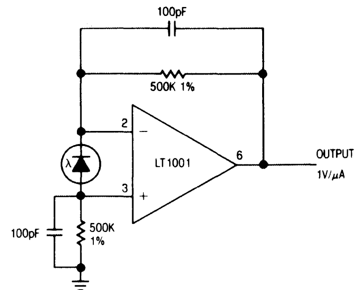
TYPICAL APPLICATIONS

Microvolt Comparator with TTL Output

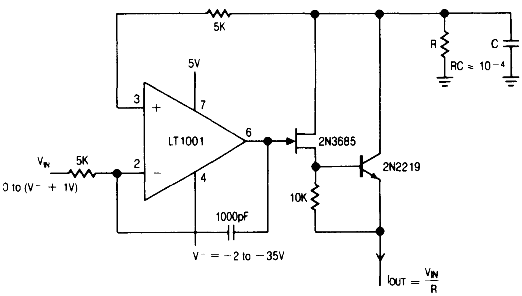


Positive feedback to one of the nulling terminals creates 5 μ to 20 μV of hysteresis. Input offset voltage is typically changed by less than 5 μV due to the feedback.

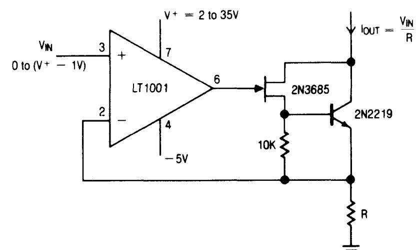
Photodiode Amplifier



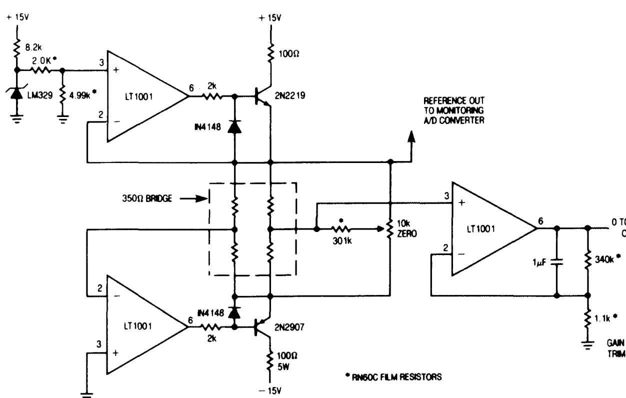
Precision Current Source



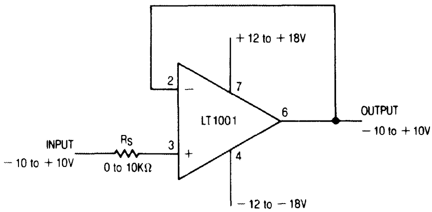
Precision Current Sink



Strain Gauge Signal Conditioner with Bridge Excitation



Large Signal Voltage Follower With 0.001% Worst-Case Accuracy

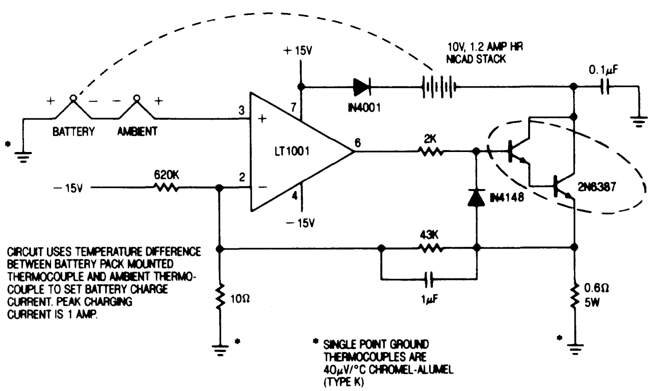


The voltage follower is an ideal example illustrating the overall excellence of the LT1001. The contributing error terms are due to offset voltage, input bias current, voltage gain, common-mode and power-supply rejections. Worst-case summation of specifications is tabulated below.

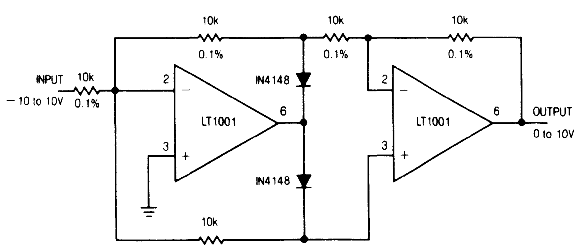
OUTPUT ACCURACY

Error	LT1001AM /883 25°C Max.	LT1001C 25°C Max.	LT1001AM /883 −55 to 125°C Max.	LT1001C 0 to 70°C Max.
Offset Voltage	15μV	60μV	60μV	110μV
Bias Current	20μV	40μV	40μV	55μV
Common-Mode Rejection	20μV	30μV	30μV	50μV
Power Supply Rejection	18μV	30μV	36μV	42μV
Voltage Gain	22μV	25μV	33μV	40μV
Worst-case Sum	95μV	185μV	199μV	297μV
Percent of Full Scale (=20V)	0.0005%	0.0009%	0.0010%	0.0015%

Thermally Controlled Nicad Charger

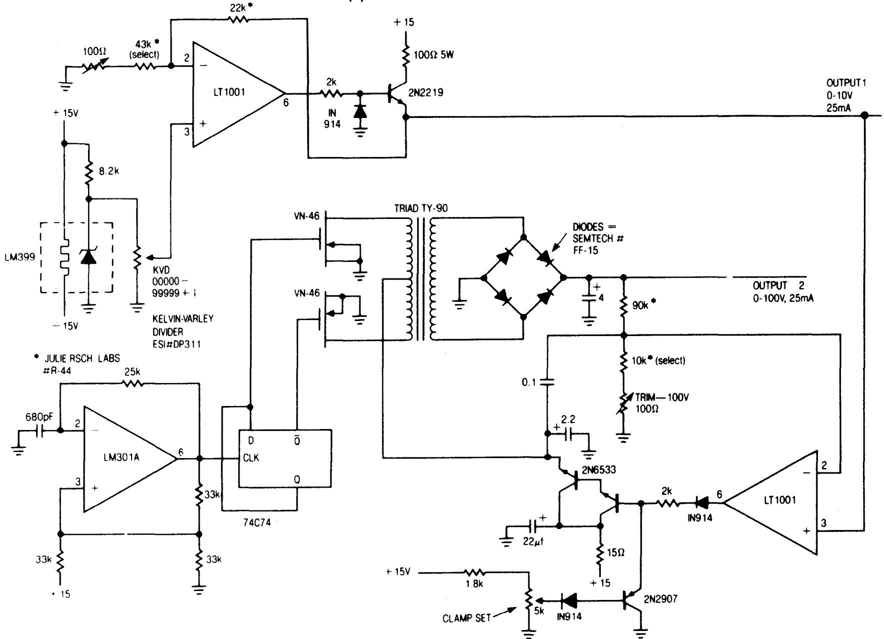


Precision Absolute Value Circuit



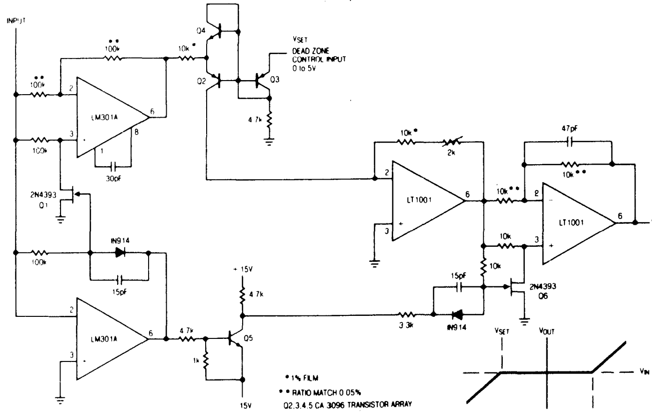
Precision Power Supply with Two Outputs

(1) 0 to 10V in 100μV STEPS
(2) 0 to 100V in 1mV STEPS

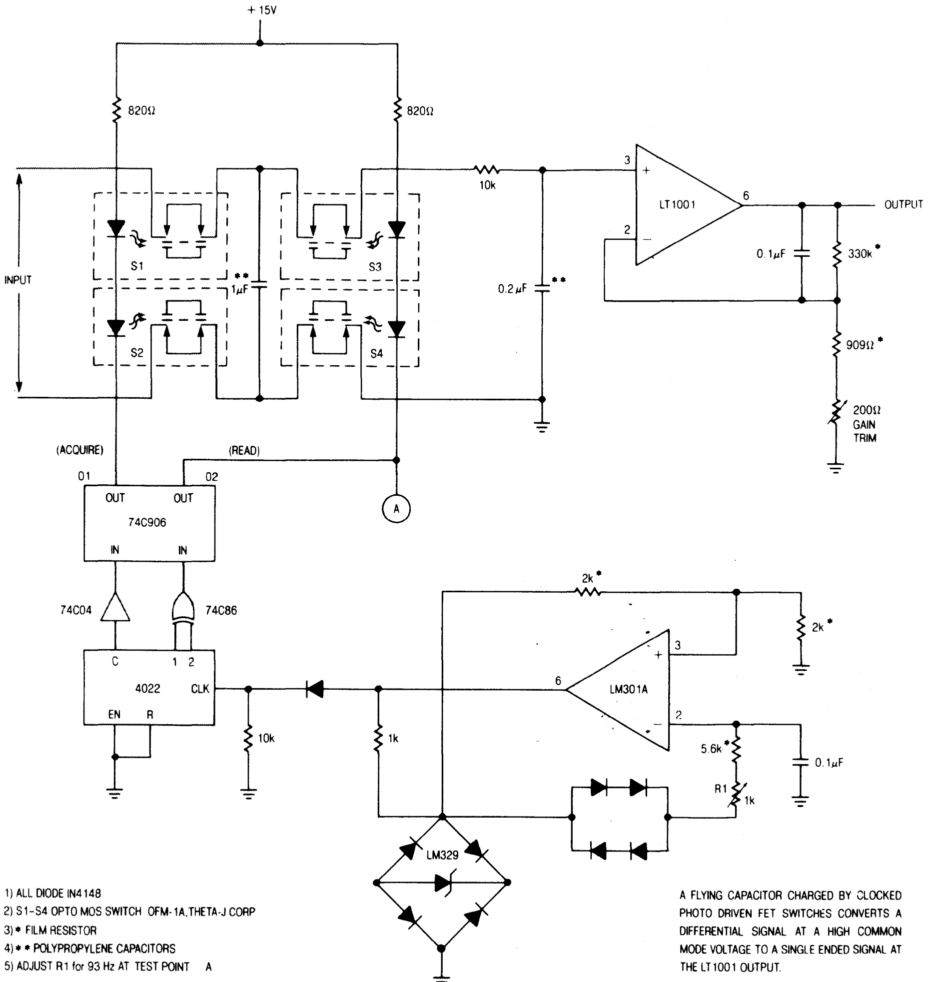


Dead Zone Generator

BIPOLAR SYMMETRY IS EXCELLENT BECAUSE ONE DEVICE, Q2, SETS BOTH LIMITS



Instrumentation Amplifier with ±300V Common Mode Range and CMRR > 150dB

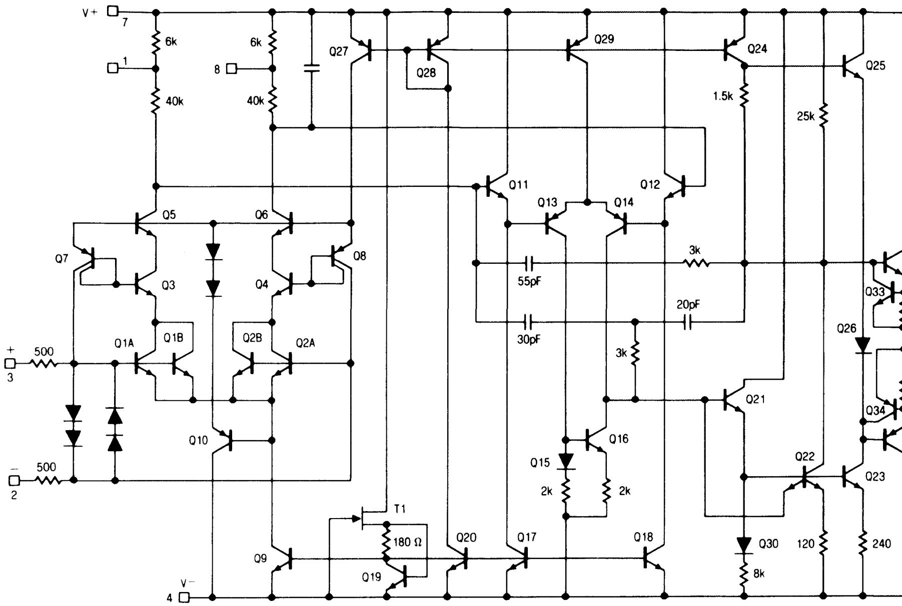


1) ALL DIODE IN4148
2) S1–S4 OPTO MOS SWITCH OFM-1A,THETA-J CORP
3) * FILM RESISTOR
4) ** POLYPROPYLENE CAPACITORS
5) ADJUST R1 for 93 Hz AT TEST POINT A

A FLYING CAPACITOR CHARGED BY CLOCKED PHOTO DRIVEN FET SWITCHES CONVERTS A DIFFERENTIAL SIGNAL AT A HIGH COMMON MODE VOLTAGE TO A SINGLE ENDED SIGNAL AT THE LT1001 OUTPUT.

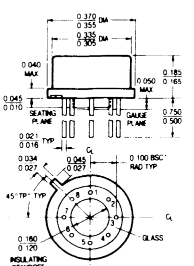
SCHEMATIC DIAGRAM

LT1001 Schematic Diagram



PACKAGE DESCRIPTION

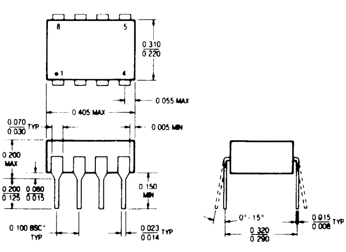
L Package
Metal Can



NOTE DIMENSIONS IN INCHES

$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

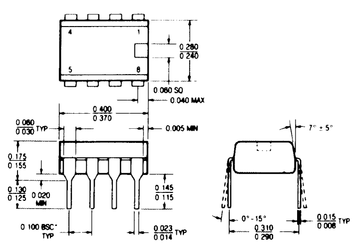
JG Package
8 Lead Hermetic Dip



NOTE DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
150°C	100°C/W

P Package
8 Lead Plastic



NOTE DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	θ_{ja}
100°C	130°C/W

FEATURES

- 4.5 nV/√Hz 10 Hz noise
- 3.8 nV/√Hz 1kHz noise
- 0.1 Hz to 10 Hz noise, 60 nV p-p, typical
- 7 million min. voltage gain, $R_L = 2k\Omega$
- 3 million min. voltage gain, $R_L = 600\Omega$
- 25μV max. offset voltage
- 0.6μV/°C max. drift with temperature
- 11V/μsec min. slew rate (LT1037)
- 117 dB min. CMRR

APPLICATIONS

- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Sine Wave Generators
- Tape Head Preamplifiers
- Microphone Preamplifiers

DESCRIPTION

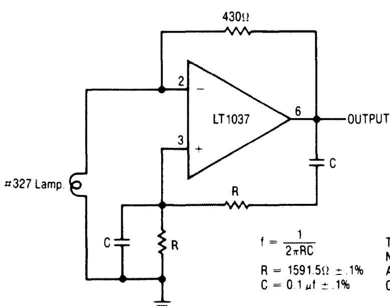
The LT1007/LT1037 series features the lowest noise performance available to date for monolithic operational amplifiers: 2.5nV/√Hz wideband noise (less than the noise of a 400Ω resistor), 1/f corner frequency of 2Hz and 60nV peak to peak 0.1Hz to 10Hz noise. Low noise is combined with outstanding precision and speed specifications: 10μV offset voltage, 0.2μV/°C drift, 130 dB common-mode and power supply rejection, and 60MHz gain-bandwith-product on the decompensated LT1037, which is stable for closed loop gains of 5 or greater.

The voltage gain of the LT1007/1037 is an extremely high 20 million driving a 2kΩ load and 12 million driving a 600Ω load to ± 10V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of even the lowest cost grades (the LT1007C and the LT1037C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

The sine wave generator application shown below utilizes the low noise and low distortion characteristics of the LT1037.

Ultra-Pure 1kHz Sine Wave Generator

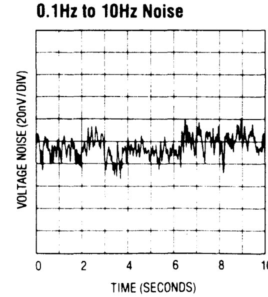


$f = \frac{1}{2\pi RC}$

R = 1591.5Ω ± .1%
C = 0.1μf ± .1%

Total Harmonic Distortion = < .0025%
Noise = < .0001%
Amplitude = ± 8 volts
Output Frequency = 1.000kHz for values given ± .4%

0.1Hz to 10Hz Noise



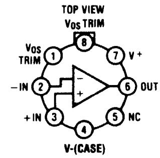
ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

TEXAS INSTRUMENTS

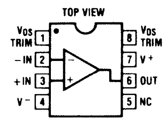
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Input Voltage .... Equal to Supply Voltage
Output Short Circuit Duration .... Indefinite
Differential Input Current (Note 8)......... ±25mA
Lead Temperature (Soldering, 10 sec.)....... 300°C
Operating Temperature Range
  LT1007/1037AM, M........... −55°C to 125°C
  LT1007/1037AC, C .... 0°C to 70°C
Storage Temperature Range
  All Devices.................. −65°C to 150°C

PACKAGE/ORDER INFORMATION



METAL CAN L PACKAGE



HERMETIC DIP JG PACKAGE
PLASTIC DIP P PACKAGE

ORDER PART NUMBER	
LT1007AML	LT1037AML
LT1007ML	LT1037ML
LT1007ACL	LT1037ACL
LT1007CL	LT1037CL
LT1007AMJG	LT1037AMJG
LT1007MJG	LT1037MJG
LT1007ACJG	LT1037ACJG
LT1007CJG	LT1037CJG
LT1007ACP	LT1037ACP
LT1007CP	LT1037CP

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1007AM/AC LT1037AM/AC MIN	TYP	MAX	LT1007M/C LT1037M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	25		20	60	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0		0.2	1.0	μV/Mo
I_{OS}	Input Offset Current			7	30		12	50	nA
I_B	Input Bias Current			±10	±35		±15	±55	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 3 and 5)		0.06	0.13		0.06	0.13	μVp-p
	Input Noise Voltage Density	f_o = 10Hz (Notes 3 and 4) f_o = 1000Hz (Note 3)		2.8 2.5	4.5 3.8		2.8 2.5	4.5 3.8	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_o = 10Hz (Notes 3 and 6) f_o = 1000Hz (Notes 3 and 6)		1.5 0.4	4.0 0.6		1.5 0.4	4.0 0.6	$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance — Common Mode			7			5		GΩ
	Input Voltage Range		±11.0	±12.5		±11.0	±12.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$	117	130		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	110	130		106	126		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 12V$ $R_L \geq 1k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	7.0 5.0 3.0	20.0 16.0 12.0		5.0 3.5 2.0	20.0 16.0 12.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±13.0 ±11.0	±13.8 ±12.5		±12.5 ±10.5	±13.5 ±12.5		V V
SR	Slew Rate LT1007 LT1037	$R_L \geq 2k\Omega$ $A_{VCL} \geq 5$	1.7 11	2.5 15		1.7 11	2.5 15		V/μS V/μS
GBW	Gain-Bandwidth Product: LT1007 LT1037	f_o = 100kHz (Note 7) f_o = 10kHz (Note 7) ($A_{VCL} \geq 5$)	5.0 45	8.0 60		5.0 45	8.0 60		MHz MHz
Z_o	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		70			70		Ω
P_d	Power Dissipation LT1007 LT1037			80 80	120 130		80 85	140 140	mW mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1007AM/LT1037AM MIN	TYP	MAX	LT1007M/LT1037M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		25	60		50	160	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 9)	●		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		15	50		20	85	nA
I_B	Input Bias Current		●		±20	±60		±35	±95	nA
	Input Voltage Range		●	±10.3	±11.5		±10.3	±11.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	●	112	126		104	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	104	126		100	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$ $R_L \geq 1k\Omega$, $V_o = \pm 10V$	● ●	3.0 2.0	14.0 10.0		2.0 1.5	14.0 10.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.5		±12.0	±13.5		V
P_d	Power Dissipation		●		100	150		100	170	mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1007AC/LT1037AC MIN	TYP	MAX	LT1007C/LT1037C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		20	50		35	110	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 9)	●		0.2	0.6		0.3	1.0	μV/°C
I_{OS}	Input Offset Current		●		10	40		15	70	nA
I_B	Input Bias Current		●		±14	±45		±20	±75	nA
	Input Voltage Range		●	±10.5	±11.8		±10.5	±11.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	114	126		106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	106	126		102	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$ $R_L \geq 1k\Omega$, $V_o = \pm 10V$	● ●	4.0 2.5	18.0 14.0		2.5 2.0	18.0 14.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.6		±12.0	±13.6		V
P_d	Power Dissipation		●		90	144		90	160	mW

NOTES:

The ● denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. AM and AC grades are guaranteed fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 5: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section.

Note 6: See the test circuit for current noise measurement in the Applications Information section.

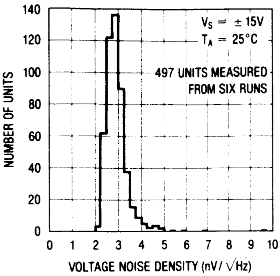
Note 7: This parameter is not tested.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

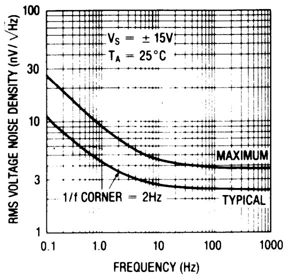
Note 9: The Average Input Offset Drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS

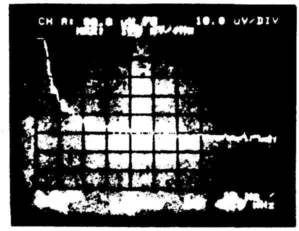
10Hz Voltage Noise Distribution



Voltage Noise vs Frequency



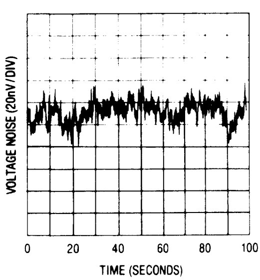
0.02 to 10Hz RMS Noise. Gain = 50,000 (Measured on HP3582 Spectrum Analyzer)



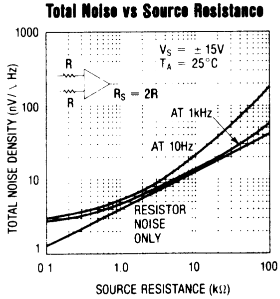
Marker at 2Hz (= 1/f corner) =

$$\frac{179\mu V/\sqrt{Hz}}{50,000} = 3.59 \frac{nV}{\sqrt{Hz}}$$

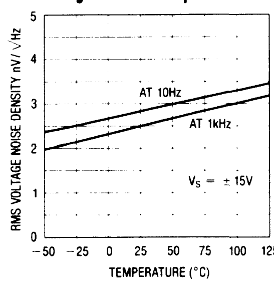
0.01 to 1Hz Peak to Peak Noise



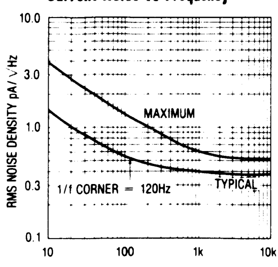
Total Noise vs Source Resistance



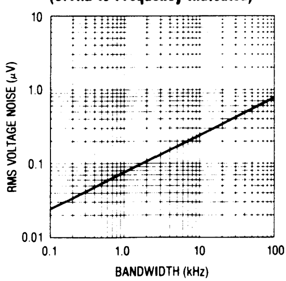
Voltage Noise vs Temperature



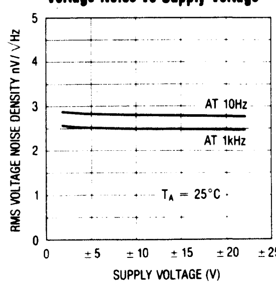
Current Noise vs Frequency



Wideband Voltage Noise (0.1Hz to Frequency Indicated)



Voltage Noise vs Supply Voltage

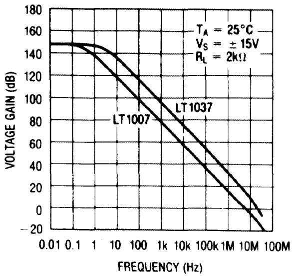


3 Operational Amplifiers

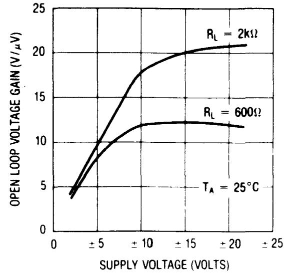
TEXAS INSTRUMENTS

TYPICAL PERFORMANCE CHARACTERISTICS

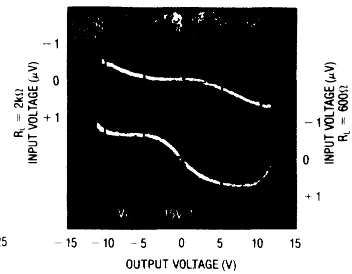
Voltage Gain vs Frequency



Voltage Gain vs Supply Voltage

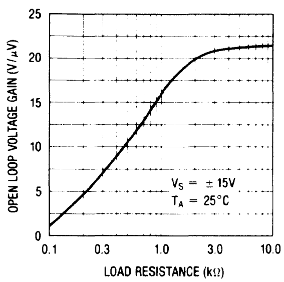


Voltage Gain, R_L = 2K and 600Ω

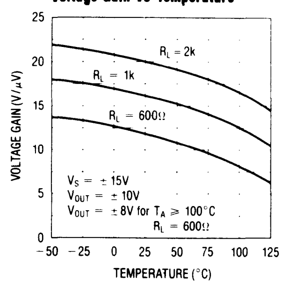


MEASURED ON TEKTRONIX 178 LINEAR IC TESTER

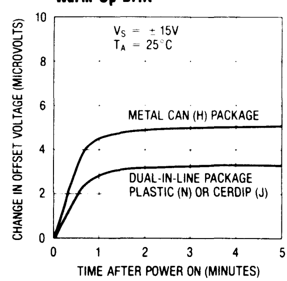
Voltage Gain vs Load Resistance



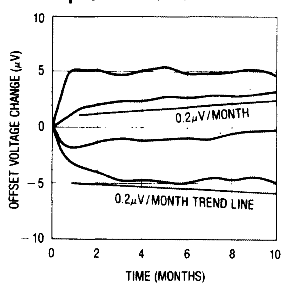
Voltage Gain vs Temperature



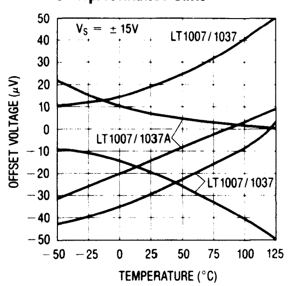
Warm-Up Drift



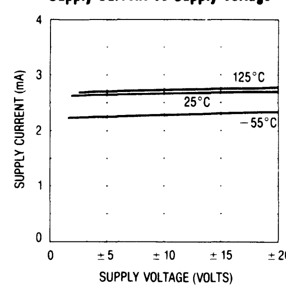
Long Term Stability of Four Representative Units



Offset Voltage Drift with Temperature of Representative Units

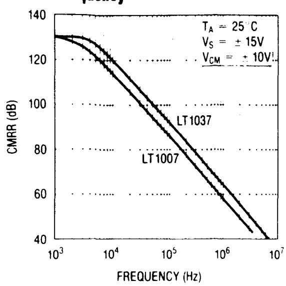


Supply Current vs Supply Voltage

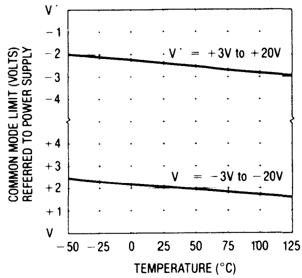


TYPICAL PERFORMANCE CHARACTERISTICS

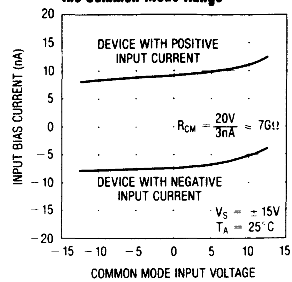
Common Mode Rejection vs Frequency



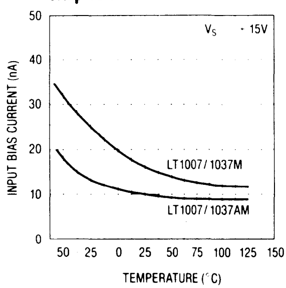
Common Mode Limit vs Temperature



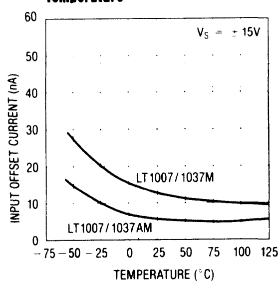
Input Bias Current Over the Common Mode Range



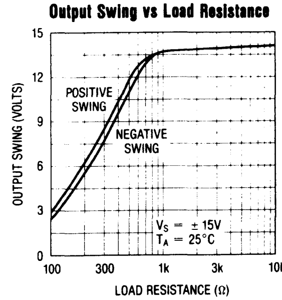
Input Bias Current vs Temperature



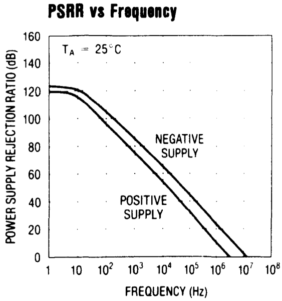
Input Offset Current vs Temperature



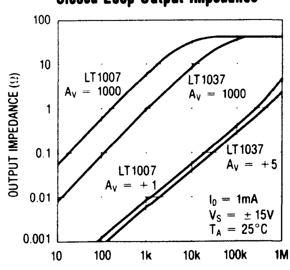
Output Swing vs Load Resistance



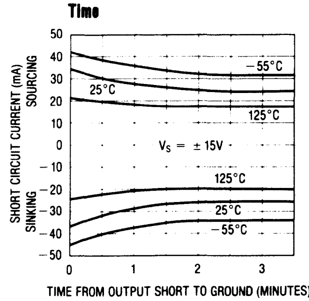
PSRR vs Frequency



Closed Loop Output Impedance

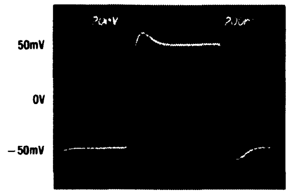


Output Short Circuit Current vs Time



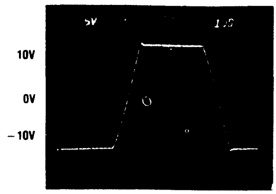
TYPICAL PERFORMANCE CHARACTERISTICS

LT1037 Small Signal Transient Response



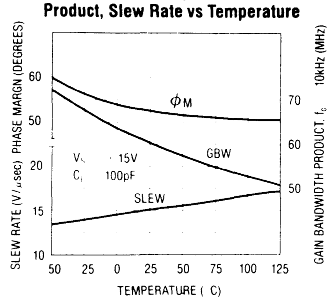
$A_{VCL} = +5$, $V_S = \pm 15V$
$C_L = 15pF$

LT1037 Large Signal Response

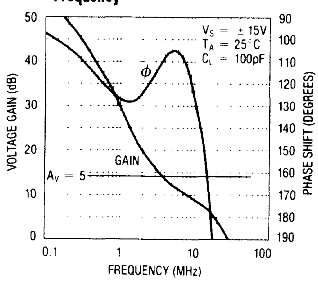


$A_{VCL} = +5$, $V_S = \pm 15V$

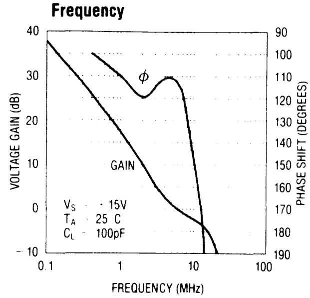
LT1037 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



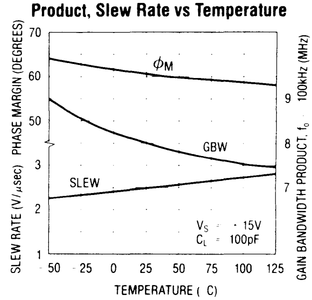
LT1037 Gain, Phase Shift vs Frequency



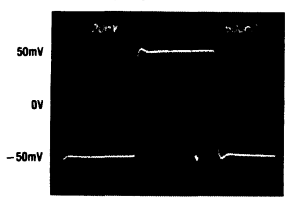
LT1007 Gain, Phase Shift vs Frequency



LT1007 Phase Margin, Gain-Bandwidth Product, Slew Rate vs Temperature

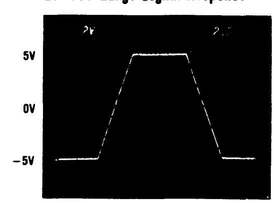


LT1007 Small Signal Transient Response



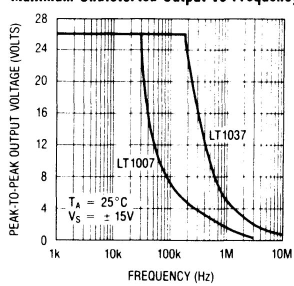
$A_{VCL} = +1$, $V_S = \pm 15V$
$C_L = 15pF$

LT1007 Large Signal Response



$A_{VCL} = -1$, $V_S = \pm 15V$

Maximum Undistorted Output vs Frequency



APPLICATIONS INFORMATION

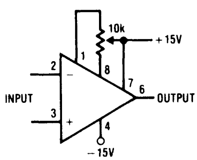
General

The LT1007/1037 series devices may be inserted directly into OP-07, OP-27, OP-37, and 5534 sockets with or without removal of external compensation or nulling components. In addition, the LT1007/1037 may be fitted to 741 sockets with the removal or modification of external nulling components.

Offset Voltage Adjustment

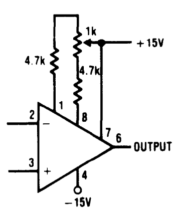
The input offset voltage of the LT1007/1037 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 10k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300)\ \mu V/°C$, e.g., if V_{OS} is adjusted to $300\mu V$, the change in drift will be $1\mu V/°C$.

Standard Adjustment



The adjustment range with a 10k pot is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of $\pm 200\mu V$.

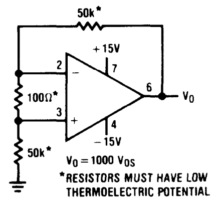
Improved Sensitivity Adjustment



Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

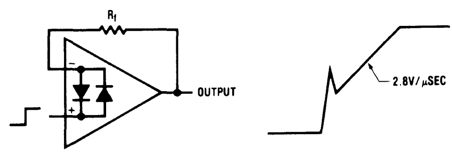
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1007/1037, with the supply voltages increased to ±20V.



Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature

Unity Gain Buffer Applications (LT1007 Only)

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_f will eliminate this problem.

APPLICATIONS INFORMATION — NOISE

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1007/1037 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 60nV peak-to-peak noise performance of the LT1007/1037 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 3μV due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

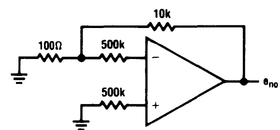
(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured in the circuit shown and calculated by the following formula:

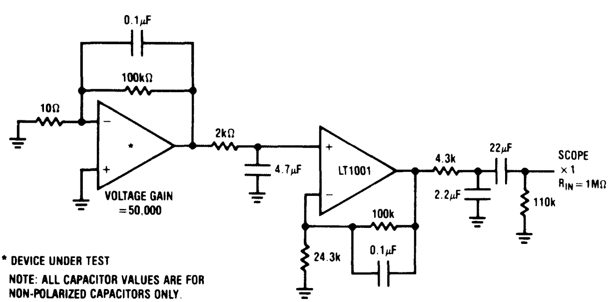
$$i_n = \frac{[e^2_{no} - (130nV)^2]^{1/2}}{1M\Omega \times 100}$$



The LT1007/1037 achieves its low noise, in part, by operating the input stage at 120μA versus the typical 10μA of most other op amps. Voltage noise is inversely proportional while current noise is directly proportional to the square root of the stage current. Therefore the LT1007/1037's current noise will be relatively high. At low frequencies, the low 1/f current noise corner frequency (≈120Hz) minimizes current noise to some extent.

In most practical applications, however, current noise will not limit system performance. This is illustrated in

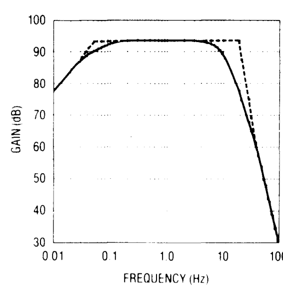
0.1Hz to 10Hz Noise Test Circuit



* DEVICE UNDER TEST

NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY.

0.1Hz to 10Hz p-p Noise Tester Frequency Response



the total noise versus source resistance plot, where total noise = [(voltage noise)^2 + (current noise × R_S)^2 + (resistor noise)^2]$^{1/2}$

Three regions can be identified as a function of source resistance:

(i) $R_S \leq 400\Omega$. Voltage noise dominates

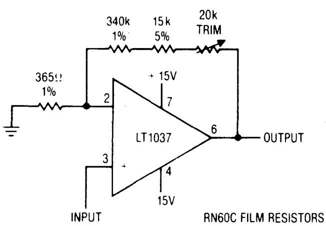
(ii) $400\Omega \leq R_S \leq 50k\Omega$ at 1kHz, $400\Omega \leq R_S \leq 8k\Omega$ at 10Hz } Resistor noise dominates

(iii) $R_S > 50k\Omega$ at 1kHz, $R_S > 8k\Omega$ at 10Hz } Current noise dominates

Clearly the LT1007/1037 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted.

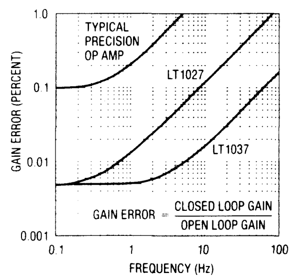
TYPICAL APPLICATIONS

Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz

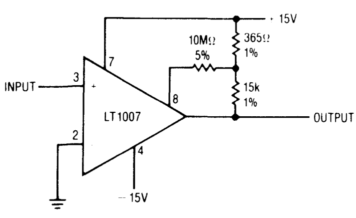


The high gain and wide bandwidth of the LT1037 and (LT1007) is useful in low frequency high closed loop gain amplifier applications. A typical precision Op Amp may have an open loop gain of one million with 500kHz bandwidth. As the gain error plot shows, this device is capable of 0.1% amplifying accuracy up to 0.3Hz only. Even instrumentation range signals can vary at a faster rate. The LT1037's "gain precision — bandwidth product" is 200 times higher, as shown.

Gain Error vs Frequency Closed Loop Gain = 1000



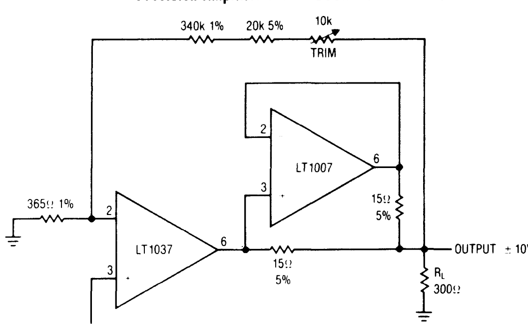
Microvolt Comparator with Hysteresis



Positive feedback to one of the nulling terminals creates approximately 5µV of hysteresis. Output can sink 16mA.

Input offset voltage is typically changed less than 5µV due to the feedback.

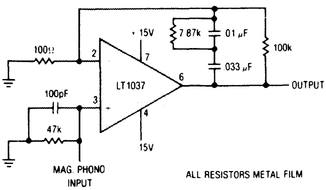
Precision Amplifier Drives 300Ω Load to ±10V



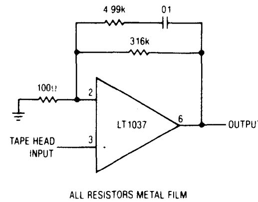
The addition of the LT1007 doubles the amplifier's output drive to ±33mA. Gain accuracy is 0.02%, slightly degraded compared to above because of self heating of the LT1037 under load.

TYPICAL APPLICATIONS

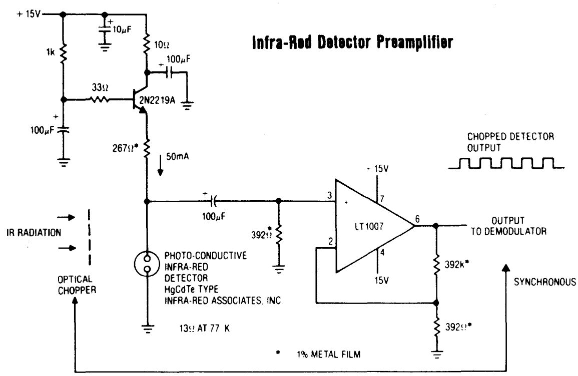
Phono Preamplifier



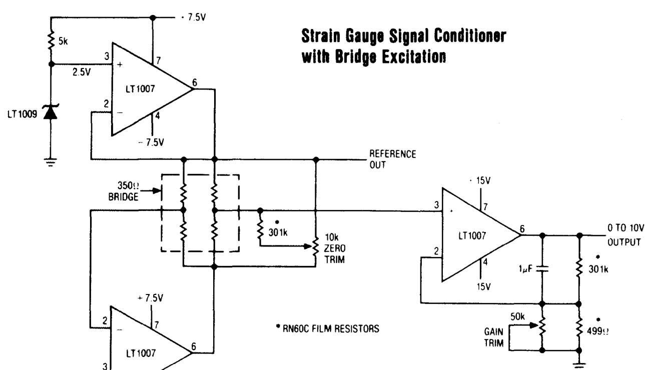
Tape Head Amplifier



Infra-Red Detector Preamplifier

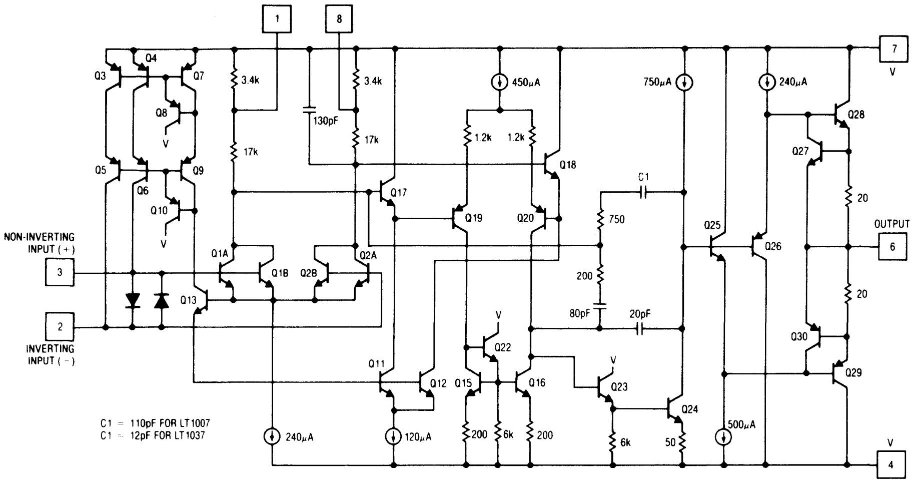


Strain Gauge Signal Conditioner with Bridge Excitation



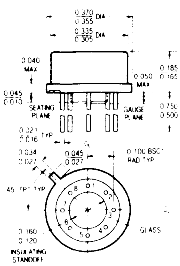
The LT1007 is capable of providing excitation current directly to bias the 350Ω bridge at 5V. With only 5V across the bridge (as opposed to the usual 10V) total power dissipation and bridge warm-up drift is reduced. The bridge output signal is halved, but the LT1007 can amplify the reduced signal accurately.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

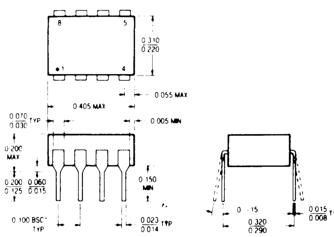
L Package
Metal Can



NOTE: DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

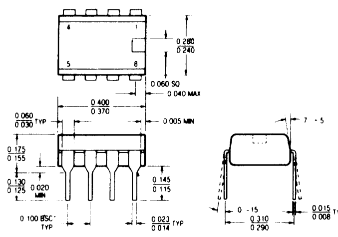
JG Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

P Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
100°C	130°C/W

PICOAMP INPUT CURRENT, MICROVOLT OFFSET LOW NOISE OP AMP

MAY 1988

FEATURES

- Bias Current
  - 25°C .... 100pA max.
  - −55°C to 125°C .... 600pA max.
- Offset Voltage .... 120μV max.
- Drift .... 1.5μV/°C max.
- Low Noise, 0.1Hz to 10Hz .... 0.5μ Vp-p
- Low Supply Current .... 600μA max.
- CMRR .... 114 dB min.
- PSRR .... 114 db min.
- Voltage Gain with 5mA load current

APPLICATIONS

- Precision instrumentation
- Charge integrators
- Wide dynamic range logarithmic amplifiers
- Light meters
- Low frequency active filters
- Standard cell buffers
- Thermocouple amplifiers

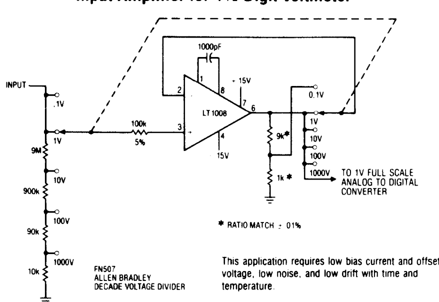
DESCRIPTION

The LT1008 is a universal precision operational amplifier which can be used in practically all precision applications. The LT1008 combines for the first time picoampere bias currents (which are maintained over the full −55°C to 125°C temperature range) microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, and the ability to deliver 5mA load current with high voltage gain round out the LT1008's superb precision specifications.

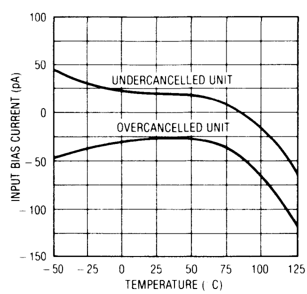
The all around excellence of the LT1008 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1008 can be stocked as the universal precision op amp.

The LT1008 is externally compensated with a single capacitor for additional flexibility in shaping the frequency response of the amplifier. It plugs into and upgrades all standard LM108A/308A applications. For an internally compensated version with even lower offset voltage but otherwise similar performance see the LT1012.

Input Amplifier for 4½ Digit Voltmeter



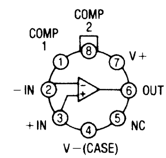
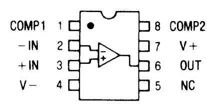
Input Bias Current vs Temperature



ABSOLUTE MAXIMUM RATING

Supply Voltage .... ±20V
Differential Input Current (Note 1) .... ±10mA
Input Voltage .... ±20V
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
  LT1008M .... −55°C to 125°C
  LT1008C .... 0°C to 70°C
Storage Temperature Range
  All Devices .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ...... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NO.
 METAL CAN (L) PACKAGE	LT1008ML LT1008CL
 HERMETIC DIP JG PACKAGE PLASTIC DIP P PACKAGE	LT1008MJG LT1008CJG LT1008CP

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1008M MIN	LT1008M TYP	LT1008M MAX	LT1008C MIN	LT1008C TYP	LT1008C MAX	UNITS
V_{OS}	Input Offset Voltage			30	120		30	120	μV
		Note 2		40	180		40	180	μV
	Long Term Input Offset Voltage Stability			0.3			0.3		μV/month
I_{OS}	Input Offset Current			30	100		30	100	pA
		Note 2		40	150		40	150	pA
I_B	Input Bias Current			±30	±100		±30	±100	pA
		Note 2		±40	±150		±40	±150	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
e_n	Input Noise Voltage Density	f_0 = 10Hz (Note 3)		17	30		17	30	$nV/\sqrt{Hz}$
		f_0 = 1000Hz (Note 4)		14	22		14	22	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_0 = 10Hz		20			20		$fA/\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L \geq 10k\Omega$	200	2000		200	2000		V/mV
		$V_{OUT} = \pm10V$, $R_L \geq 2k\Omega$	120	600		120	600		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm13.5V$	114	132		114	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2V$ to $\pm20V$	114	132		114	132		dB
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	±13	±14		±13	±14		V
	Slew Rate	C_f = 30pF	0.1	0.2		0.1	0.2		V/μsec
I_S	Supply Current	Note 2		380	600		380	600	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$ for the LT1008C and $-55°C \leq T_A \leq 125°C$ for the LT1008M, unless otherwise noted.

				LT1008M			LT1008C			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		50	250		40	180	μV
		Note 2	●		60	320		50	250	μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.2	1.5		0.2	1.5	μV/°C
I_{OS}	Input Offset Current		●		60	250		40	180	pA
		Note 2	●		80	350		50	250	pA
	Average Temperature Coefficient of Input Offset Current		●		0.4	2.5		0.4	2.5	pA/°C
I_B	Input Bias Current		●		±80	±600		±40	±180	pA
		Note 2	●		±150	±800		±50	±250	pA
	Average Temperature Coefficient of Input Bias Current		●		0.6	6.0		0.4	2.5	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	●	100	1000		150	1500		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128		110	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	●	108	126		110	128		dB
	Input Voltage Range		●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±14		±13	±14		V
I_S	Supply Current		●		400	800		400	800	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistors are used.

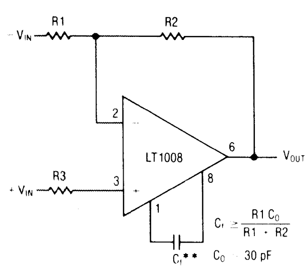
Note 2: These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ ($\pm 2.5V \leq V_S \leq \pm 20V$ over the temperature range) and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$).

Note 3: 10Hz noise voltage density is sample tested on every lot.

Note 4: This parameter is tested on a sample basis only.

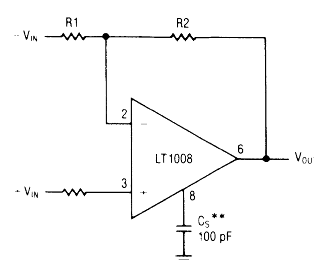
FREQUENCY COMPENSATION CIRCUITS

Standard Compensation Circuit



** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO 1/C_f

Alternate* Frequency Compensation



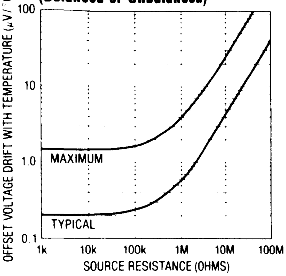
* IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF 5

** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO 1/C_S

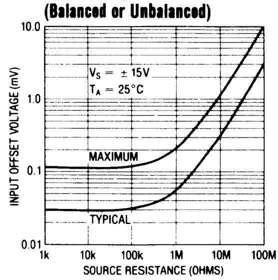
FOR $\frac{R2}{R1} > 200$ NO EXTERNAL FREQUENCY COMPENSATION IS NECESSARY

TYPICAL PERFORMANCE CHARACTERISTICS

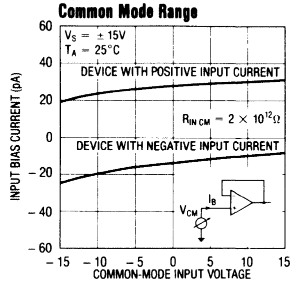
Offset Voltage Drift vs Source Resistance (Balanced or Unbalanced)



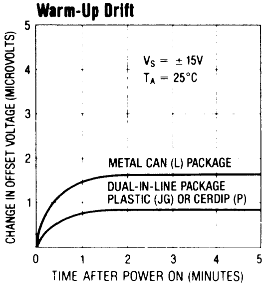
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



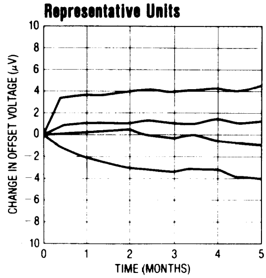
Input Bias Current Over Common Mode Range



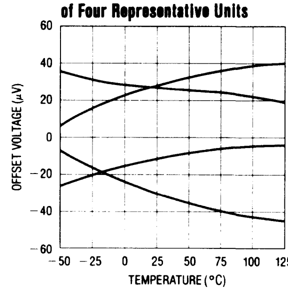
Warm-Up Drift



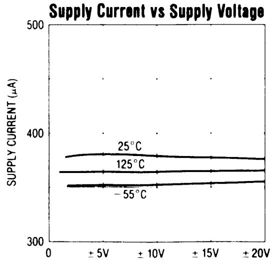
Long Term Stability of Four Representative Units



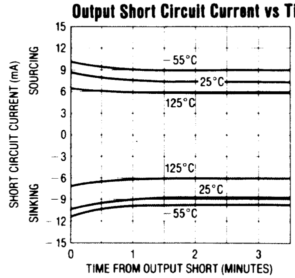
Offset Voltage Drift with Temperature of Four Representative Units



Supply Current vs Supply Voltage

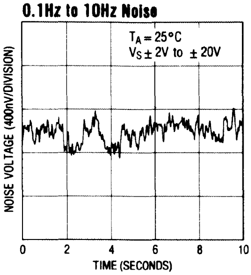


Output Short Circuit Current vs Time

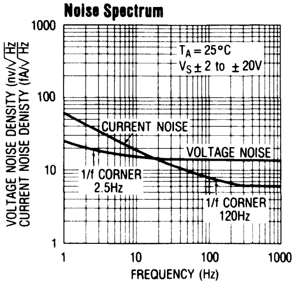


TYPICAL PERFORMANCE CHARACTERISTICS

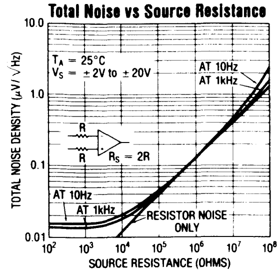
0.1Hz to 10Hz Noise



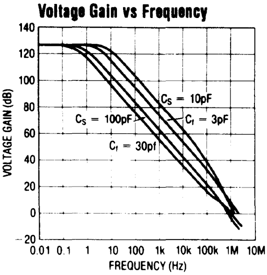
Noise Spectrum



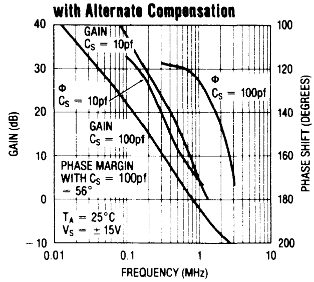
Total Noise vs Source Resistance



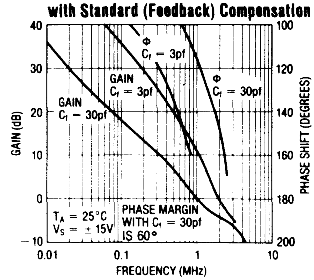
Voltage Gain vs Frequency



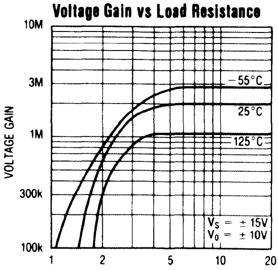
Gain, Phase Shift vs Frequency with Alternate Compensation



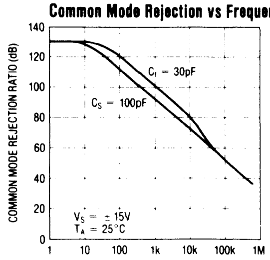
Gain, Phase Shift vs Frequency with Standard (Feedback) Compensation



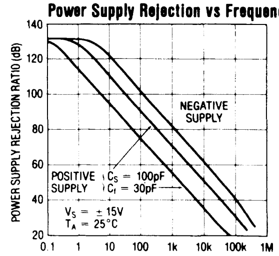
Voltage Gain vs Load Resistance



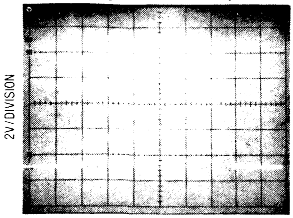
Common Mode Rejection vs Frequency



Power Supply Rejection vs Frequency

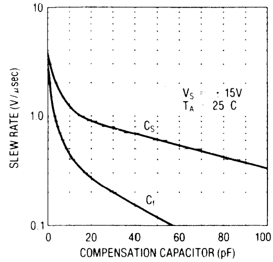


Large Signal Transient Response

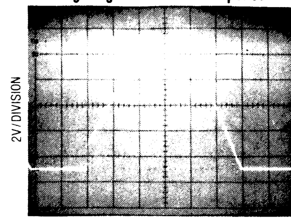


A_V = +1, C_S = 100pF, 20µsec/DIV

Slew Rate vs Compensation Capacitance

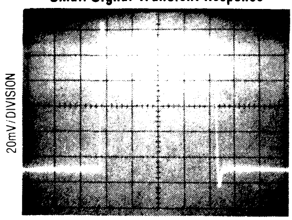


Large Signal Transient Response



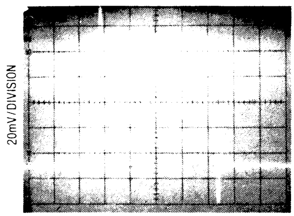
A_V = +1, C_f = 30pF, 20µsec/DIV

Small Signal Transient Response



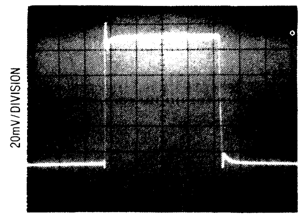
A_V = +1, C_S = 100pF, C_{LOAD} = 100pF, 5µsec/DIV

Small Signal Transient Response



A_V = +1, C_S = 100pF, C_{LOAD} = 600pF, 5µsec/DIV

Small Signal Transient Response



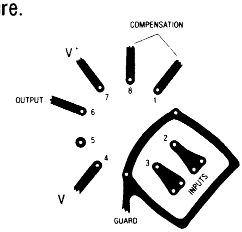
A_V = +1, C_f = 30pF, C_{LOAD} = 100pF, 5µsec/DIV

APPLICATIONS INFORMATION

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere — microvolt level accuracy of the LT1008, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the compensation terminals can affect offset voltage and drift with temperature.

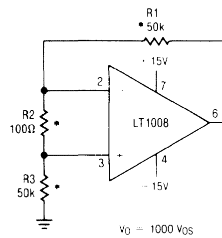


APPLICATIONS INFORMATION

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

The LT1008 is specified over a wide range of power-supply voltages from ±2V to ±18V. Operation with lower supplies is possible down to ±1.0V (two Ni-Cad batteries).

Test Circuit for Offset Voltage and its Drift with Temperature



* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL

** THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1008, WITH SUPPLY VOLTAGES INCREASED TO ±20V, R1 = R3 = 20k, R2 = 200Ω, A_V = 100

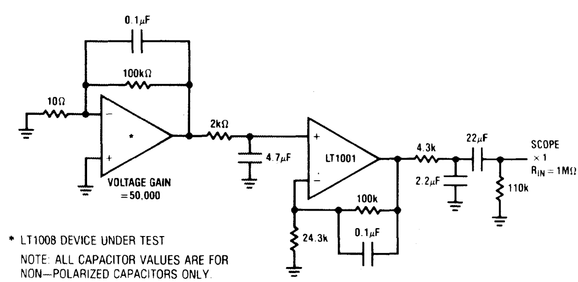
Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1008 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

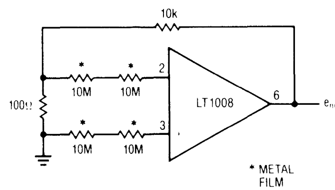
A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured in the circuit shown and calculated by the following formula where the noise of the source resistors is subtracted.

0.1Hz to 10Hz Noise Test Circuit



$$i_n = \frac{[e^2_{no} - (820nV)^2]^{1/2}}{40M\Omega \times 100}$$



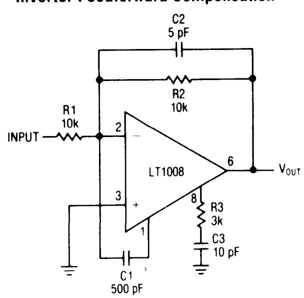
APPLICATIONS INFORMATION

Frequency Compensation

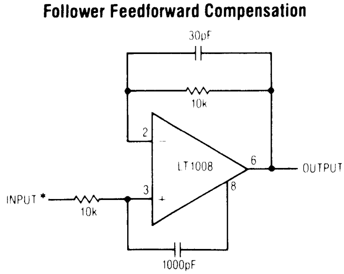
The LT1008 is externally frequency compensated with a single capacitor. The two standard compensation circuits shown on page 3 are identical to the LM108A/308A frequency compensation schemes. Therefore, the LT1008 operational amplifiers can be inserted directly into LM108A/308A sockets, with similar AC and upgraded DC performance.

External frequency compensation provides the user with additional flexibility in shaping the frequency response of the amplifier. For example, for a voltage gain of ten, and $C_f = 3pF$, a gain bandwidth product of 5MHz and slew rate of 1.2V/μsec can be realized. For closed loop gains in excess of 200, no external compensation is necessary, and slew rate increases to 4V/μsec. The LT1008 can also be overcompensated (i.e. $C_f > 30pF$ or $C_S > 100pF$) to improve capacitive load handling capability or to narrow noise bandwidth. In many applications, the feedback loop around the amplifier has gain (e.g. logarithmic amplifiers); overcompensation can stabilize these circuits with a single capacitor.

Inverter Feedforward Compensation



Follower Feedforward Compensation

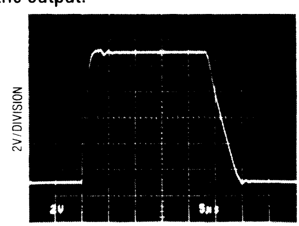


* SOURCE RESISTANCE - 15k FOR STABILITY

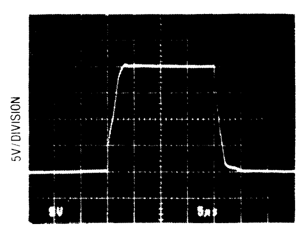
The availability of the compensation terminals permits the use of feedforward frequency compensation to enhance slew rate in low closed loop gain configurations. The inverter slew rate is increased to 1.4V/μsec. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly 10V/μsec.

The inputs of the LT1008 are protected with back-to-back diodes. Current limiting resistors are not used, because the leakage of these resistors would prevent the realization of picoampere level bias currents at elevated temperatures. In the voltage follower configuration, when the input is driven by a fast, large signal pulse (> 1V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short circuit protection will flow through the diodes.

The use of a feedback resistor, as shown in the voltage follower, feedforward diagram, is recommended because this resistor keeps the current below the short circuit limit, resulting in faster recovery and settling of the output.



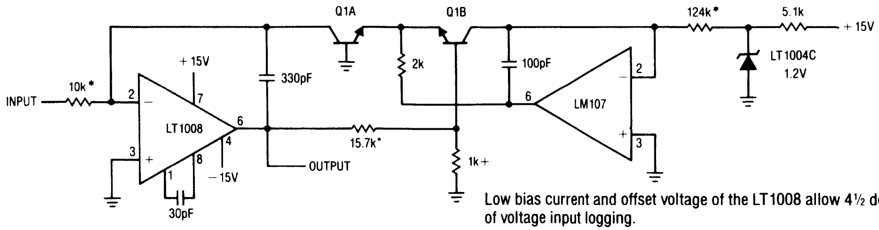
5μsec/DIVISION



5μsec/DIVISION

APPLICATIONS

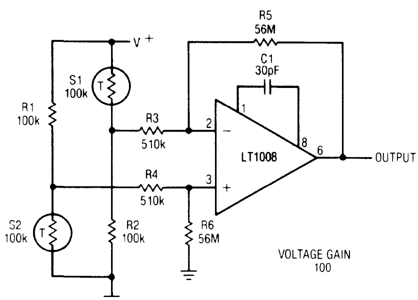
Logarithmic Amplifier



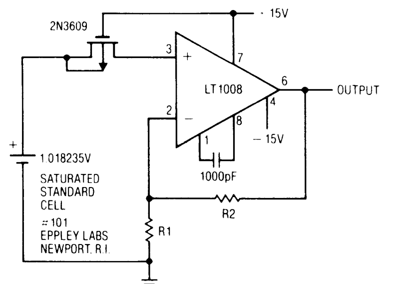
Low bias current and offset voltage of the LT1008 allow 4½ decades of voltage input logging.

+ = TEL. LABS, TYPE Q81
* = 1% FILM RESISTOR
Q1 = 2N2979

Amplifier for Bridge Transducers

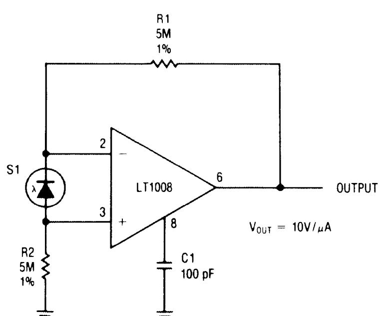


Saturated Standard Cell Amplifier

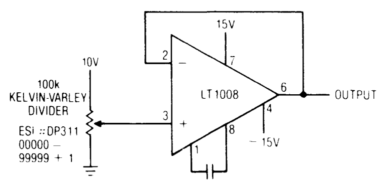


The typical 30pA bias current of the LT1008 will degrade the standard cell by only 1 ppm/year. Noise is a fraction of a ppm. Unprotected gate MOSFET isolates standard cell on power down.

Amplifier For Photodiode Sensor



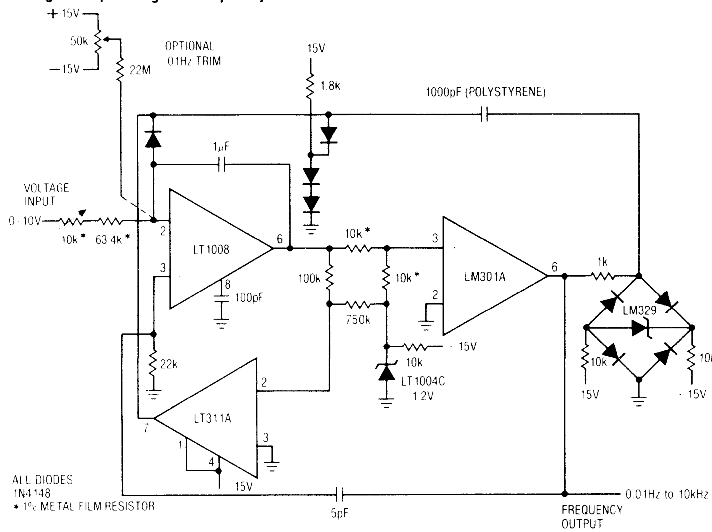
Five Decade Kelvin-Varley Divider Buffered by the LT1008



Approximate error due to noise, bias current, common-mode rejection, voltage gain of the amplifier is 1/5 of a least significant bit.

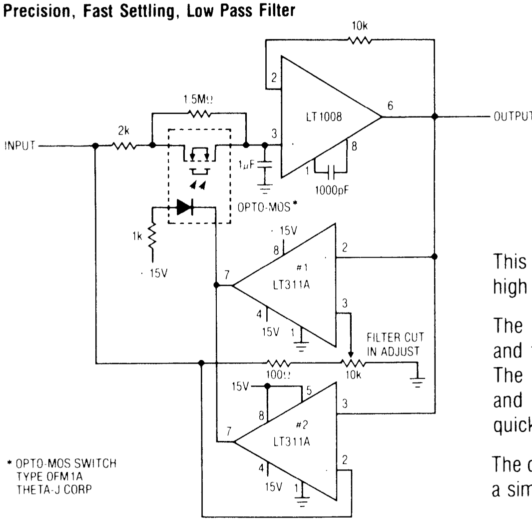
3 Operational Amplifiers

Extended Range Charge Pump Voltage to Frequency Converter



The LT1008 integrator extends low frequency range. Total dynamic range is 0.01Hz to 10kHz (or 120dB) with 0.01% linearity.

Precision, Fast Settling, Low Pass Filter

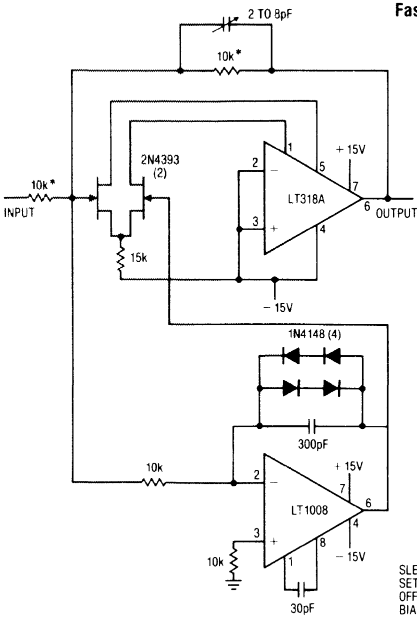


This circuit is useful where fast signal acquisition and high precision are required, as in electronic scales.

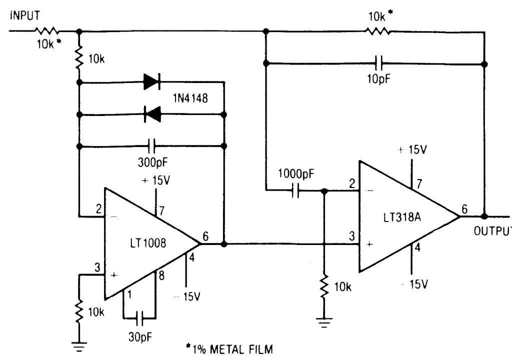
The filter's time constant is set by the 2KΩ resistor and the 1μF capacitor until comparator #1 switches. The time constant is then set by the 1.5MΩ resistor and the 1μF capacitor. Comparator #2 provides a quick reset.

The circuit settles to a final value three times as fast as a simple 1.5MΩ — 1μF filter, with almost no DC error.

Fast Precision Inverters

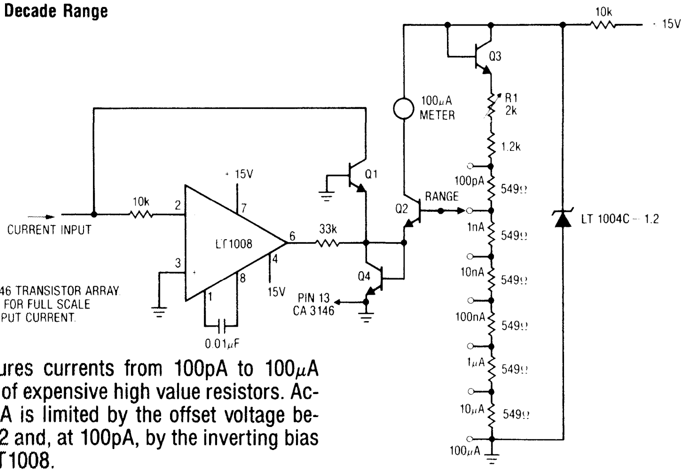


SLEW RATE ≥ 100V/µS
SETTLING = 5µS TO .01%/10 VOLT STEP
OFFSET VOLTAGE = 30µV
BIAS CURRENT = 30pA
* 1% METAL FILM



FULL POWER BANDWIDTH = 2MHz
SLEW RATE = 50V/µsec
SETTLING (10V STEP) = 12µS TO 0.01%
BIAS CURRENT DC = 30pA
OFFSET DRIFT = 0.3µV/°C
OFFSET VOLTAGE = 30µV

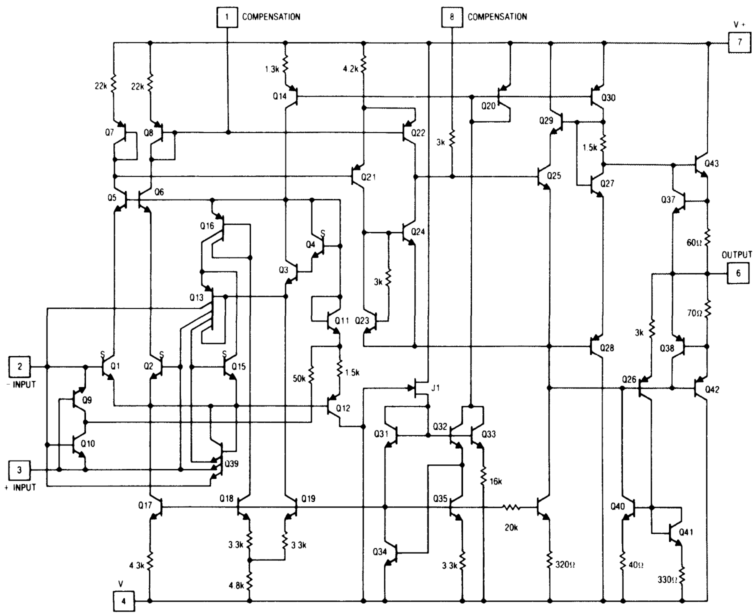
Ammeter With Six Decade Range



Q1, Q2, Q3, Q4, RCA CA3146 TRANSISTOR ARRAY.
CALIBRATION: ADJUST R1 FOR FULL SCALE
DEFLECTION WITH 1µA INPUT CURRENT.

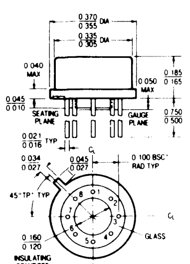
Ammeter measures currents from 100pA to 100µA without the use of expensive high value resistors. Accuracy at 100µA is limited by the offset voltage between Q1 and Q2 and, at 100pA, by the inverting bias current of the LT1008.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

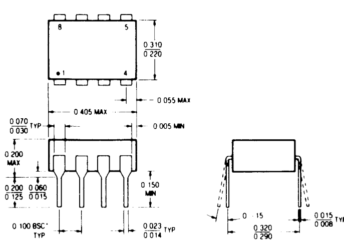
L Package
Metal Can



NOTE DIMENSIONS IN INCHES

$T_j$max	Θ_{ja}	Θ_{jc}
150°C	150°C/W	45°C/W

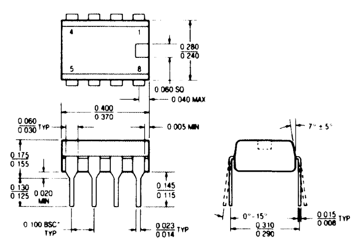
JG Package
8 Lead Hermetic Dip



NOTE DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
150°C	100°C/W

P Package
8 Lead Plastic



NOTE DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_j$max	Θ_{ja}
100°C	130°C/W

TEXAS INSTRUMENTS

PICOAMP INPUT CURRENT, MICROVOLT OFFSET LOW NOISE OP AMP

JULY 1988

FEATURES

- Internally Compensated
- Offset Voltage 35μV max.
- Bias Current
  - 25°C 100pA max.
  - −55°C to 125°C 600pA max.
- Drift 1.5μV/°C max.
- Low Noise, 0.1Hz to 10Hz 0.5μVp-p
- Low Supply Current 600μA max.
- CMRR 114 dB min.
- PSRR 114 db min.
- Voltage Gain with 5mA load current

APPLICATIONS

- Precision instrumentation
- Charge integrators
- Wide dynamic range logarithmic amplifiers
- Light meters
- Low frequency active filters
- Standard cell buffers
- Thermocouple amplifiers

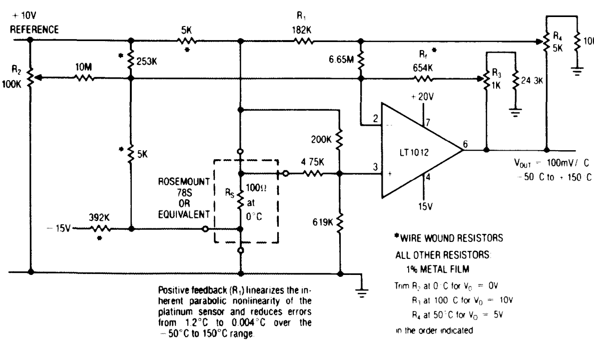
DESCRIPTION

The LT1012 is an internally compensated universal precision operational amplifier which can be used in practically all precision applications. The LT1012 combines picoampere bias currents (which are maintained over the full −55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically unmeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1012's superb precision specifications.

The all around excellence of the LT1012 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1012 can be stocked as the universal internally compensated precision op amp.

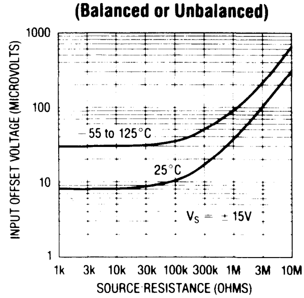
For an externally compensated version with additional flexibility in shaping the frequency response of the amplifier, but otherwise similar performance, see the LT1008.

Kelvin-Sensed Platinum Temperature Sensor Amplifier



Positive feedback (R1) linearizes the inherent parabolic nonlinearity of the platinum sensor and reduces errors from 1.2°C to 0.004°C over the −50°C to 150°C range

Offset Voltage vs Source Resistance (Balanced or Unbalanced)



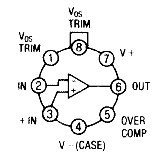
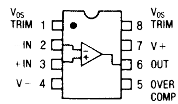
ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

TEXAS INSTRUMENTS

ABSOLUTE MAXIMUM RATING

Supply Voltage .... ±20V
Differential Input Current (Note 1) .... ±10mA
Input Voltage .... ±20V
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
  LT1012M .... −55°C to 125°C
  LT1012C .... 0°C to 70°C
Storage Temperature Range
  All Devices .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ...... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NO.
TOP VIEW  METAL CAN L PACKAGE	LT1012ML LT1012CL
TOP VIEW  PLASTIC DIP P PACKAGE	LT1012CP

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012M MIN	LT1012M TYP	LT1012M MAX	LT1012C MIN	LT1012C TYP	LT1012C MAX	UNITS
V_{OS}	Input Offset Voltage			8	35		10	50	μV
		Note 2		20	90		25	120	μV
	Long Term Input Offset Voltage Stability			0.3			0.3		μV/month
I_{OS}	Input Offset Current			15	100		20	150	pA
		Note 2		25	150		30	200	pA
I_B	Input Bias Current			±25	±100		±30	±150	pA
		Note 2		±35	±150		±40	±200	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
e_n	Input Noise Voltage Density	f_0 = 10Hz (Note 3)		17	30		17	30	nV/√Hz
		f_0 = 1000Hz (Note 4)		14	22		14	22	nV/√Hz
i_n	Input Noise Current Density	f_0 = 10Hz		20			20		fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L \geq 10k\Omega$	300	2000		200	2000		V/mV
		$V_{OUT} = \pm10V$, $R_L \geq 2k\Omega$	200	1000		120	1000		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm13.5V$	114	132		110	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2V$ to $\pm20V$	114	132		110	132		dB
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	±13	±14		±13	±14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/μsec
I_S	Supply Current	Note 2		380	600		380	600	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$ for the LT1012C and $-55°C \leq T_A \leq 125°C$ for the LT1012M, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1012M MIN	LT1012M TYP	LT1012M MAX	LT1012C MIN	LT1012C TYP	LT1012C MAX	UNITS
V_{OS}	Input Offset Voltage		●		30	180		20	120	μV
		Note 2	●		40	250		30	200	μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.2	1.5		0.2	1.5	μV/°C
I_{OS}	Input Offset Current		●		30	250		20	230	pA
		Note 2	●		70	350		40	300	pA
	Average Temperature Coefficient of Input Offset Current		●		0.3	2.5		0.3	2.5	pA/°C
I_B	Input Bias Current		●		±80	±600		±35	±230	pA
		Note 2	●		±150	±800		±50	±300	pA
	Average Temperature Coefficient of Input Bias Current		●		0.6	6.0		0.3	2.5	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	●	150	1000		150	1500		V/mV
		$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	100	600		100	800		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128		108	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	●	108	126		108	128		dB
	Input Voltage Range		●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±14		±13	±14		V
I_S	Supply Current		●		400	800		400	800	μA

The ● denotes the specifications which apply over the full operating temperature range.

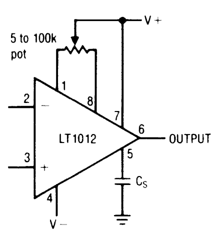
Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ ($\pm 2.5V \leq V_S \leq \pm 20V$ over the temperature range) and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$).

Note 3: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 4: This parameter is tested on a sample basis only.

Optional Offset Nulling and Over-Compensation Circuits

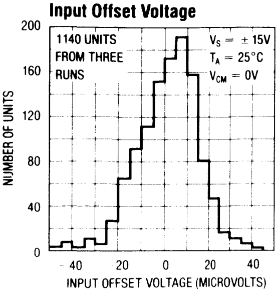


Input offset voltage can be adjusted over a ±800μV range with a 5k to 100k potentiometer.

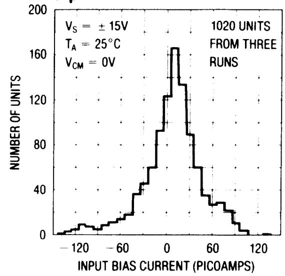
The LT1012 is internally compensated for unity gain stability. The over-compensation capacitor, C_S, can be used to improve capacitive load handling capability, to narrow noise bandwidth, or to stabilize circuits with gain in the feedback loop.

TYPICAL PERFORMANCE CHARACTERISTICS

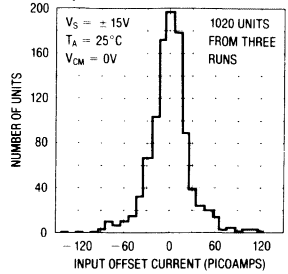
Typical Distribution of Input Offset Voltage



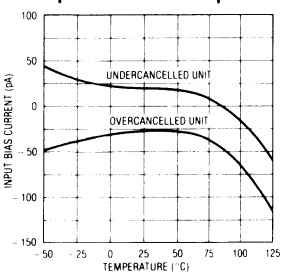
Typical Distribution of Input Bias Current



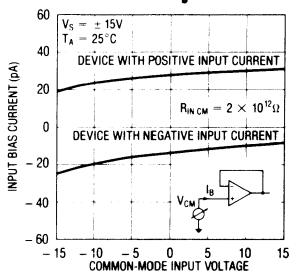
Typical Distribution of Input Offset Current



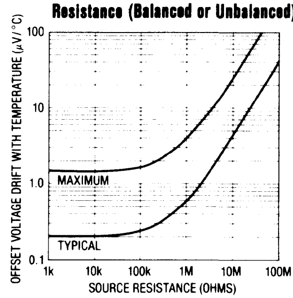
Input Bias Current vs Temperature



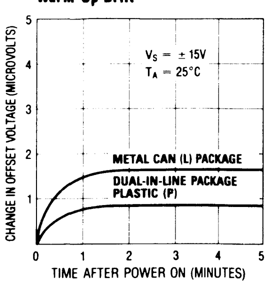
Input Bias Current Over Common Mode Range



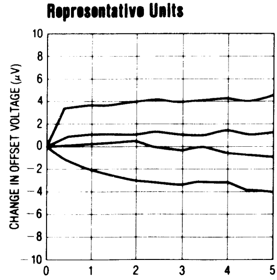
Offset Voltage Drift vs Source Resistance (Balanced or Unbalanced)



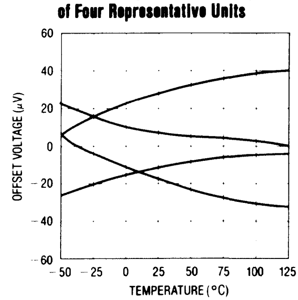
Warm-Up Drift



Long Term Stability of Four Representative Units

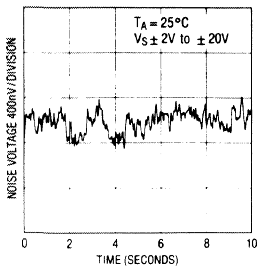


Offset Voltage Drift with Temperature of Four Representative Units

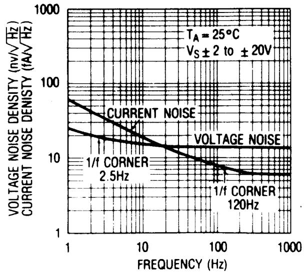


TYPICAL PERFORMANCE CHARACTERISTICS

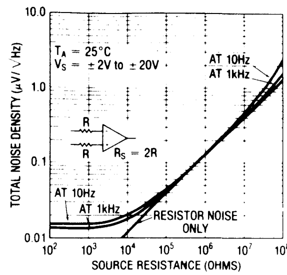
0.1Hz to 10Hz Noise



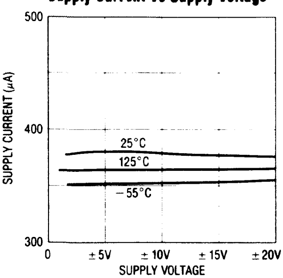
Noise Spectrum



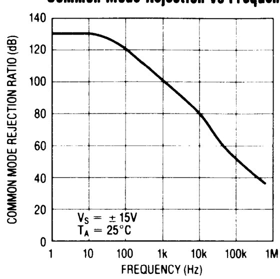
Total Noise vs Source Resistance



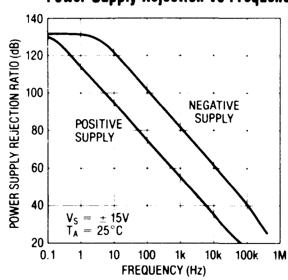
Supply Current vs Supply Voltage



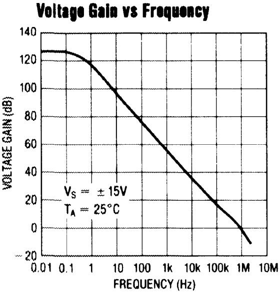
Common Mode Rejection vs Frequency



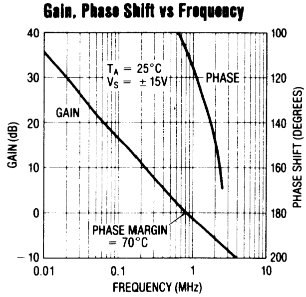
Power Supply Rejection vs Frequency



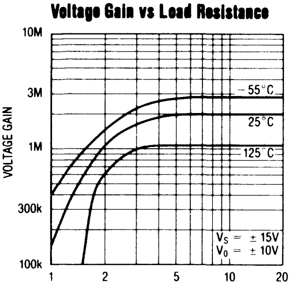
Voltage Gain vs Frequency



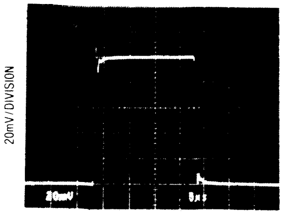
Gain, Phase Shift vs Frequency



Voltage Gain vs Load Resistance

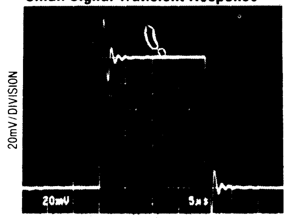


Small Signal Transient Response



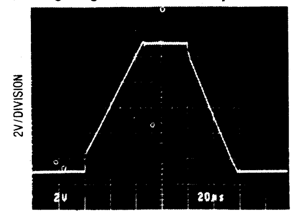
$A_V = +1$, $C_{LOAD} = 100pF$, 5μsec/DIV

Small Signal Transient Response



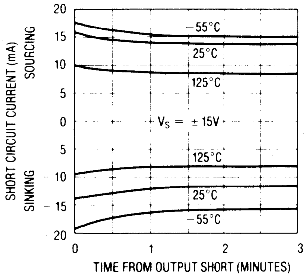
$A_V = +1$, $C_{LOAD} = 1000pF$, 5μsec/DIV

Large Signal Transient Response

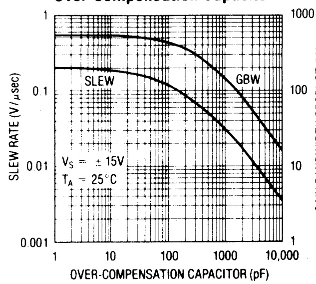


$A_V = +1$, 20μsec/DIV

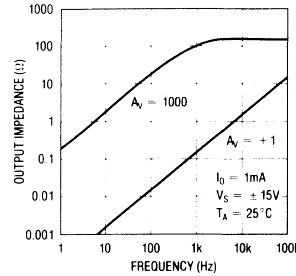
Output Short Circuit Current vs Time



Slew Rate, Gain Bandwidth Product vs Over-Compensation Capacitor



Closed Loop Output Impedance



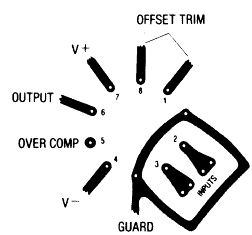
APPLICATIONS INFORMATION

The LT1012 may be inserted directly into OP-07, LM11, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1012 can also be used in 741, LF411, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1012 is specified over a wide range of power supply voltages from ±2V to ±18V. Operation with lower supplies is possible down to ±1.0V (two Ni-Cad batteries).

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere — microvolt level accuracy of the LT1012, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.



APPLICATIONS INFORMATION

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Noise Testing

For application information on noise testing and calculations, please see the LT1008 data sheet.

Frequency Compensation

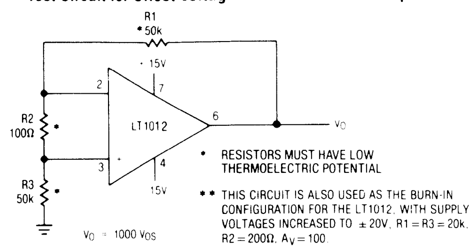
The LT1012 can be overcompensated to improve capacitive load handling capability or to narrow noise bandwidth. In many applications, the feedback loop around the amplifier has gain (e.g. logarithmic amplifiers); overcompensation can stabilize these circuits with a single capacitor.

The availability of the compensation terminal permits the use of feedforward frequency compensation to enhance slew rate. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly 10V/μsec.

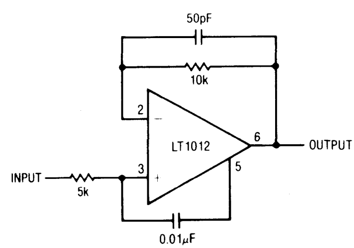
The inputs of the LT1012 are protected with back-to-back diodes. Current limiting resistors are not used, because the leakage of these resistors would prevent the realization of picoampere level bias currents at elevated temperatures. In the voltage follower configuration, when the input is driven by a fast, large signal pulse (> 1V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short circuit protection will flow through the diodes.

The use of a feedback resistor, as shown in the voltage follower feedforward diagram, is recommended because this resistor keeps the current below the short circuit limit, resulting in faster recovery and settling of the output.

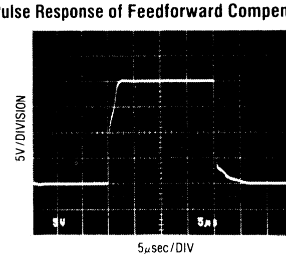
Test Circuit for Offset Voltage and its Drift with Temperature



Follower Feedforward Compensation

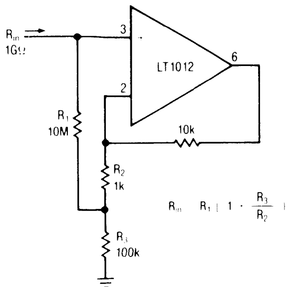


Pulse Response of Feedforward Compensation



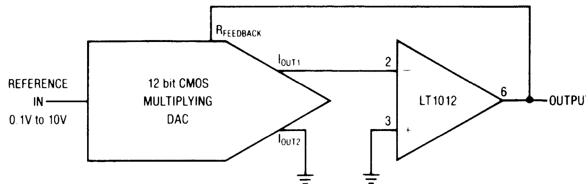
TYPICAL APPLICATIONS

Resistor Multiplier



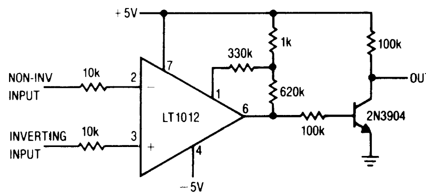
$R_{in} = R_1\left(1 + \frac{R_3}{R_2}\right)$

"No Trims" 12 bit Multiplying DAC Output Amplifier

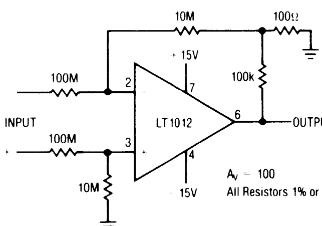


When the reference input drops to 0.1V, the least significant bit decreases to the microvolt/picoampere range.

Low Power Comparator with <10μV Hysteresis

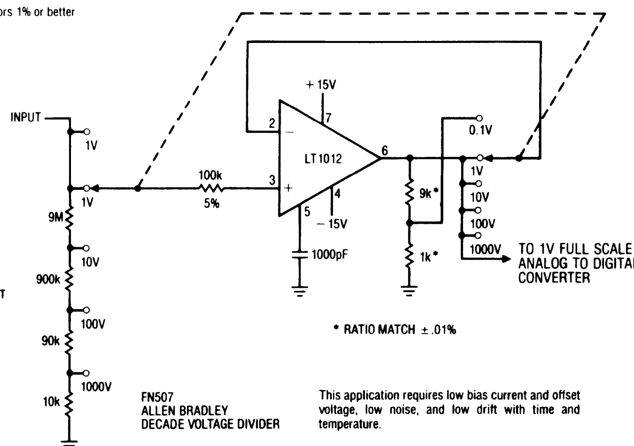


Instrumentation Amplifier with ±100 Volt Common Mode Range



$A_V = 100$
All Resistors 1% or better

Input Amplifier for 4½ Digit Voltmeter

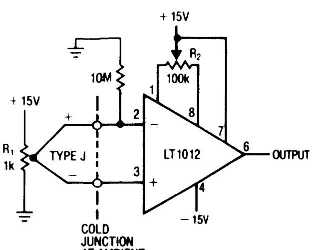


* RATIO MATCH ±.01%

FN507
ALLEN BRADLEY
DECADE VOLTAGE DIVIDER

This application requires low bias current and offset voltage, low noise, and low drift with time and temperature.

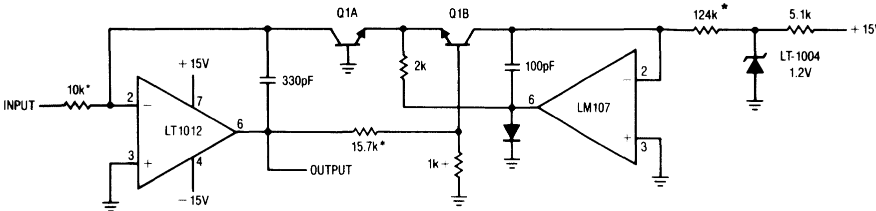
Air Flow Detector



Mount R_1 in airflow.
Adjust R_2 so output goes high when airflow stops.

TYPICAL APPLICATIONS

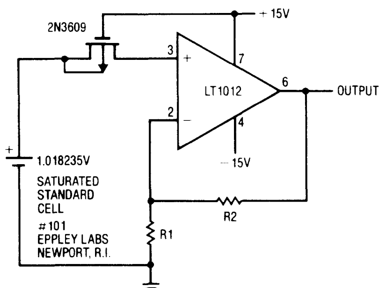
Logarithmic Amplifier



+ = TEL. LABS, TYPE Q81
* = 1% FILM RESISTOR
Q1 = 2N2979

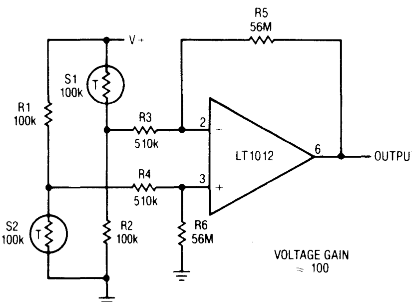
Low bias current and offset voltage of the LT1012 allow 4½ decades of voltage input logging.

Saturated Standard Cell Amplifier

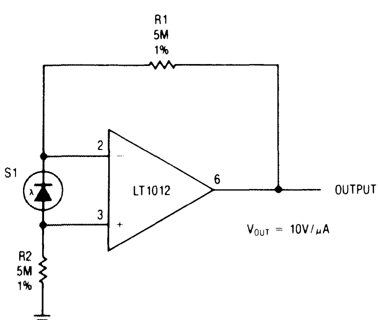


The typical 30pA bias current of the LT1012 will degrade the standard cell by only 1 ppm/year. Noise is a fraction of a ppm. Unprotected gate MOSFET isolates standard cell on power down.

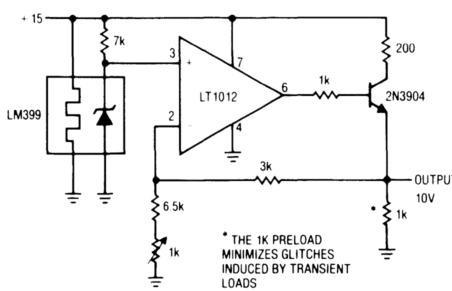
Amplifier for Bridge Transducers



Amplifier For Photodiode Sensor

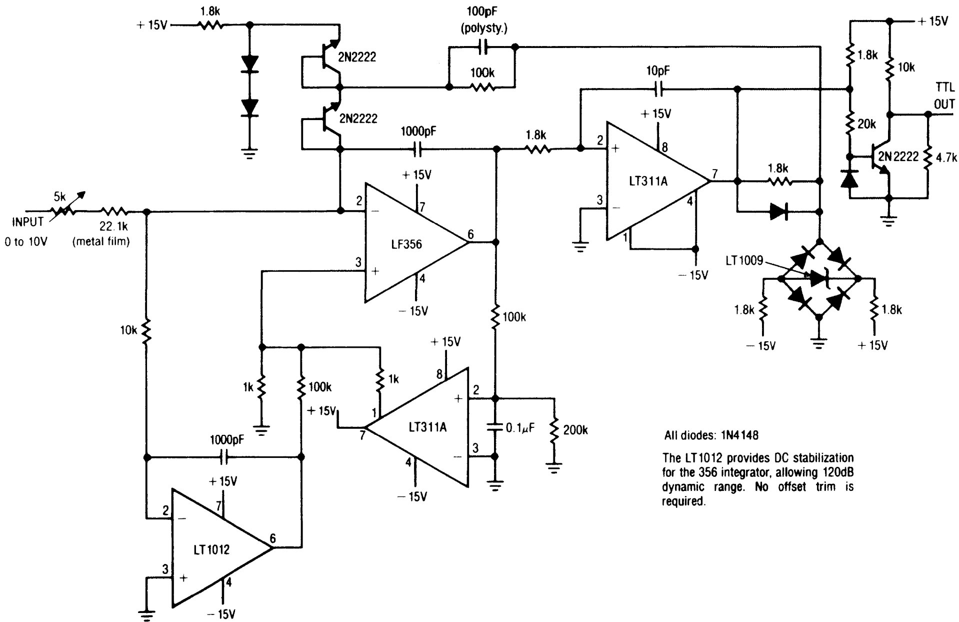


Buffered Reference for A to D Converters



TYPICAL APPLICATIONS

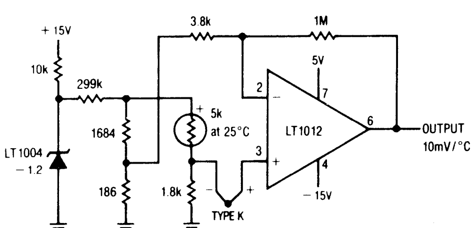
1Hz to 1MHz Voltage to Frequency Converter



All diodes: 1N4148

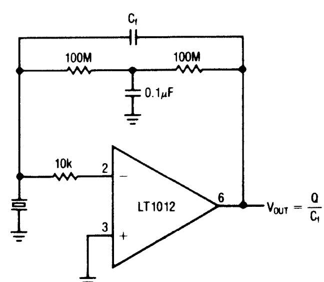
The LT1012 provides DC stabilization for the 356 integrator, allowing 120dB dynamic range. No offset trim is required.

Thermocouple Thermometer

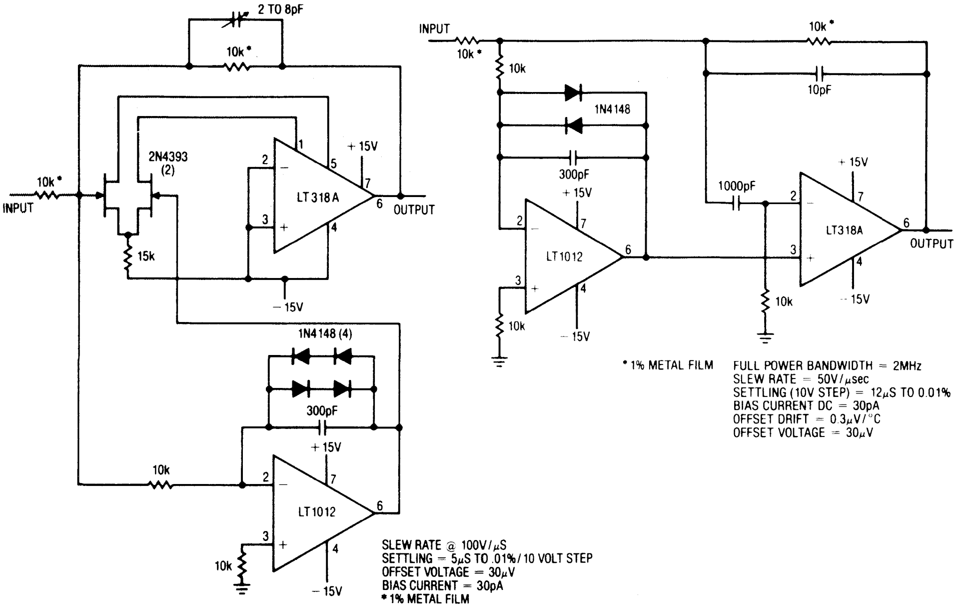


+ YSI #44007
COLD JUNCTION
COMPENSATION ± 1°C
OVER 0 to 60°C

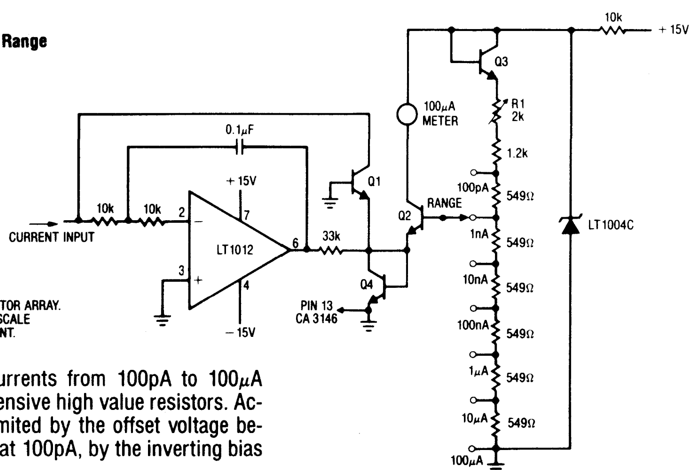
Charge Amplifier for Piezoelectric Transducers



Fast Precision Inverters



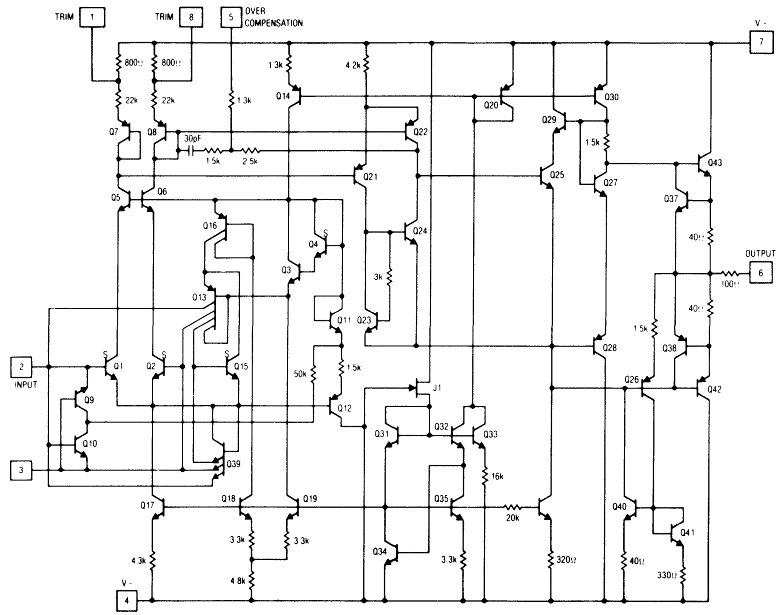
Ammeter With Six Decade Range



Q1, Q2, Q3, Q4, RCA CA3146 TRANSISTOR ARRAY.
CALIBRATION: ADJUST R1 FOR FULL SCALE DEFLECTION WITH 1μA INPUT CURRENT.

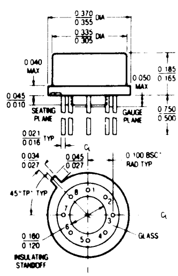
Ammeter measures currents from 100pA to 100μA without the use of expensive high value resistors. Accuracy at 100μA is limited by the offset voltage between Q1 and Q2 and, at 100pA, by the inverting bias current of the LT1012.

SCHEMATIC DIAGRAM



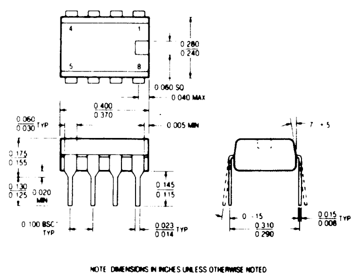
PACKAGE DESCRIPTION

L Package
Metal Can



$T_j$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

P Package
8 Lead Plastic



$T_j$max	θ_{ja}
100°C	130°C/W

MAY 1988

FEATURES

- Single Supply Operation
  - Input Voltage Range Extends to Ground
  - Output Swings to Ground while Sinking Current
- Pin Compatible to 1458 and 324 with Precision Specs
- Offset Voltage 150μV Max.
- Low Drift 2μV/°C Max.
- Offset Current 0.8nA Max.
- High Gain
  - 5mA Load Current 1.5 Million Min.
  - 17mA Load Current 0.8 Million Min.
- Low Supply Current 500μA Max.
- Low Voltage Noise, 0.1Hz to 10Hz 0.55μVp-p
- Low Current Noise–Better than OP-07, 0.07 pA/$\sqrt{HZ}$

APPLICATIONS

- Battery-Powered Precision Instrumentation
  - Strain Gauge Signal Conditioners
  - Thermocouple Amplifiers
  - Instrumentation Amplifiers
- 4mA–20mA Current Loop Transmitters
- Multiple Limit Threshold Detection
- Active Filters
- Multiple Gain Blocks

ABSOLUTE MAXIMUM RATINGS

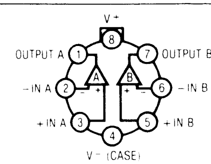
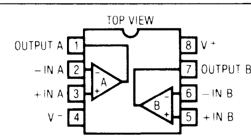
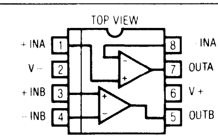
Supply Voltage .... ±22V
Differential Input Voltage .... ±30V
Input Voltage .... Equal to Positive Supply Voltage
...... 5V Below Negative Supply Voltage
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
LT1013AM/LT1013M .... −55°C to 125°C
LT1013AC/1013C/1013D .... 0°C to 70°C
Storage Temperature Range
All Grades .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)........ 300°C

DESCRIPTION

The LT1013 is the first precision dual op amp in the 8-pin industry standard configuration, upgrading the performance of such popular devices as the MC1458/1558, LM158 and OP-221. The LT1013's specifications are similar to (even somewhat better than) the LT1014's.

The LT1013 can be operated off a single 5V power supply: input common-mode range includes ground; the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent on previous single-supply designs, is eliminated. A full set of specifications is provided with ± 15V and single 5V supplies.

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 METAL CAN L PACKAGE	LT1013AML LT1013ML LT1013ACL LT1013CL
 HERMETIC DIP JG PACKAGE PLASTIC DIP P PACKAGE	LT1013AMJG LT1013MJG LT1013ACJG LT1013CJG LT1013CP LT1013DP
 D PACKAGE PLASTIC SO	LT1013DD

The D packages are available taped and reeled. Add the suffix R to the device type when ordering taped parts. (ie. LT1013DDR)

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

TEXAS INSTRUMENTS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM/LT1013AC MIN	TYP	MAX	LT1013M/LT1013C LT1013DP MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1013 LT1013DP	– –	40 –	150 –	– –	60 200	300 800	μV μV
	Long Term Input Offset Voltage Stability		–	0.4	–	–	0.5	–	μV/Mo.
I_{OS}	Input Offset Current		–	0.15	0.8	–	0.2	1.5	nA
I_B	Input Bias Current		–	12	20	–	15	30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	–	0.55	–	–	0.55	–	μVp-p
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1000Hz$	– –	24 22	– –	– –	24 22	– –	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	$f_0 = 10Hz$	–	0.07	–	–	0.07	–	pA/√Hz
	Input Resistance—Differential Common-Mode	(Note 1)	100 –	400 5	– –	70 –	300 4	– –	MΩ GΩ

Note 1: This parameter is not tested. Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1013s, typically 240 op amps (or 120) will be better than the indicated specification.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC MIN	TYP	MAX	LT1013M/LT1013C LT1013DP MIN	TYP	MAX	UNITS
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$ $V_O = \pm 10V$, $R_L = 600\Omega$	1.5 0.8	8.0 2.5	– –	1.2 0.5	7.0 2.0	– –	V/μV V/μV
	Input Voltage Range		+13.5 −15.0	+13.8 −15.3	– –	+13.5 −15.0	+13.8 −15.3	– –	V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V, -15.0V$	100	117	–	97	114	–	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	103	120	–	100	117	–	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$	123	140	–	120	137	–	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±13	±14	–	±12.5	±14	–	V
	Slew Rate		0.2	0.4	–	0.2	0.4	–	V/μs
I_S	Supply Current	Per Amplifier	–	0.35	0.50	–	0.35	0.55	mA

ELECTRICAL CHARACTERISTICS

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{OUT} = 1.4V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC MIN	LT1013AM LT1013AC TYP	LT1013AM LT1013AC MAX	LT1013M/LT1013C LT1013DP MIN	LT1013M/LT1013C LT1013DP TYP	LT1013M/LT1013C LT1013DP MAX	UNITS
V_{OS}	Input Offset Voltage	LT1013 LT1013DP	– –	60 –	250 –	– –	90 250	450 950	μV μV
I_{OS}	Input Offset Current		–	0.2	1.3	–	0.3	2.0	nA
I_B	Input Bias Current		–	15	35	–	18	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 5mV$ to 4V, $R_L = 500\Omega$	–	1.0	–	–	1.0	–	V/μV
	Input Voltage Range		+3.5 0	+3.8 −0.3	– –	+3.5 0	+3.8 −0.3	– –	V V
V_{OUT}	Output Voltage Swing	Output Low, No Load Output Low, 600Ω to Ground Output Low, $I_{SINK} = 1mA$ Output High, No Load Output High, 600Ω to Ground	– – – 4.0 3.4	15 5 220 4.4 4.0	25 10 350 – –	– – – 4.0 3.4	15 5 220 4.4 4.0	25 10 350 – –	mV mV mV V V
I_S	Supply Current	Per Amplifier	–	0.31	0.45	–	0.32	0.50	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $-55°C \leq T_A \leq 125°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1013AM MIN	LT1013AM TYP	LT1013AM MAX	LT1013M MIN	LT1013M TYP	LT1013M MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	80	300	—	110	550	μV
		V_S = +5V, 0V; V_O = +1.4V								
		$-55°C \leq T_A \leq 100°C$	●	—	80	450	—	100	750	μV
		V_{CM} = 0.1V, T_A = 125°C		—	120	450	—	200	750	μV
		V_{CM} = 0V, T_A = 125°C		—	250	900	—	400	1500	μV
	Input Offset Voltage Drift	(Note 2)	●	—	0.4	2.0	—	0.5	2.5	μV/°C
I_{OS}	Input Offset Current		●	—	0.3	2.5	—	0.4	5.0	nA
		V_S = +5V, 0V; V_O = +1.4V	●	—	0.6	6.0	—	0.9	10.0	nA
I_B	Input Bias Current		●	—	15	30	—	18	45	nA
		V_S = +5V, 0V; V_O = +1.4V	●	—	20	80	—	28	120	nA
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 2k	●	0.5	2.0	—	0.25	2.0	—	V/μV
CMRR	Common-Mode Rejection	V_{CM} = +13.0V, −14.9V	●	97	114	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	●	100	117	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	R_L = 2k	●	±12	±13.8	—	±11.5	±13.8	—	V
		V_S = +5V, 0V; R_L = 600Ω to Ground								
		Output Low	●	—	6	15	—	6	18	mV
		Output High	●	3.2	3.8	—	3.1	3.8	—	V
I_S	Supply Current Per Amplifier		●	—	0.38	0.60	—	0.38	0.7	mA
		V_S = +5V, 0V; V_O = +1.4V	●	—	0.34	0.55	—	0.34	0.65	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$ unless otherwise noted

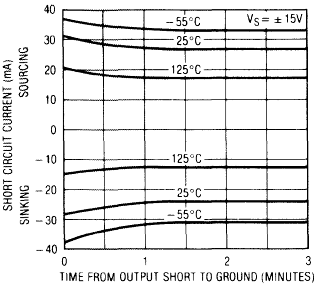
SYMBOL	PARAMETER	CONDITIONS		LT1013AC MIN	LT1013AC TYP	LT1013AC MAX	LT1013C/LT1013DP MIN	LT1013C/LT1013DP TYP	LT1013C/LT1013DP MAX	UNITS
V_{OS}	Input Offset Voltage		●	—	55	240	—	80	400	μV
		LT1013DP	●	—	—	—	—	230	1000	μV
		V_S = +5V, 0V; V_O = 1.4V	●	—	75	350	—	110	570	μV
		LT1013DN8, LT1014DN	●	—	—	—	—	280	1200	μV
	Average Input Offset Voltage Drift	(Note 2)	●	—	0.3	2.0	—	0.4	2.5	μV/°C
		LT1013DN	●	—	—	—	—	0.7	5.0	μV/°C
I_{OS}	Input Offset Current		●	—	0.2	1.5	—	0.3	2.8	nA
		V_S = +5V, 0V, V_O = 1.4V	●	—	0.4	3.5	—	0.5	6.0	nA
I_B	Input Bias Current		●	—	13	25	—	16	38	nA
		V_S = +5V, 0V, V_O = 1.4V	●	—	18	55	—	24	90	nA
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 2k	●	1.0	5.0	—	0.7	4.0	—	V/μV
CMRR	Common-Mode Rejection Ratio	V_{CM} = +13.0V, −15.0V	●	98	116	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±18V	●	101	119	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	R_L = 2k	●	±12.5	±13.9	—	±12.0	±13.9	—	V
		V_S = +5V, 0V, R_L = 600Ω								
		Output Low	●	—	6	13	—	6	13	mV
		Output High	●	3.3	3.9	—	3.2	3.9	—	V
I_S	Supply Current per Amplifier		●	—	0.36	0.55	—	0.37	0.60	mA
		V_S = +5V, 0V, V_O = 1.4V	●	—	0.32	0.50	—	0.34	0.55	mA

Note 2: This parameter is not 100% tested

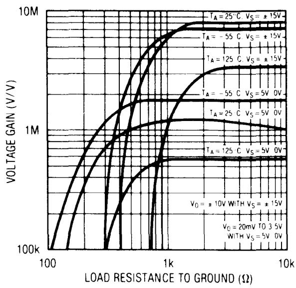
The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

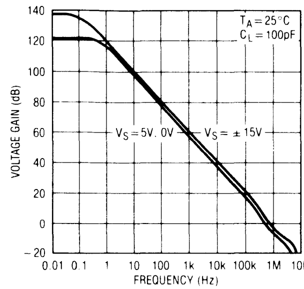
Output Short Circuit Current vs Time



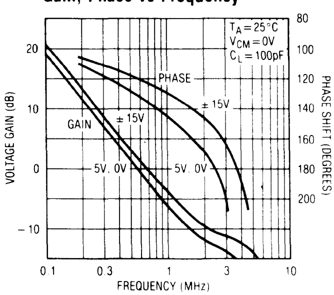
Voltage Gain vs Load Resistance



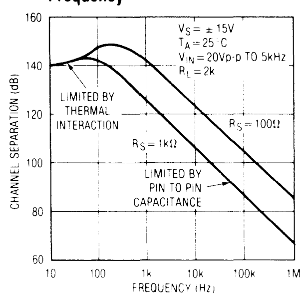
Voltage Gain vs Frequency



Gain, Phase vs Frequency



Channel Separation vs Frequency



APPLICATIONS INFORMATION

Single Supply Operation

The LT1013 is fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1013 has specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

a) when the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1013, the 400Ω resistors, in series with the input (see schematic diagram), protect the devices even when the input is 5V below ground.

APPLICATIONS INFORMATION

b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1013 outputs do not reverse, as illustrated below, even when the inputs are at −1.5V.

There is one circumstance, however, under which the phase reversal protection circuitry does not function: when the other op amp on the LT1013 is driven hard into negative saturation at the output.

Phase reversal protection does not work on amplifier:
A when D's output is in negative saturation. B's and C's outputs have no effect.
B when C's output is in negative saturation. A's and D's outputs have no effect.
C when B's output is in negative saturation. A's and D's outputs have no effect.
D when A's output is in negative saturation. B's and C's outputs have no effect.

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1013's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

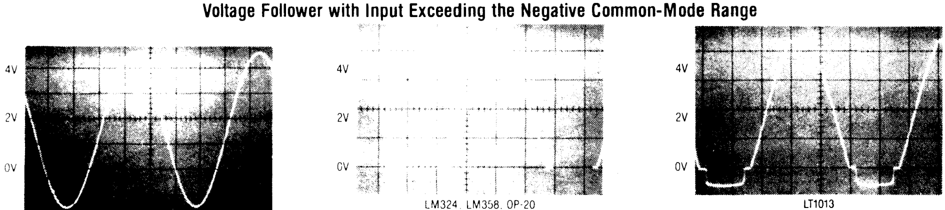
In dual supply operations, the output stage is crossover distortion-free.

Comparator Applications

The single supply operation of the LT1013 lends itself to its use as a precision comparator with TTL compatible output:

In systems using both op amps and comparators, the LT1013 can perform multiple duties.

Voltage Follower with Input Exceeding the Negative Common-Mode Range

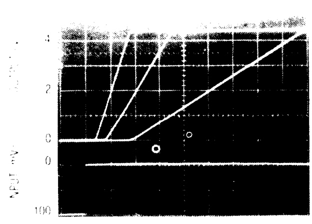


6Vp-p INPUT −1.5V TO 4.5V

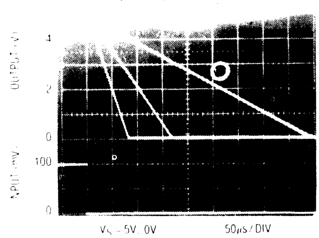
LM324, LM358, OP-20 EXHIBIT OUTPUT PHASE REVERSAL

LT1013 NO PHASE REVERSAL

Comparator Rise Response Time 10mV, 5mV, 2mV Overdrives



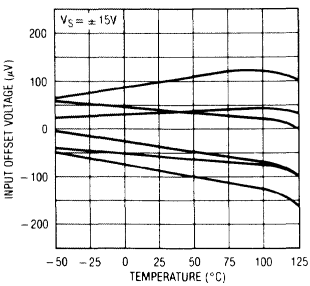
Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



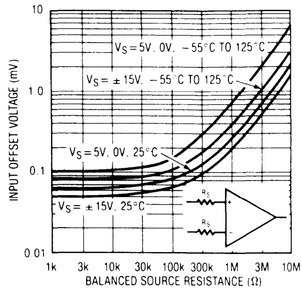
TEXAS INSTRUMENTS

TYPICAL PERFORMANCE CHARACTERISTICS

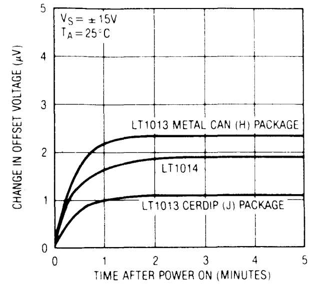
Offset Voltage Drift with Temperature of Representative Units



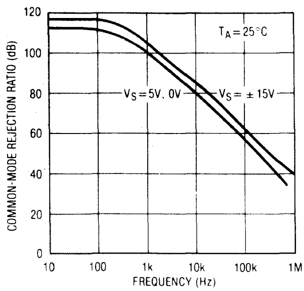
Offset Voltage vs Balanced Source Resistance



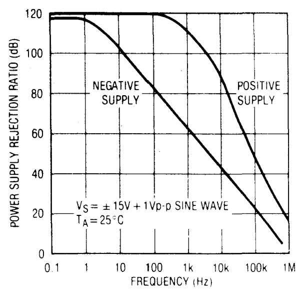
Warm-Up Drift



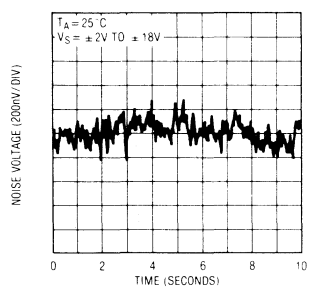
Common-Mode Rejection Ratio vs Frequency



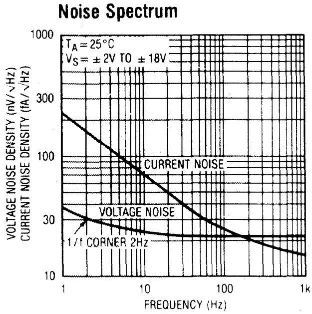
Power Supply Rejection Ratio vs Frequency



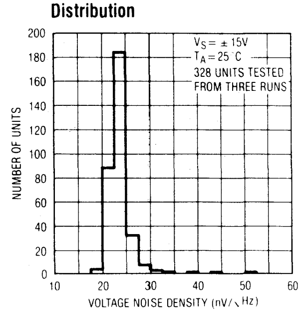
0.1Hz to 10Hz Noise



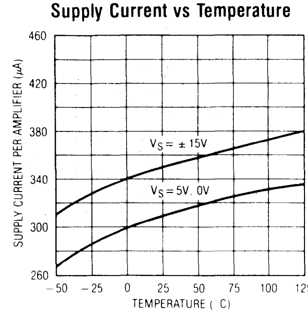
Noise Spectrum



10Hz Voltage Noise Distribution

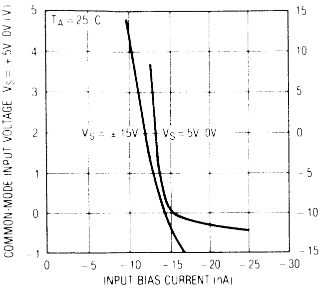


Supply Current vs Temperature

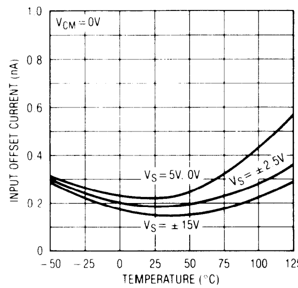


TYPICAL PERFORMANCE CHARACTERISTICS

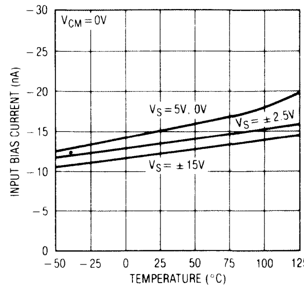
Input Bias Current vs Common-Mode Voltage



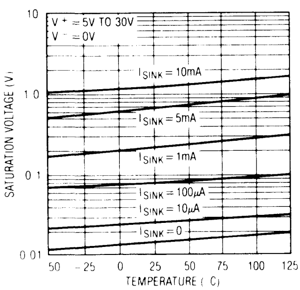
Input Offset Current vs Temperature



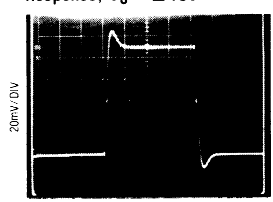
Input Bias Current vs Temperature



Output Saturation vs Sink Current vs Temperature

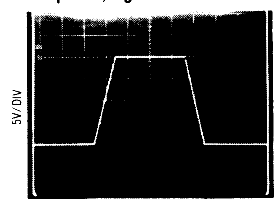


Small Signal Transient Response, $V_S = \pm 15V$



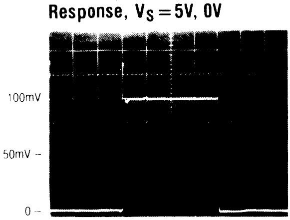
$A_V = +1$ 2μs/DIV

Large Signal Transient Response, $V_S = \pm 15V$



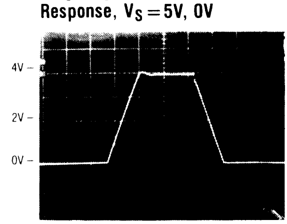
$A_V = +1$ 50μs/DIV

Small Signal Transient Response, $V_S = 5V, 0V$



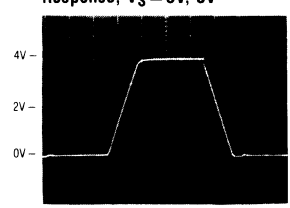
$A_V = +1$ 20μs/DIV
$R_L = 600\Omega$ TO GROUND
INPUT = 0V TO 100mV PULSE

Large Signal Transient Response, $V_S = 5V, 0V$



$A_V = +1$ 10μs/DIV
$R_L = 4.7k$ to 5V
INPUT = 0V TO 4V PULSE

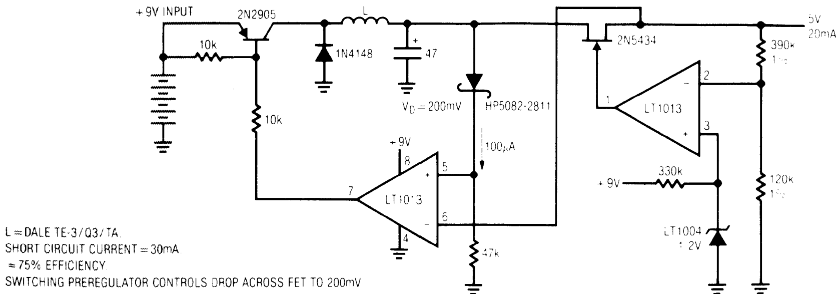
Large Signal Transient Response, $V_S = 5V, 0V$



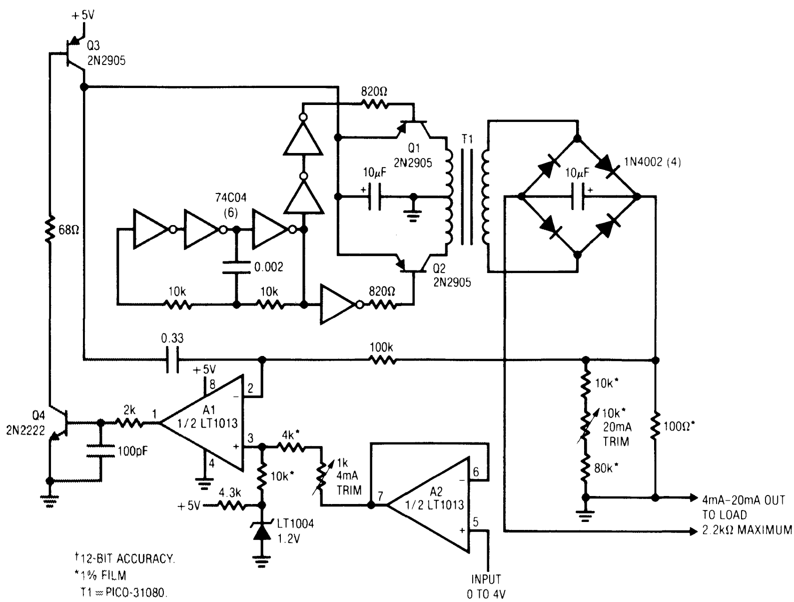
$A_V = +1$ 10μs/DIV
NO LOAD
INPUT = 0V TO 4V PULSE

TYPICAL APPLICATIONS

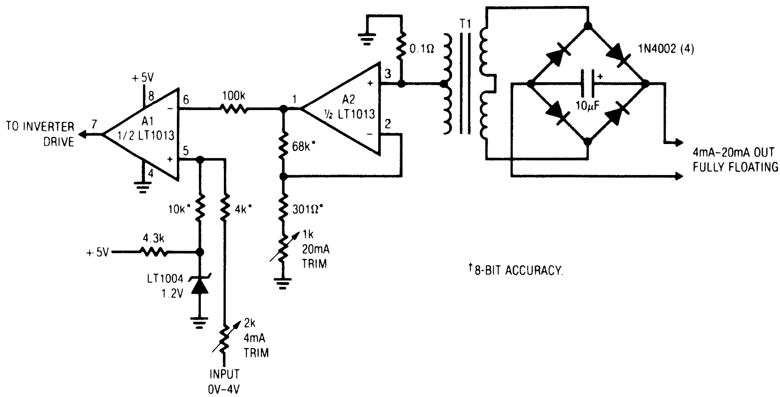
Low Power 9V to 5V Converter



5V Powered 4mA-20mA Current Loop Transmitter †

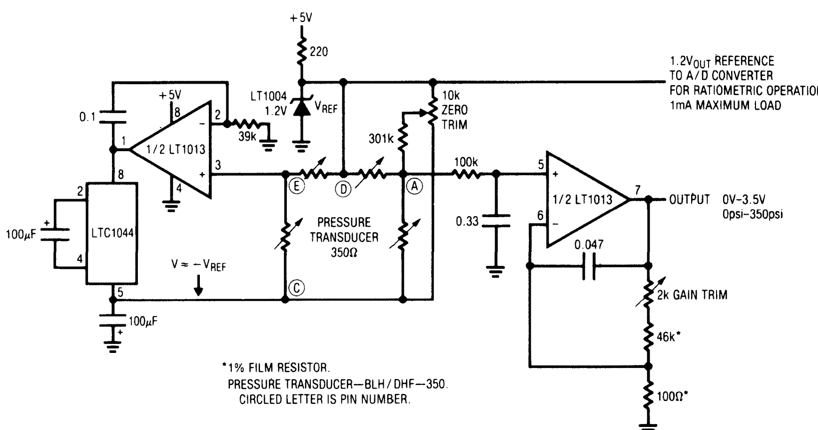


Fully Floating Modification to 4mA-20mA Current Loop†



†8-BIT ACCURACY.

Strain Gage Bridge Signal Conditioner



*1% FILM RESISTOR.
PRESSURE TRANSDUCER—BLH/DHF—350.
CIRCLED LETTER IS PIN NUMBER.

3 Operational Amplifiers

APPLICATIONS INFORMATION

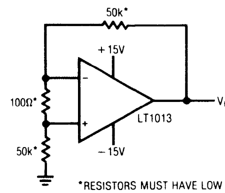
Low Supply Operation

The minimum supply voltage for proper operation of the LT1013 is 3.4V (three Ni-Cad batteries). Typical supply current at this voltage is 290μA, therefore power dissipation is only one milliwatt per amplifier.

Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1008 data sheet.

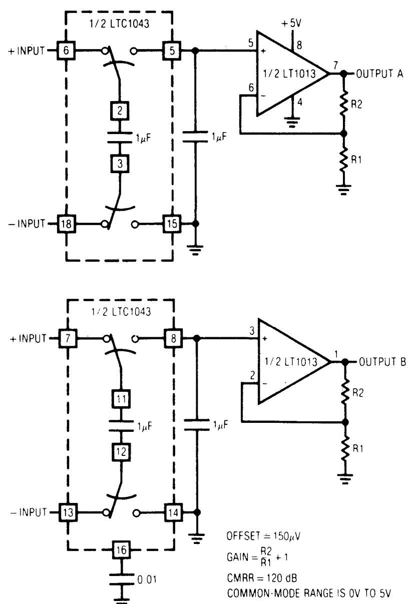
Test Circuit for Offset Voltage and Offset Drift with Temperature



*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.
**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO ±20V.
$V_O = 1000V_{OS}$

TYPICAL APPLICATIONS

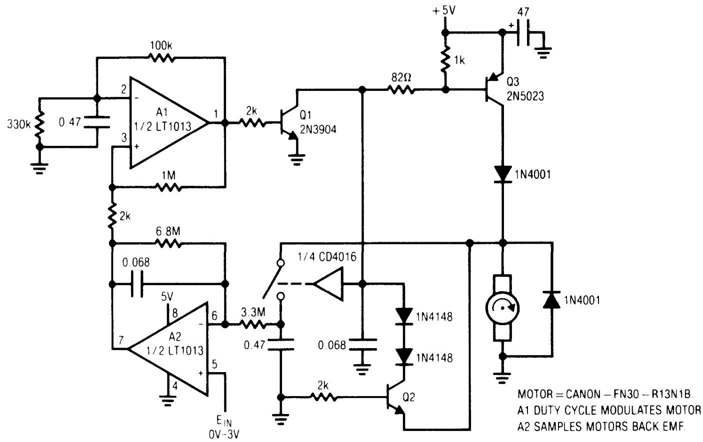
5V Single Supply Dual Instrumentation Amplifier



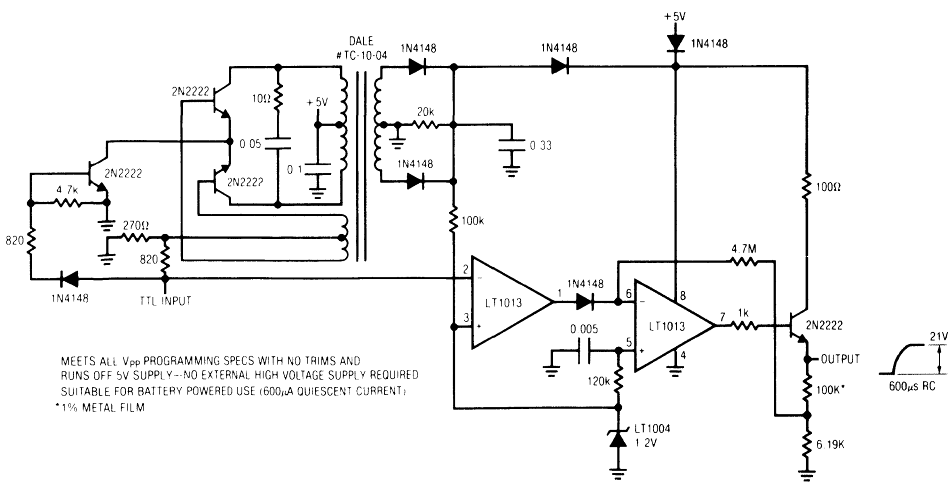
OFFSET = 150μV
GAIN = $\frac{R2}{R1} + 1$
CMRR = 120 dB
COMMON-MODE RANGE IS 0V TO 5V

TYPICAL APPLICATIONS

5V Powered Motor Speed Controller
No Tachometer Required

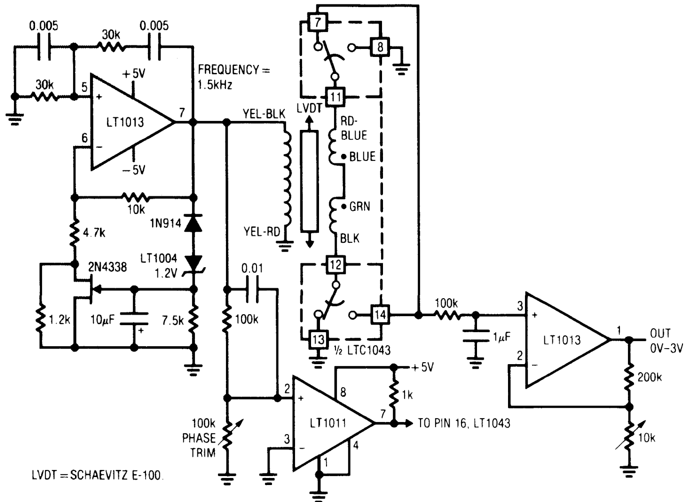


5V Powered EEPROM Pulse Generator



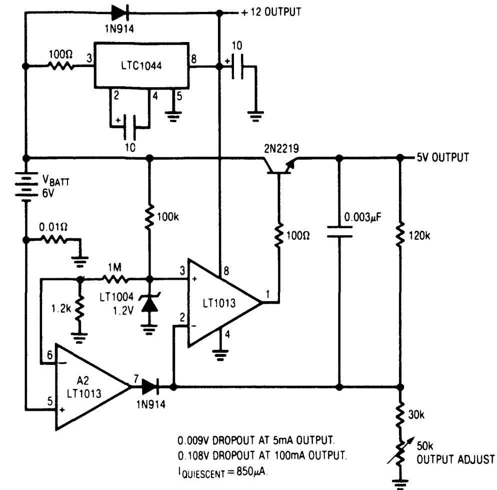
TYPICAL APPLICATIONS

LVDT Signal Conditioner

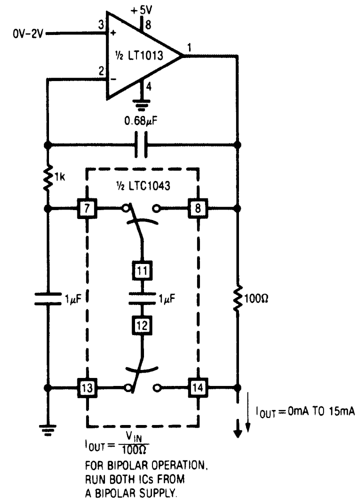


TYPICAL APPLICATIONS

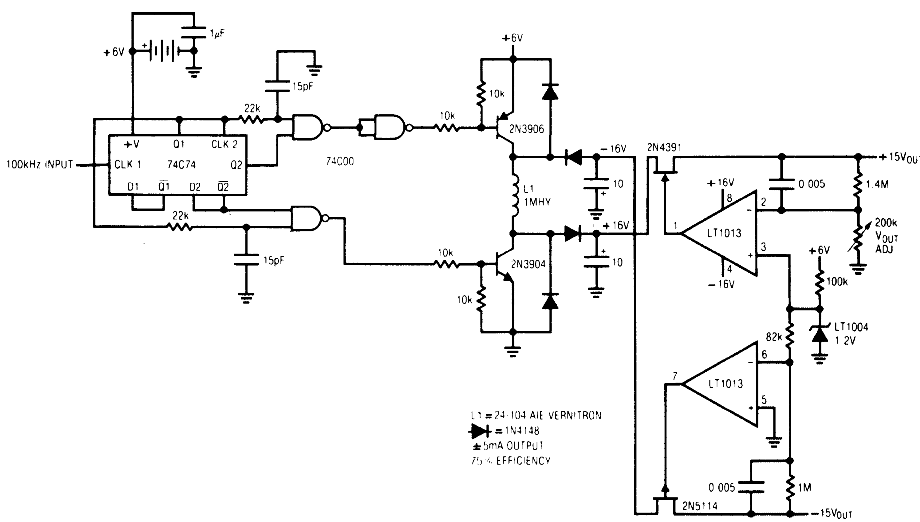
Low Dropout Regulator for 6V Battery



Voltage Controlled Current Source with Ground Referred Input and Output

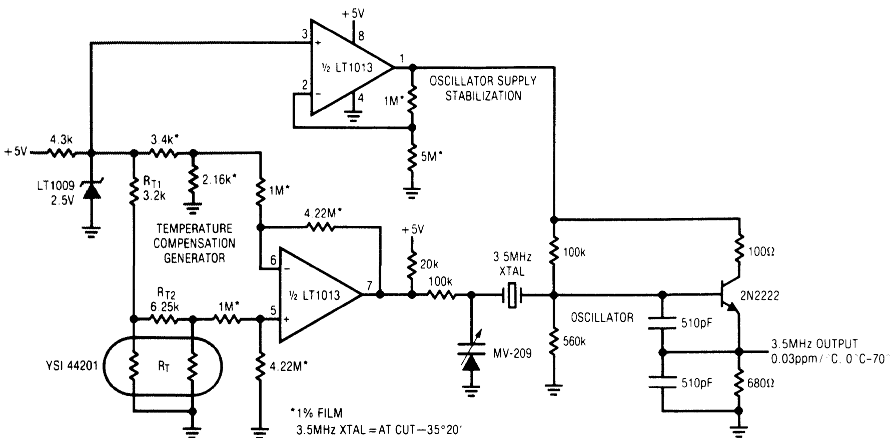


6V to ±15V Regulating Converter



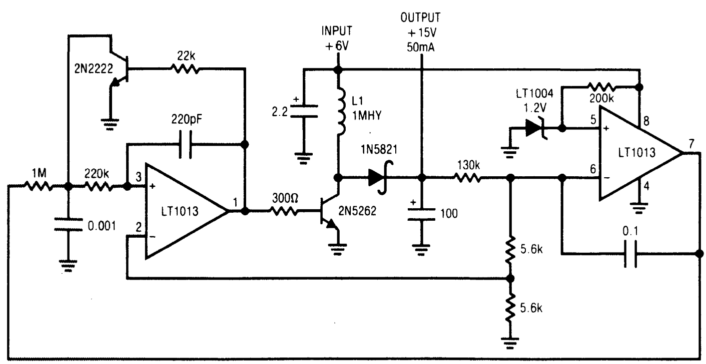
TYPICAL APPLICATIONS

Low Power, 5V Driven, Temperature Compensated Crystal Oscillator (TXCO)†



*1% FILM
3.5MHz XTAL = AT CUT—35°20′
MOUNT R_T NEAR XTAL
3mA POWER DRAIN
†THERMISTOR-AMPLIFIER-VARACTOR NETWORK GENERATES A TEMPERATURE COEFFICIENT OPPOSITE THE CRYSTAL TO MINIMIZE OVERALL OSCILLATOR DRIFT

Step-Up Switching Regulator for 6V Battery



L1 = AIE—VERNITRON 24-104
78% EFFICIENCY

FEATURES

- Voltage Noise — 1.1nV/√Hz Max. at 1kHz; 0.85nV/√Hz Typ. at 1kHz; 1.0nV/√Hz Typ. at 10Hz; 35nVp-p Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product — 50MHz Min.
- Slew Rate — 11V/μs Min.
- Offset Voltage — 40μV Max.
- Voltage Gain — 7 Million Min.
- Drift with Temperature — 0.8μV/°C Max.

APPLICATIONS

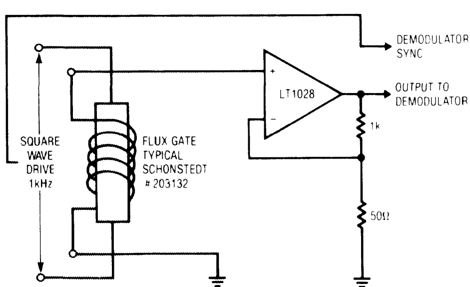
- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

DESCRIPTION

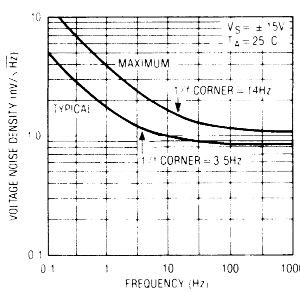
The LT1028 achieves a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz), distortion free output, and true precision parameters (0.1μV/°C drift, 10μV offset voltage, 30 million voltage gain). Although the LT1028 input stage operates at nearly 1mA of collector currents to achieve low voltage noise, input bias current is only 25nA.

The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

Flux Gate Amplifier



Voltage Noise vs Frequency



ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

TEXAS INSTRUMENTS

ABSOLUTE MAXIMUM RATINGS

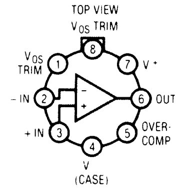
Supply Voltage
- −55°C to 105°C .... ±22V
- 105°C to 125°C .... ±16V

Differential Input Current (Note 8)................ ±25mA
Input Voltage ....Equal to Supply Voltage
Output Short Circuit Duration ....Indefinite
Operating Temperature Range
- LT1028AM, M........................ −55°C to 125°C
- LT1028AC, C ....0°C to 70°C

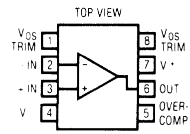
Storage Temperature Range
- All Devices.......................... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.).............300°C

PACKAGE/ORDER INFORMATION

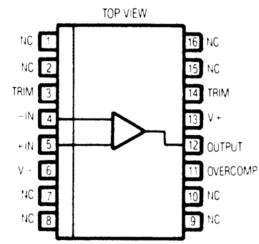


L PACKAGE TO-5 METAL CAN



JG PACKAGE HERMETIC DIP
P PACKAGE PLASTIC DIP

ORDER PART NUMBER
LT1028AML LT1028ML LT1028ACL LT1028CL
LT1028AMJG LT1028MJG LT1028ACJG LT1028CJG LT1028ACP LT1028CP



D PACKAGE
PLASTIC SO

ORDER PART NUMBER
LT1028CD
PART MARKING
LT1028CD

The D packages are available taped and reeled. Add the suffix R to the device type when ordering taped parts (ie. LT1028CDR)

3 Operational Amplifiers

TEXAS INSTRUMENTS

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AM/AC MIN	LT1028AM/AC TYP	LT1028AM/AC MAX	LT1028M/C MIN	LT1028M/C TYP	LT1028M/C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	40		20	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3			0.3		μV/Mo
I_{OS}	Input Offset Current	$V_{CM} = 0V$		12	50		18	100	nA
I_B	Input Bias Current	$V_{CM} = 0V$		± 25	± 90		± 30	± 180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	75		35	90	nVp-p
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 4) $f_o = 1000Hz$		1.0 0.85	1.7 1.1		1.0 0.9	1.9 1.2	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	$f_o = 10Hz$ (Notes 3 and 5) $f_o = 1000Hz$		4.7 1.0	10.0 1.6		4.7 1.0	12.0 1.8	pA/√Hz pA/√Hz
	Input Resistance Common-Mode Differential Mode			 300 20			 300 20		 MΩ kΩ
	Input Capacitance			5			5		pF
	Input Voltage Range		± 11.0	± 12.2		± 11.0	± 12.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	117	133		110	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 12V$ $R_L \geq 1k\Omega, V_o = \pm 10V$ $R_L \geq 600\Omega, V_o = \pm 10V$	7.0 5.0 3.0	30.0 20.0 15.0		5.0 3.5 2.0	30.0 20.0 15.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	± 12.3 ± 11.0	± 13.0 ± 12.2		± 12.0 ± 10.5	± 13.0 ± 12.2		V V
SR	Slew Rate	$A_{VCL} = -1$	11	15		11	15		V/μs
GBW	Gain-Bandwidth Product	$f_o = 20kHz$ (Note 6)	50	75		50	75		MHz
Z_o	Open Loop Output Impedance	$V_o = 0, I_o = 0$		80			80		Ω
I_S	Supply Current			7.4	9.5		7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AM MIN	LT1028AM TYP	LT1028AM MAX	LT1028M MIN	LT1028M TYP	LT1028M MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	120		45	180	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift		●		0.2	0.8		0.25	1.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		25	90		30	180	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±40	±150		±50	±300	nA
	Input Voltage Range		●	±10.3	±11.7		±10.3	±11.7		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 16V$	●	110	130		104	130		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$ $R_L \ge 1k\Omega$, $V_O = \pm 10V$	●	3.0 2.0	14.0 10.0		2.0 1.5	14.0 10.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±10.3	±11.6		±10.3	±11.6		V
I_S	Supply Current		●		8.7	11.5		9.0	13.0	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AC MIN	LT1028AC TYP	LT1028AC MAX	LT1028C MIN	LT1028C TYP	LT1028C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		15	80		30	125	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift		●		0.1	0.8		0.2	1.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		15	65		22	130	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±30	±120		±40	±240	nA
	Input Voltage Range		●	±10.5	±12.0		±10.5	±12.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	110	124		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	114	132		107	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_O = \pm 10V$ $R_L \ge 1k\Omega$, $V_O = \pm 10V$	●	5.0 4.0	25.0 18.0		3.0 2.5	25.0 18.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$ $R_L \ge 600\Omega$ (Note 8)	●	±11.5 ±9.5	±12.7 ±11.0		±11.5 ±9.0	±12.7 ±10.5		V V
I_S	Supply Current		●		8.0	10.5		8.2	11.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25°C$, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from testing at 1kHz.

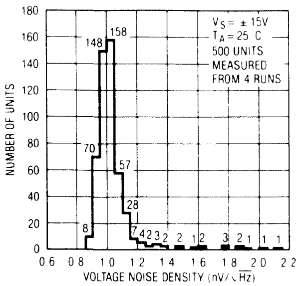
Note 6: Gain-bandwidth product is not tested. It is characterized by design and by inference from the slew rate measurement.

Note 7: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ± 1.8V, the input current should be limited to 25mA.

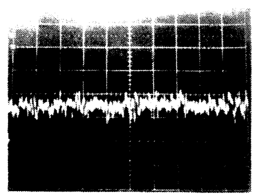
Note 8: This parameter characterized by design, fully warmed up at $T_A = 70°C$. It includes chip temperature increase due to supply and load currents

TYPICAL PERFORMANCE CHARACTERISTICS

10Hz Voltage Noise Distribution

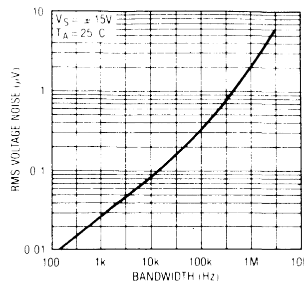


Wideband Noise, DC to 20kHz

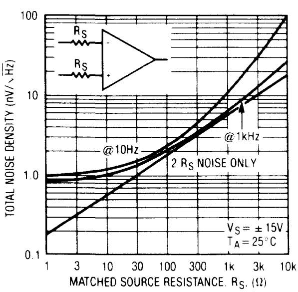


VERTICAL SCALE = 0.5μV/DIV
HORIZONTAL SCALE = 0.5ms/DIV

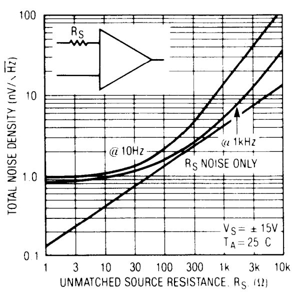
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



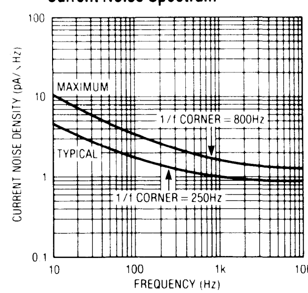
Total Noise vs Matched Source Resistance



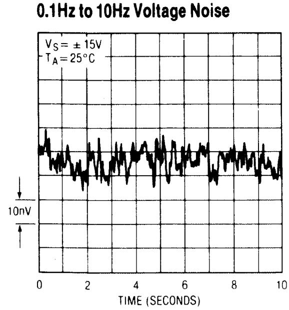
Total Noise vs Unmatched Source Resistance



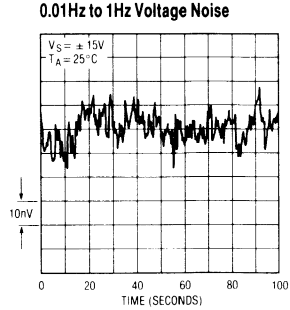
Current Noise Spectrum



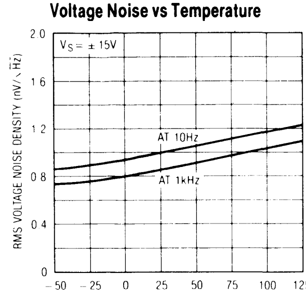
0.1Hz to 10Hz Voltage Noise



0.01Hz to 1Hz Voltage Noise



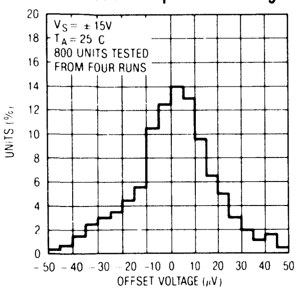
Voltage Noise vs Temperature



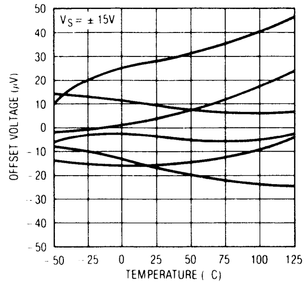
3 Operational Amplifiers

TYPICAL PERFORMANCE CHARACTERISTICS

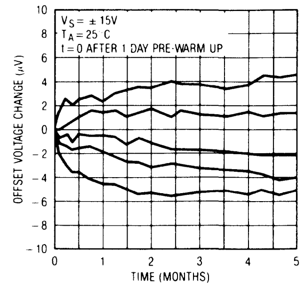
Distribution of Input Offset Voltage



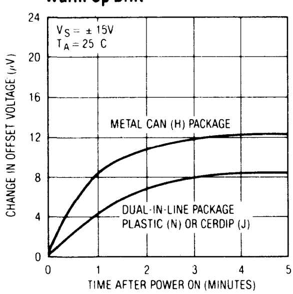
Offset Voltage Drift with Temperature of Representative Units



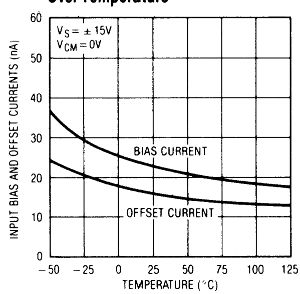
Long Term Stability of Five Representative Units



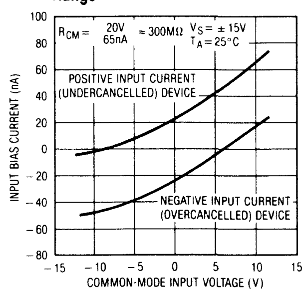
Warm-Up Drift



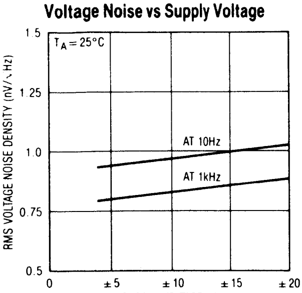
Input Bias and Offset Currents Over Temperature



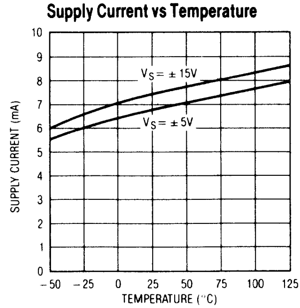
Bias Current Over the Common-Mode Range



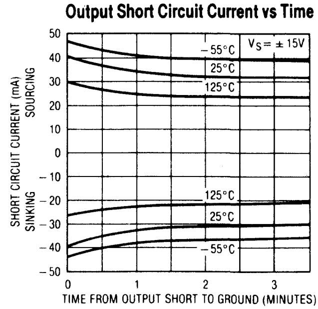
Voltage Noise vs Supply Voltage



Supply Current vs Temperature

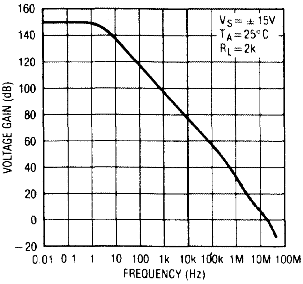


Output Short Circuit Current vs Time

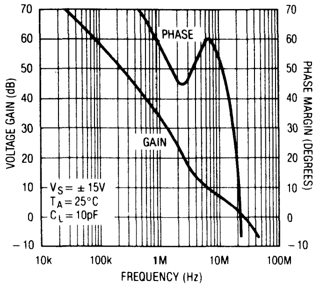


TYPICAL PERFORMANCE CHARACTERISTICS

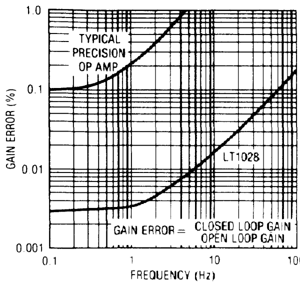
Voltage Gain vs Frequency



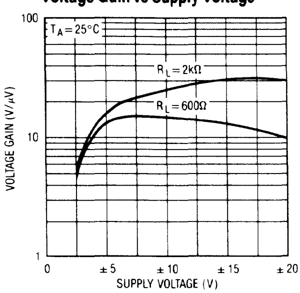
Gain, Phase vs Frequency



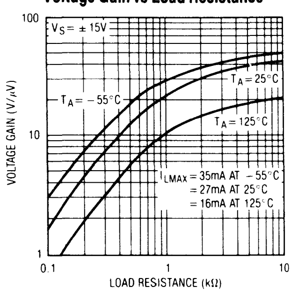
Gain Error vs Frequency Closed Loop Gain = 1000



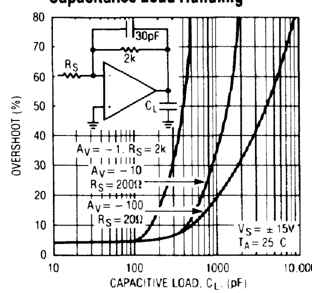
Voltage Gain vs Supply Voltage



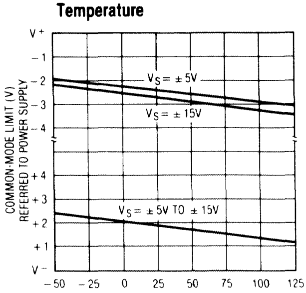
Voltage Gain vs Load Resistance



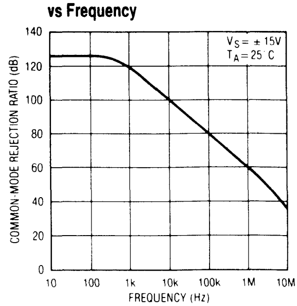
Capacitance Load Handling



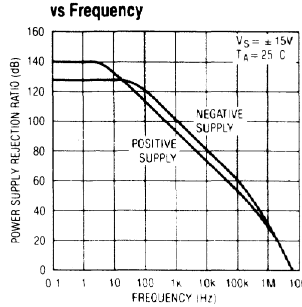
Common-Mode Limit Over Temperature



Common-Mode Rejection Ratio vs Frequency

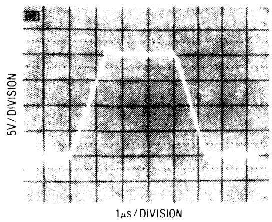


Power Supply Rejection Ratio vs Frequency



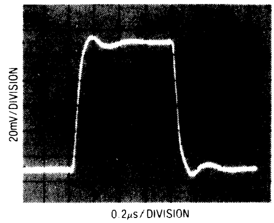
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Transient Response



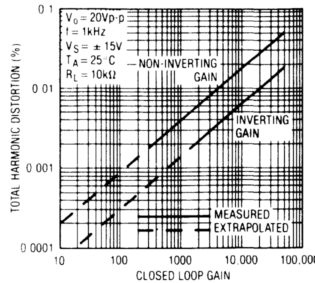
$A_V = -1$ $R_S = R_f = 2k$ $C_f = 30pF$

Small Signal Transient Response

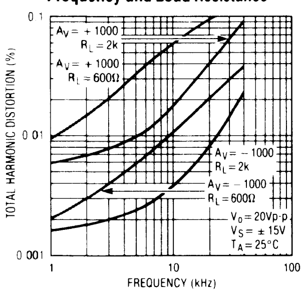


$A_V = -1$ $R_S = R_f = 2k\Omega$
$C_f = 30pF$, $C_L = 80pF$

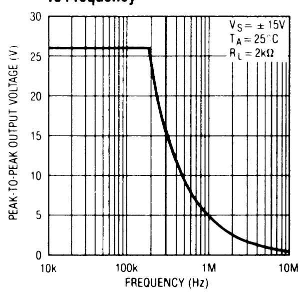
Total Harmonic Distortion vs Closed Loop Gain



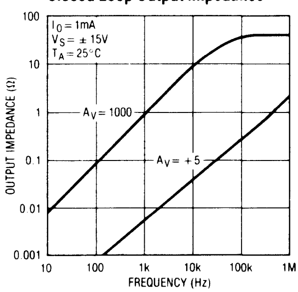
Total Harmonic Distortion vs Frequency and Load Resistance



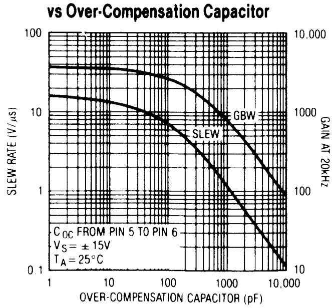
Maximum Undistorted Output vs Frequency



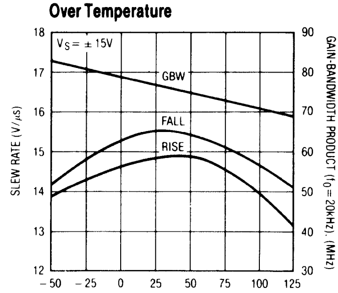
Closed Loop Output Impedance



Slew Rate, Gain-Bandwidth-Product vs Over-Compensation Capacitor



Slew Rate, Gain-Bandwidth Product Over Temperature



APPLICATIONS INFORMATION —NOISE

Voltage Noise vs Current Noise

The LT1028's less than $1nV/\sqrt{Hz}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise (e_n), current noise (i_n) and resistor noise (r_n).

Total Noise vs Source Resistance

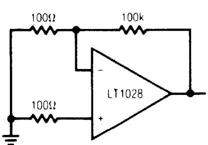
The total input referred noise of an op amp is given by

$$e_t = [e_n^2 + r_n^2 + (i_n R_{eq})^2]^{1/2}$$

where R_{eq} is the total equivalent source resistance at the two inputs

and $r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{R_{eq}}$ in $nV/\sqrt{Hz}$ at 25°C

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown below.



$R_{eq} = 100\Omega + 100\Omega \| 100k \approx 200\Omega$
$r_n = 0.13\sqrt{200} = 1.84nV/\sqrt{Hz}$
$e_n = 0.85nV/\sqrt{Hz}$
$i_n = 1.0pA/\sqrt{Hz}$
$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04nV/\sqrt{Hz}$

output noise $= 1000\, e_t = 2.04\mu V/\sqrt{Hz}$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As R_{eq} is increased resistor noise becomes the largest term—as in the example above—and the LT1028's voltage noise becomes negligible. As R_{eq} is further increased, current noise becomes important. At 1kHz, when R_{eq} is in excess of 20kΩ, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k\Omega$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1kΩ because the resistor noise contribution is less. When $R_S > 1k\Omega$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1028 is the optimum amplifier for noise performance—provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise—as the source resistance is increased beyond the LT1028's level of usefulness.

Best Op Amp for Lowest Total Noise vs Source Resistance

SOURCE RESISTANCE (Note 1)	BEST OP AMP AT LOW FREQ (10Hz)	BEST OP AMP WIDEBAND (1kHz)
0 to 400Ω	LT1028	LT1028
400Ω to 4kΩ	LT1007/1037	LT1028
4kΩ to 40kΩ	LT1001	LT1007/1037
40kΩ to 500kΩ	LT1012	LT1001
500kΩ to 5MΩ	LT1012 or LT1055	LT1012
>5M	LT1055	LT1055

Note 1: Source resistance is defined as matched or unmatched, e.g., $R_S = 1k\Omega$ means: 1kΩ at each input, or 1kΩ at one input and zero at the other.

3 Operational Amplifiers

APPLICATIONS INFORMATION —NOISE

Noise Testing—Voltage Noise

The LT1028's RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed loop gain of 31 with a 60Ω source resistor and a 1.8kΩ feedback resistor. The noise of this resistor combination is $0.13\sqrt{58} = 1.0\text{nV}/\sqrt{\text{Hz}}$. An LT1028 with $0.85\text{nV}/\sqrt{\text{Hz}}$ noise will read $(0.85^2 + 1.0^2)^{1/2} = 1.31\text{nV}/\sqrt{\text{Hz}}$. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8-10% too high.

The 0.1Hz to 10Hz peak-to-peak noise of the LT1028 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028 requires special test precautions:

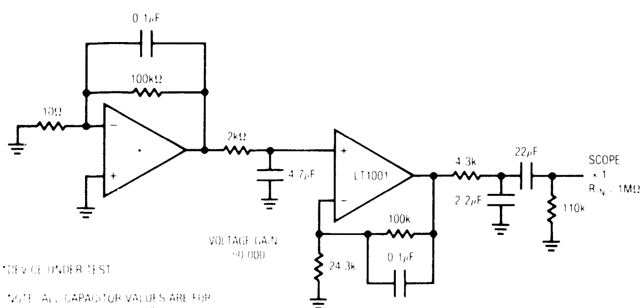
(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 10μV due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

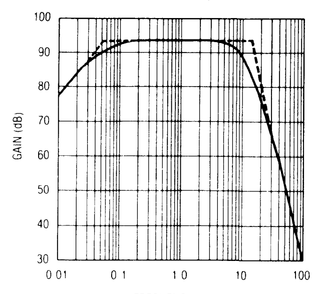
(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz p-p Noise Tester Frequency Response



3 Operational Amplifiers

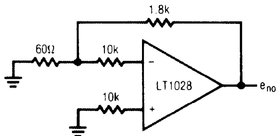
TEXAS INSTRUMENTS

APPLICATIONS INFORMATION —NOISE

Noise Testing—Current Noise

Current noise density (i_n) is defined by the following formula, and can be measured in the circuit shown:

$$i_n = \frac{[e_{no}^2 - (31 \times 18.4nV/\sqrt{Hz})^2]^{1/2}}{20k \times 31}$$



If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

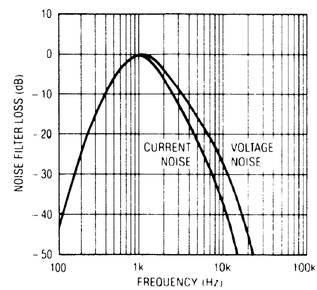
100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.

Automated Tester Noise Filter



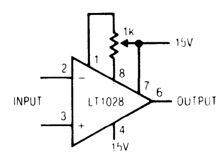
APPLICATIONS INFORMATION

General

The LT1028 series devices may be inserted directly into OP-07, OP-27, OP-37, LT1007 and LT1037 sockets with or without removal of external nulling components. In addition, the LT1028 may be fitted to 5534 sockets with the removal of external compensation components.

Offset Voltage Adjustment

The input offset voltage of the LT1028 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 1k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C.



The adjustment range with a 1k pot is approximately ±1.1mV.

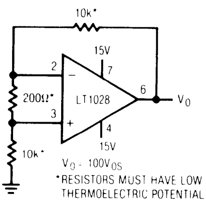
Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

APPLICATIONS INFORMATION

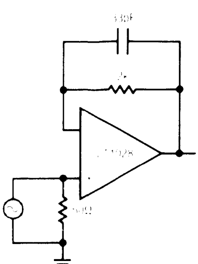
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1028.

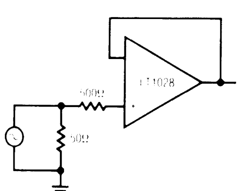
Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



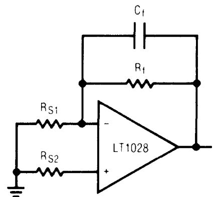
Frequency Response

The LT1028's Gain, Phase vs Frequency plot indicates that the device is stable in closed loop gains greater than +2 or −1 because phase margin is about 50° at an open loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the non-inverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided $C_f < 68pF$), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the non-inverting input has a similar effect. The following voltage follower configurations are stable:



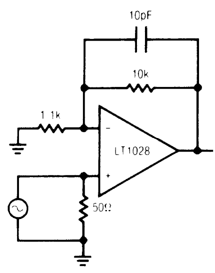


Another configuration which requires unity gain stability is shown below. When C_f is large enough to effectively short the output to the input at 15MHz, oscillations can occur. The insertion of $R_{S2} \geq 500\Omega$ will prevent the LT1028 from oscillating. When $R_{S1} \geq 500\Omega$, the additional noise contribution due to the presence of R_{S2} will be minimal. When $R_{S1} \leq 100\Omega$, R_{S2} is not necessary, because R_{S1} represents a heavy load on the output through the C_f short. When $100\Omega < R_{S1} < 500\Omega$, R_{S2} should match R_{S1}. For example, $R_{S1} = R_{S2} = 300\Omega$ will be stable. The noise increase due to R_{S2} is 40%.



If C_f is only used to cut noise bandwidth, a similar effect can be achieved using the over-compensation terminal.

The Gain, Phase plot also shows that phase margin is about 45° at a gain of 10 (20dB). The following configuration has a high (≈70%) overshoot without the 10pF capacitor because of additional phaseshift caused by the feedback resistor—input capacitance pole. The presence of the 10pF capacitor cancels this pole and reduces overshoot to 5%.

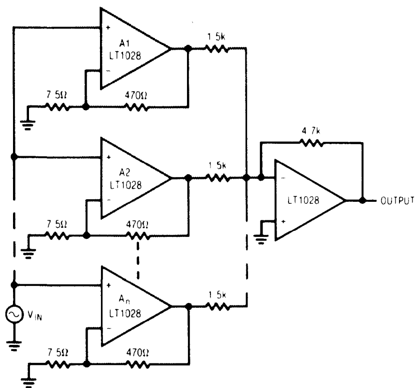


Over-Compensation

The LT1028 is equipped with a frequency over-compensation terminal (pin 5). A capacitor connected between pin 5 and the output will reduce noise bandwidth. Details are shown on the Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor plot. An additional benefit is increased capacitive load handling capability.

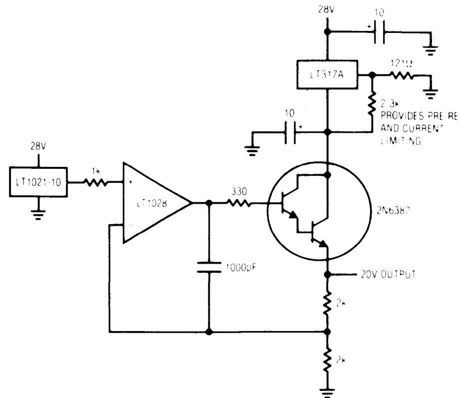
TYPICAL APPLICATIONS

Paralleling Amplifiers to Reduce Voltage Noise

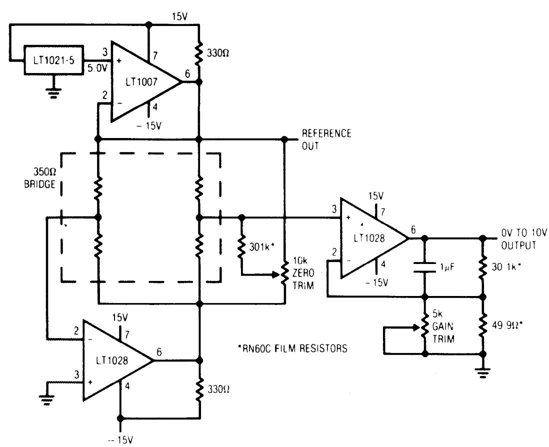


1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = 0.9nV/$\sqrt{Hz}$
2. GAIN WITH n LT1028's IN PARALLEL = n × 200
3. OUTPUT NOISE = $\sqrt{n}$ × 200 × 0.9nV/$\sqrt{Hz}$
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = \frac{0.9}{\sqrt{n}}$ nV/$\sqrt{Hz}$
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES
6. IF n = 5, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz, = $\frac{2\mu V}{\sqrt{5}}$ = 0.9μV

Low Noise Voltage Regulator



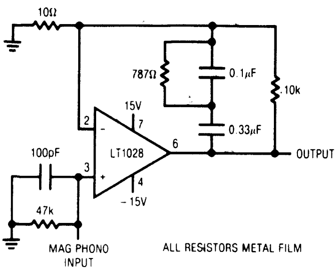
Strain Gauge Signal Conditioner with Bridge Excitation



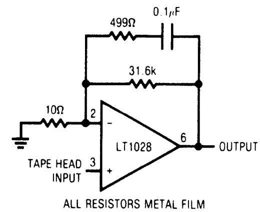
THE LT1028's NOISE CONTRIBUTION IS NEGLIGIBLE COMPARED TO THE BRIDGE NOISE

TYPICAL APPLICATIONS

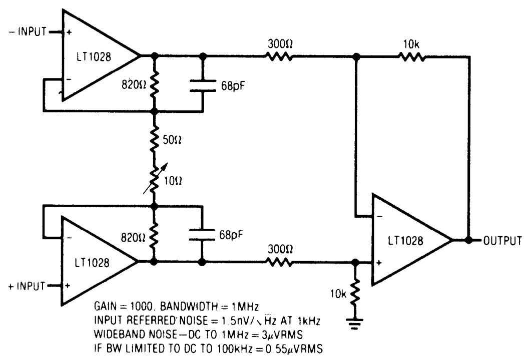
Phono Preamplifier



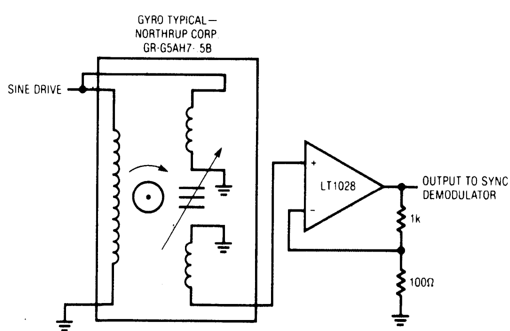
Tape Head Amplifier



Low Noise, Wide Bandwidth Instrumentation Amplifier



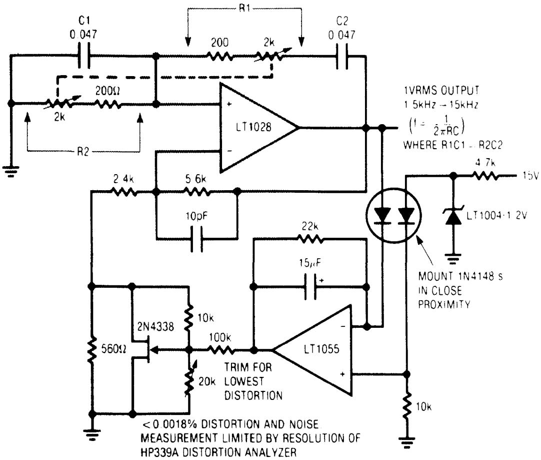
Gyro Pick-Off Amplifier



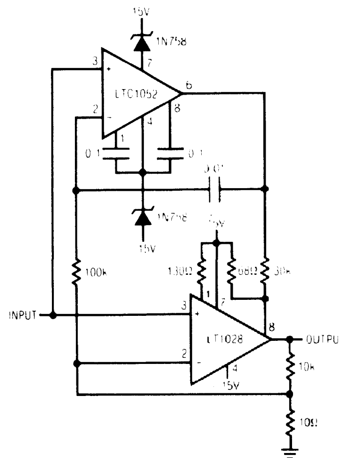
3 Operational Amplifiers

TYPICAL APPLICATIONS

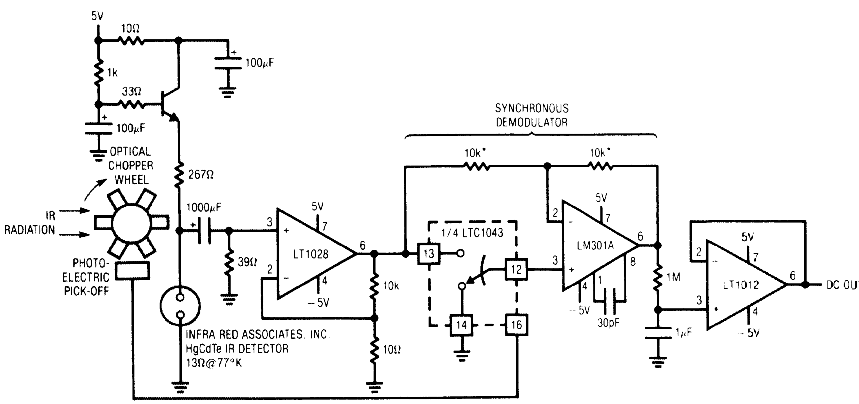
Super Low Distortion Variable Sine Wave Oscillator



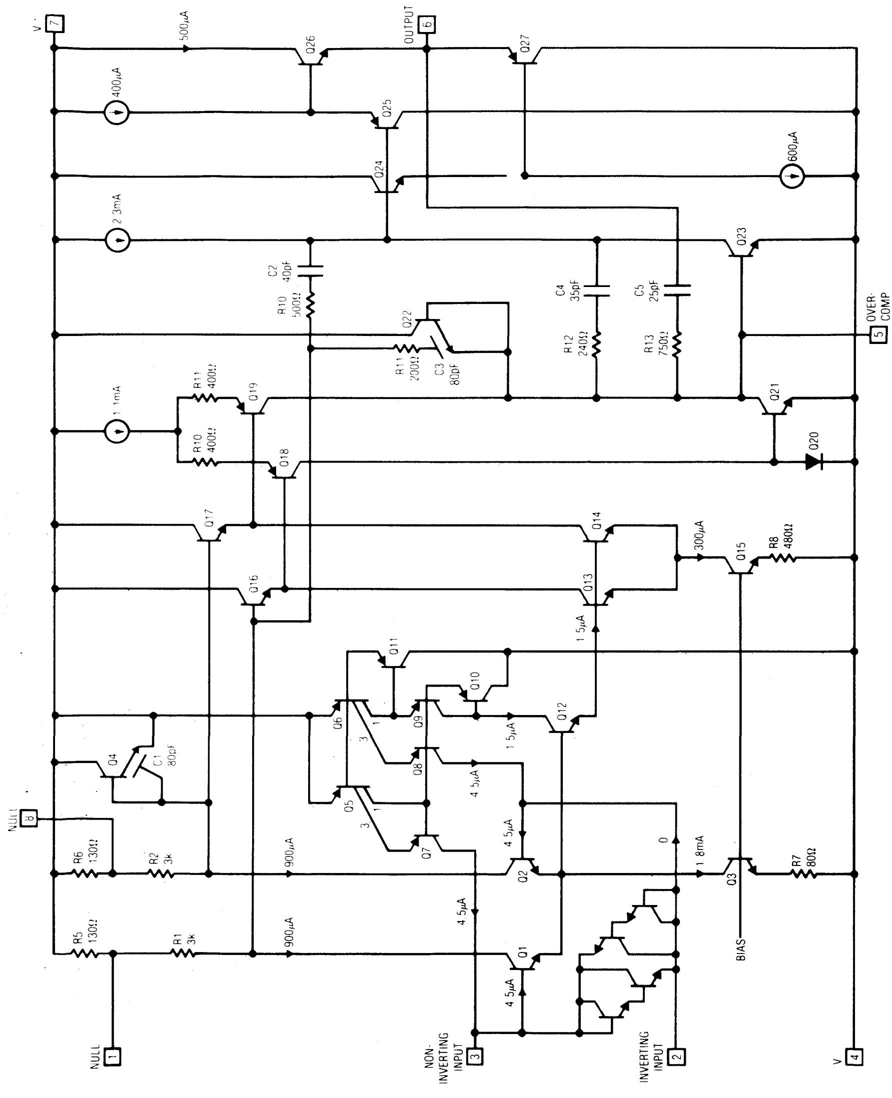
Chopper Stabilized Amplifier



Low Noise Infrared Detector



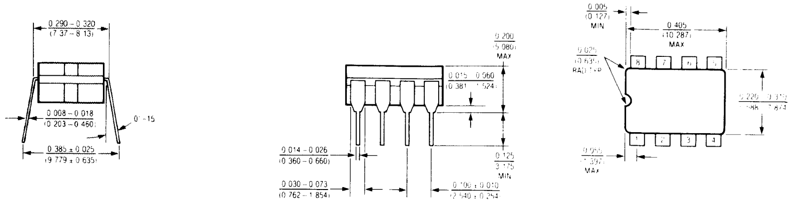
SCHEMATIC DIAGRAM



TEXAS INSTRUMENTS

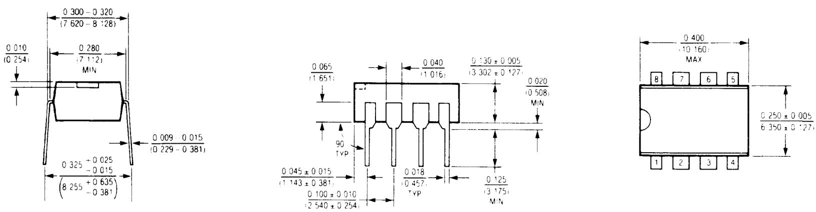
PACKAGE DESCRIPTIONS Dimensions in inches (millimeters) unless otherwise noted.

JG Package
Ceramic DIP



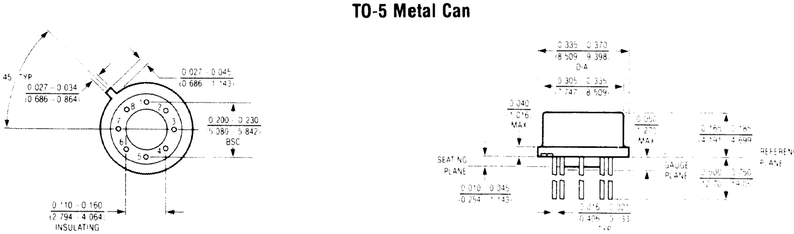
$T_j$max	θ_{ja}
165°C	100°C/W

P Package
Molded DIP



$T_j$max	θ_{ja}
115°C	130°C/W

L Package
TO-5 Metal Can

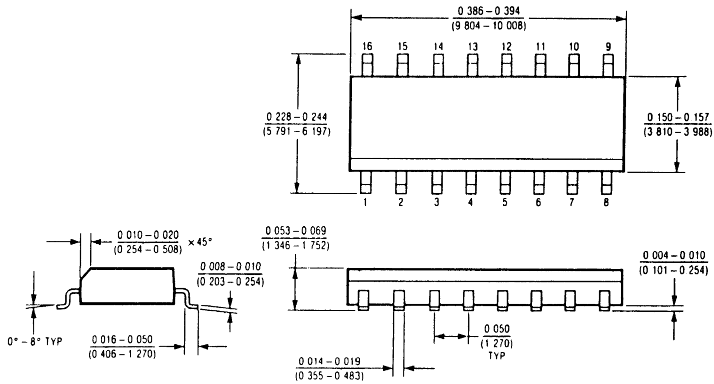


NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE

$T_j$max	θ_{ja}	θ_{jc}
175°C	140°C/W	40°C/W

PACKAGE DESCRIPTIONS Dimensions in inches (millimeters) unless otherwise noted.

D Package



FEATURES

- Max. Offset 5μV
- Max. Offset Drift 0.05μV/°C
- Typ. Offset Drift 0.01μV/°C
- Excellent Long Term Stability 100nV/√Month
- Max. Input Bias Current 30pA
- Over Operating Temperature Range
  Min. Gain 120dB
  Min. CMRR 120dB
  Min. PSRR 120dB
- Single Supply Operation 4.75V to 16V
  (Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V⁻ with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

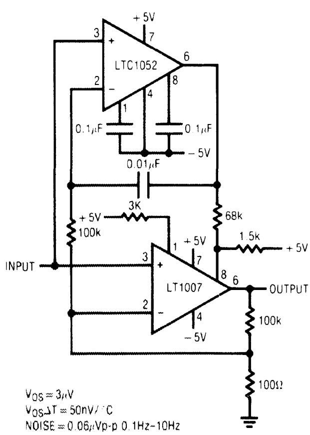
DESCRIPTION

The LTC1052 and LTC7652 are low noise Chopper-stabilized op amps (CSOA™) manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common-mode voltage are corrected. This, coupled with picoampere input currents, gives these amplifiers unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

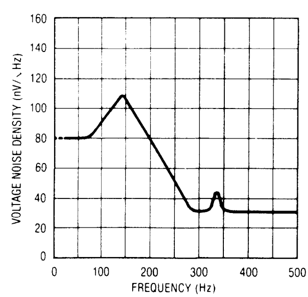
The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin version to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

Ultra Low Noise, Low Drift Amplifier



$V_{OS} \approx 3\mu V$
$V_{OS}\Delta T \approx 50nV/°C$
NOISE ≈ 0.06μVp-p 0.1Hz–10Hz

LTC1052 Noise Spectrum



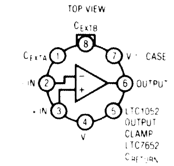
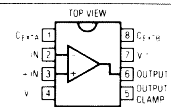
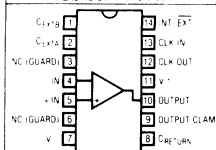
CSOA™ and LTCMOS™ are trademarks of Linear Technology Corporation
Teflon™ is a trademark of DuPont

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage .... (V^+ +0.3V) to (V^- −0.3V)
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
  LTC1052C/LTC7652C .... −40°C to 85°C
  LTC1052M .... −55°C to 125°C
Storage Temperature Range .... −55°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER	REPLACES
 METAL CAN L PACKAGE	LTC7652CL LTC1052CL LTC1052ML	ICL7652CTV ICL7652ITV ICL7650CTV-1 ICL7650ITV-1 ICL7650CTV ICL7650ITV ICL7650MTV
 HERMETIC DIP JG PACKAGE PLASTIC DIP P PACKAGE	LTC1052CP LTC1052CJG LTC1052MJG	ICL7650CPA ICL7650IJA
 HERMETIC DIP J PACKAGE PLASTIC DIP N PACKAGE	LTC1052CJ LTC1052CN LTC1052MJ	ICL7652IJD ICL7650IJD ICL7652CPD ICL7650CPD ICL7650MJD

ELECTRICAL CHARACTERISTICS

V_S = ±5V, T_A = operating temperature range, test circuit TC1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1052M MIN	LTC1052M TYP	LTC1052M MAX	LTC1052C/LTC7652C MIN	LTC1052C/LTC7652C TYP	LTC1052C/LTC7652C MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 3)			±0.5	±5		±0.5	±5	μV
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Drift	(Note 3)	●		±0.01	±0.05		±0.01	±0.05	μV/°C
$\Delta V_{OS}/\Delta Time$	Long Term Offset Voltage Stability				100			100		nV/√Month
I_{OS}	Input Offset Current	T_A = 25°C			±5	±30		±5	±30	pA
			●			±2000			±350	pA
I_B	Input Bias Current	T_A = 25°C			±1	±30		±1	±30	pA
			●			±1000			±175	pA
e_{np-p}	Input Noise Voltage	R_S = 100Ω, DC to 10Hz, TC3			1.5			1.5		μVp-p
		R_S = 100Ω, DC to 1Hz, TC3			0.5			0.5		μVp-p
i_n	Input Noise Current	f = 10Hz (Note 5)			0.6			0.6		fA/√Hz
CMRR	Common-Mode Rejection Ratio	V_{CM} = V− to +2.7V	●	120	140		120	140		dB
PSRR	Power Supply Rejection Ratio	V_{SUPPLY} = ±2.375V to ±8V	●	120	150		120	150		dB
A_{VOL}	Large Signal Voltage Gain	R_L = 10k, V_{OUT} = ±4V	●	120	150		120	150		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	R_L = 10k	●	±4.7	±4.85		±4.7	±4.85		V
		R_L = 100k			±4.95			±4.95		V
SR	Slew Rate	R_L = 10k, C_L = 50pF			4			4		V/μs
GBW	Gain Bandwidth Product				1.2			1.2		MHz
I_S	Supply Current	No Load, T_A = 25°C			1.7	2.0		1.7	2.0	mA
			●			3.0			3.0	mA
f_S	Internal Sampling Frequency				330			330		Hz
	Clamp On Current	R_L = 100k	●	25	100		25	100		μA
	Clamp Off Current	−4V < V_{OUT} < +4V			10	100		10	100	pA
			●			2			1	nA

TEXAS INSTRUMENTS

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052/LTC7652.

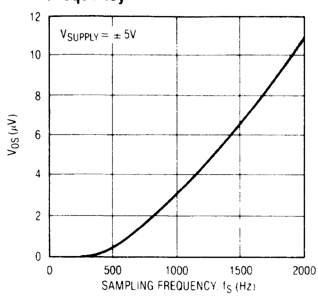
Note 3: Thermocouple effects preclude measurement of these voltage levels in high speed automatic testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB}, A_{VOL}, CMRR and PSRR are measured to insure proper operation of the nulling loop to insure meeting the V_{OS} and V_{OS} drift specification. See Package-Induced V_{OS} in applications section.

Note 4: Output clamp not connected.

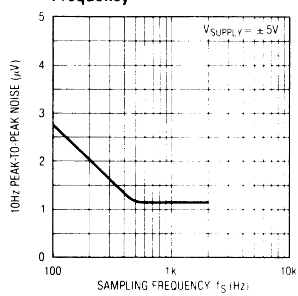
Note 5: Current noise is calculated from the formula: $i_n = (2q\, I_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb.

TYPICAL PERFORMANCE CHARACTERISTICS

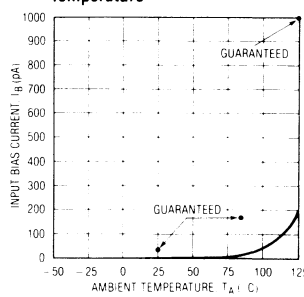
Offset Voltage vs Sampling Frequency



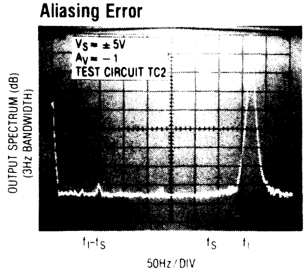
10Hzp-p Noise vs Sampling Frequency



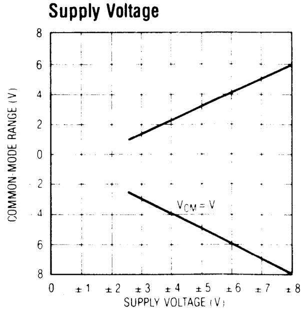
Input Bias Current vs Temperature



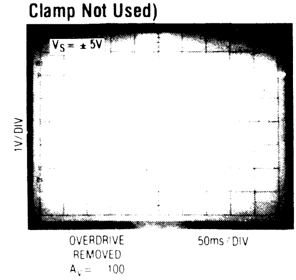
Aliasing Error



Common-Mode Input Range vs Supply Voltage

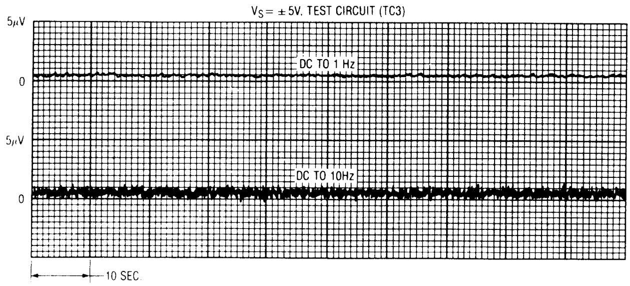


Overload Recovery (Output Clamp Not Used)

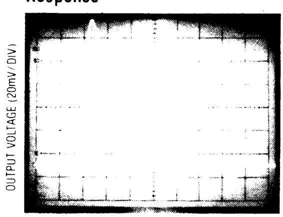


TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise Voltage

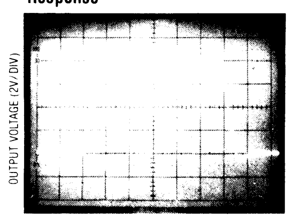


Small Signal Transient Response*



$A_V = +1$ $2\mu s/DIV$
$R_L = 10k$
$C_L = 100pF$
$V_S = \pm 5V$

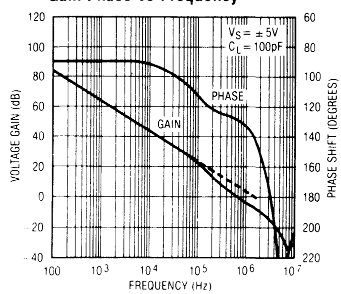
Large Signal Transient Response*



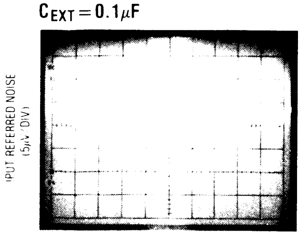
$A_V = +1$ $2\mu s/DIV$
$R_L = 10k$
$C_L = 100pF$
$V_S = \pm 5V$

*RESPONSE IS NOT DEPENDENT ON PHASE OF CLOCK

Gain Phase vs Frequency

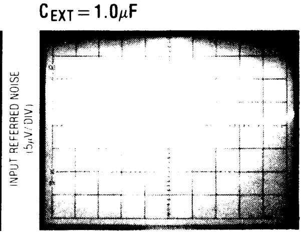


Broadband Noise, $C_{EXT} = 0.1\mu F$



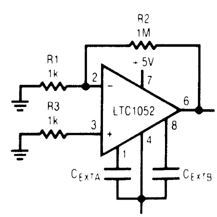
$A_V = 1000$ 1ms/DIV

Broadband Noise, $C_{EXT} = 1.0\mu F$



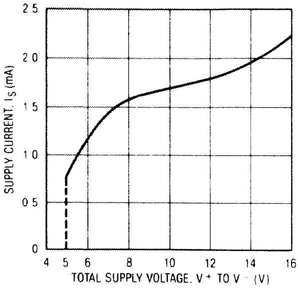
$A_V = 1000$ 1ms/DIV

Broadband Noise Test Circuit (TC2)

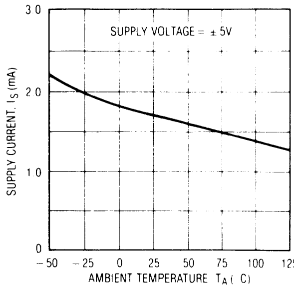


TYPICAL PERFORMANCE CHARACTERISTICS

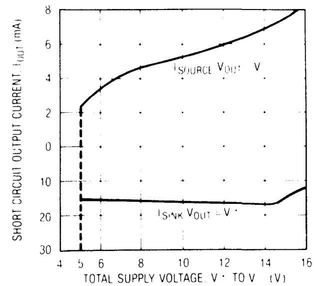
Supply Current vs Supply Voltage



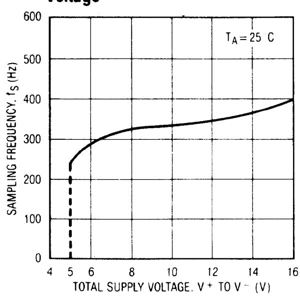
Supply Current vs Temperature



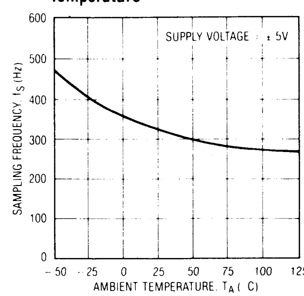
Output Short Circuit Current vs Supply Voltage



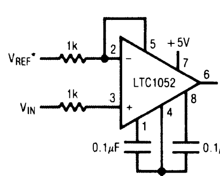
Sampling Frequency vs Supply Voltage



Sampling Frequency vs Temperature

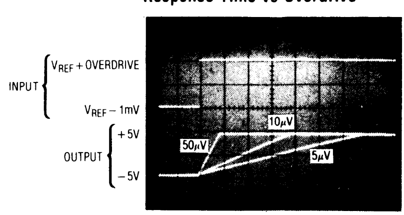


Comparator Operation



* − 5V ≤ V_{REF} ≤ 2.7V

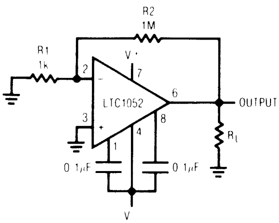
Response Time vs Overdrive



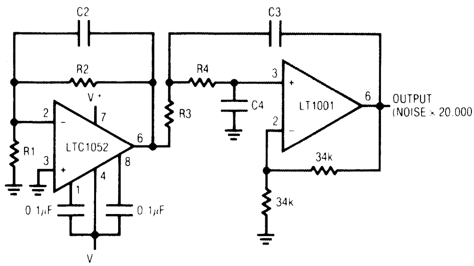
20ms/DIV

TEST CIRCUITS

Electrical Characteristics Test Circuit (TC1)



DC to 10Hz and DC to 1Hz Noise Test Circuit (TC3)



BANDWIDTH	R1	R2	R3	R4	C2	C3	C4
10Hz	16.2Ω	162k	16.2k	16.2k	0.1μF	1.0μF	1.0μF
1Hz	16.2Ω	162k	162k	162k	1.0μF	1.0μF	1.0μF

THEORY OF OPERATION

DC OPERATION

The shaded portion of the LTC1052 block diagram (Figure 1) entirely determines the amplifier's DC characteristics. During the auto-zero portion of the cycle, the inputs are shorted together and a feedback path is closed around the input stage to null its offset. Switch S2 and capacitor C_{EXTA} act as a sample and hold to store the nulling voltage during the next step—the sampling cycle.

In the sampling cycle, the zeroed amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S2 act as a sample and hold to store the amplified input signal during the auto-zero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the auto-zero cycle the inputs are not only shorted together, but are also shorted to the negative input. This forces nulling with the common-mode voltage present and accounts for the extremely high CMRR of the LTC1052. In the same fashion, variations in power supply are also nulled. For nulling to take place, the offset voltage, common-mode voltage and power supply must not change at a frequency which is high compared to the frequency response of the nulling loop.

AC OPERATION AND ALIASING ERRORS

So far, the DC performance of the LTC1052 has been explained. As the input signal frequency increases, the problem of aliasing must be addressed. Aliasing is the spurious formation of low and high frequency signals caused by the mixing of the input signal with the sampling frequency, f_S. The frequency of the error signals, f_E, is:

$$f_E = f_S \pm f_I$$

where f_I = input signal frequency.

Normally it is the difference frequency ($f_S - f_I$) which is of concern because the high frequency ($f_S + f_I$) can be easily filtered. As the input frequency approaches the sampling frequency, the difference frequency approaches zero and will cause DC errors—the exact problem that the chopping amplifier is meant to eliminate.

The solution is simple. Filter the input so the sampling loop never sees any frequency near the sampling frequency.

At a frequency well below the sampling frequency, the LTC1052 forces I_1 to equal I_2 (see Figure 1B). This makes δI zero, thus the gain of the sampling loop zero at this and higher frequencies—i.e., a low pass filter. The corner frequency of this low pass filter is set by the output stage pole ($1/R_{L4}\, g_{m5}\, R_{L5}\, C2$).

THEORY OF OPERATION

For frequencies above this pole, I_2 is:

$$I_2 = V_{IN}\, g_{m6} \times \frac{1}{SC2} \times SC1$$

and

$$I_1 - I_2 = V_{IN}\, g_{m1} - V_{IN}\, g_{m6} \times \frac{C1}{C2}.$$

The LTC1052 is very carefully designed so that $g_{m1} = g_{m6}$ and $C1 = C2$. Substituting these values in the above equation shows $I_1 - I_2 = 0$.

The g_{m6} input stage, with C1 and C2, not only filters the input to the sampling loop, but also acts as a high frequency path to give the LTC1052 good high frequency response. The unity-gain cross frequencies for both the DC path and high frequency path are identical

$$[f3dB = \frac{1}{2\pi}(g_{m1}/C1) = \frac{1}{2\pi}(g_{m6}/C2)].$$

This makes the frequency response smooth and continuous and eliminates sampling noise in the output as the loop transitions from the high gain DC loop to the high frequency loop.

The typical curves show just how well the amplifier works. The output spectrum shows the difference frequency ($f_I - f_S = 100Hz$) is down by 80dB and the frequency response curve shows no abnormalities or perturbations. Also note the well-behaved small and large signal step responses and the absence of the sampling frequency in the output spectrum. If the dynamics of the amplifier, i.e., slew rate and overshoot, depend on the sampling clock, the sampling frequency will appear in the output spectrum.

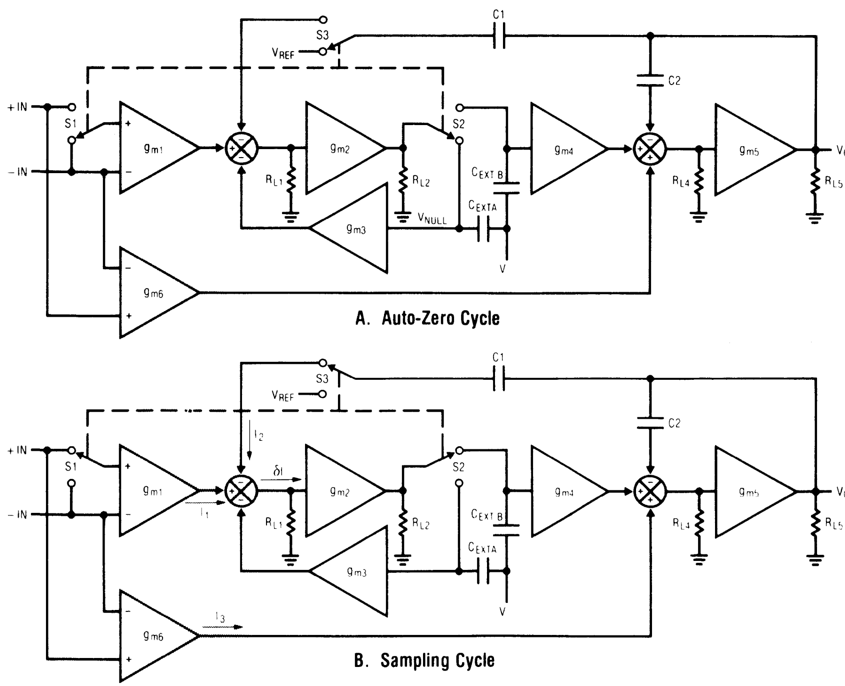


Figure 1. LTC1052 Block Diagram

APPLICATIONS INFORMATION

EXTERNAL CAPACITORS

C_{EXTA} and C_{EXTB} are the holding elements of a sample and hold circuit. The important capacitor characteristics are leakage current and dielectric absorption. A high quality film-type capacitor such as mylar or polypropylene provides excellent performance. However, low grade capacitors such as ceramic are suitable in many applications.

Capacitors with very high dielectric absorption (ceramic) can take several seconds to settle after power is first turned on. This settling appears as clock ripple on the output and, as the capacitor settles, the ripple gradually disappears. If fast settling after power turn-on is important, mylar or polypropylene is recommended.

Above 85°C, leakage, both from the holding capacitors and the printed circuit board, becomes important. To maintain the capabilities of the LTC1052 it may be necessary to use Teflon™ capacitors and Teflon standoffs when operating at 125°C (see Achieving Picoampere/Microvolt Performance).

C_{EXTA} and C_{EXTB} are normally in the range of 0.1μF to 1.0μF. All specifications are characterized with 0.1μF and the broadband noise (see typical photos) is only very slightly degraded with 0.1μF. Output clock ripple is not present for capacitors of 0.1μF or greater at any temperature.

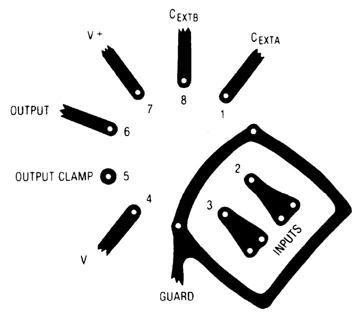
On competitive devices, connecting C_{EXTA} and C_{EXTB} to V^- causes an increase in amplifier noise. Design changes have eliminated this problem on the LTC1052. On the 14-pin LTC1052 and 8-pin LTC7652, the capacitors can be returned to V^- or C_{RETURN} with no change in noise performance.

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1052, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary—particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.



Microvolts

Thermocouple effects must be considered if the LTC1052's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C—4 times the maximum drift specification of

APPLICATIONS INFORMATION

the LTC1052. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C—700 times the maximum drift specification of the LTC1052.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 2 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table I shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

When all of these errors are considered, it may seem impossible to take advantage of the extremely low drift specifications of the LTC1052. To show that this is not the case, examine the temperature test circuit of Figure 3. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity and thermal resistance each input sees is balanced because of the symmetrical connection of resistors and their identical size. Thermal EMF-induced shifts are equal in phase and amplitude, thus cancellation occurs.

Figure 4 shows the response of this circuit under temperature transient conditions. Metal film resistors and an 8-pin DIP socket were used. Care was taken in the construction to thermally balance the inputs to the amplifier. The units were placed in an oven and allowed to stabilize at 25°C. The recording was started, and after 100 seconds the oven, preset to 125°C, was switched on. The test was first performed on an 8-pin plastic package and then was repeated for a TO-5 package plugged into the same test board. It is significant that the change in V_{OS}, even under these severe thermal transient conditions, is quite good. As temperature stabilizes, note that the steady-state change of V_{OS} is well within the maximum $\pm 0.05\mu$V/°C drift specification.

Table I. Resistor Thermal EMF

Resistor Type	Thermal EMF/°C Gradient
Tin Oxide	~ mV/°C
Carbon Composition	~ 450μV/°C
Metal Film	~ 20μV/°C
Wire Wound	
Evenohm	~ 2μV/°C
Manganin	~ 2μV/°C

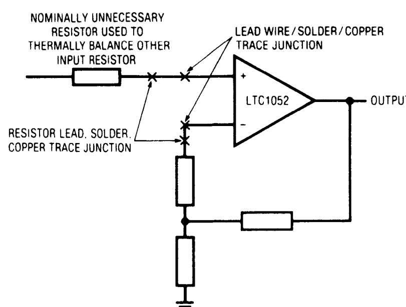


Figure 2

APPLICATIONS INFORMATION

Very slight air currents can still affect even this arrangement. Figure 5 shows strip charts of output noise with the circuit covered and with no cover in "still" air. This data illustrates why it is often prudent to enclose the LTC1052 and its attendant components inside some form of thermal baffle.

PACKAGE-INDUCED OFFSET VOLTAGE

Since the LTC1052 is constantly fixing its own offset, it may be asked why there is any error at all, even under transient temperature conditions. The answer is simple. The LTC1052 can only fix offsets inside its own nulling loop. There are many thermal junctions outside this loop that cannot be distinguished from legitimate signals.

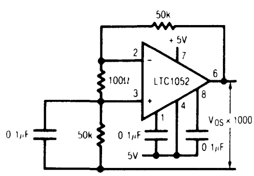


Figure 3. Offset Drift Test Circuit

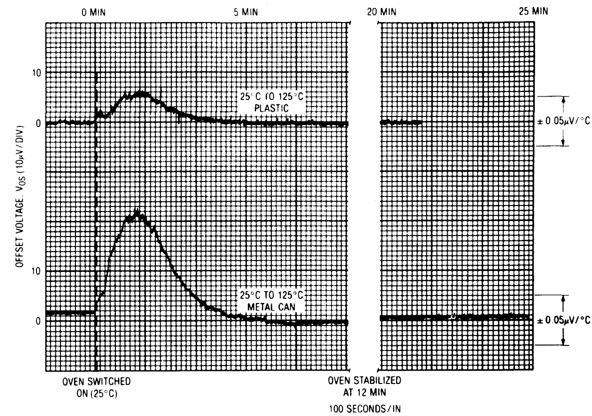


Figure 4. Transient Response of Offset Drift Test Circuit with 100°C Temperature Step

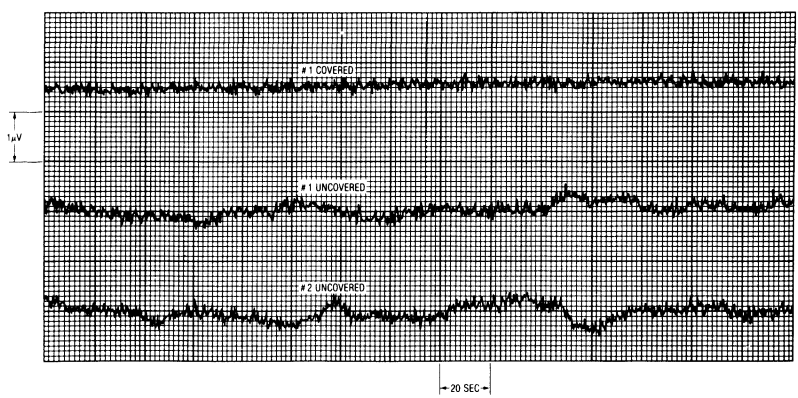


Figure 5. DC to 1Hz (Test Circuit TC3)

TEXAS INSTRUMENTS

APPLICATIONS INFORMATION

Some have been discussed previously, but the package thermal EMF effects are an important source of errors.

Notice the difference in the thermal response curves of Figure 4. This can only be attributed to the package since everything else is identical. In fact, the V_{OS} specification is set by the package-induced warm-up drift, not by the LTC1052. TO-99 metal cans exhibit the worst warm-up drift and Linear Technology sample tests TO-99 lots to minimize this problem.

Two things make 100% screening costly: (1) the extreme precision required on the LTC1052 and (2) the thermal time constant of the package is 0.5 to 3 minutes, depending on package type. The first precludes the use of automatic handling equipment and the second takes a long time. Bench test equipment is available to 100% test for warmed-up drift if offsets of less than $\pm 5\mu V$ are required.

CLOCK

The LTC1052 has an internal clock, setting the nominal sampling frequency at 330Hz. On 8-pin devices there is no way to control the clock externally. In some applications it may be desirable to control the sampling clock and this is the function of the 14-pin device.

CLK IN, CLK OUT and INT/$\overline{EXT}$ are provided to accomplish this. With no external connection, an internal pull-up holds INT/$\overline{EXT}$ at the V^+ supply and the 14-pin device self-oscillates at 330Hz. In this mode there is a signal on the CLK IN pin of 660Hz (2 times sampling frequency) with a 30% duty cycle. A divide-by-two drives the CLK OUT pin and sets the sampling frequency.

To use an external clock, connect INT/$\overline{EXT}$ to V^- and the external clock to CLK IN. The logic threshold of CLK IN is 2.5V below the positive supply. This allows CMOS logic to drive it directly with logic supplies of V^+ and ground. CLK IN can be driven from V^+ to V^- if desired. The duty cycle of the external clock is not particularly critical but should be kept between 30% and 60%.

Capacitance between CLK IN and CLK OUT (pins 13 and 12) can cause the divide-by-two circuit to malfunction. To avoid this, keep this capacitance below 5pF.

OUTPUT CLAMP

If the LTC1052 is driven into saturation, the nulling loop, attempting to force the differential input voltage to zero, will drive C_{EXTA} and C_{EXTB} to a supply rail. After the saturating drive is removed, the capacitors take a finite time to recover—this is the overload recovery time. The overload recovery is longest when the capacitors are driven to the negative rail (see Overload Recovery in typical performance section). The overload recovery time in this case is typically 225ms. In the opposite direction, i.e., C_{EXTA} and C_{EXTB} at positive rail, it is about ten times faster (25ms). The overload recovery time for the LTC1052 is much faster than competitive devices, but if a faster overload recovery time is necessary, the output clamp function can be used.

When the output clamp is connected to the negative input it prevents the amplifier from saturating and thus keeps C_{EXTA} and C_{EXTB} at their nominal voltages. The output clamp is a switch that turns on when the output gets to within approximately 1V of either supply rail. This switch is in parallel with the amplifier's feedback resistor and as the output moves closer to the rail, the switch on resistance decreases, reducing the closed loop gain. The output swing is reduced when the clamp function is used.

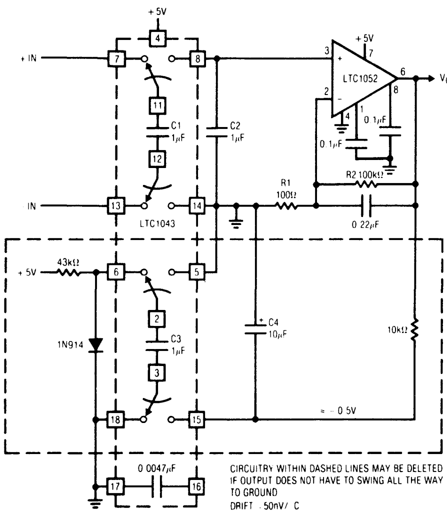
How much current the output clamp leaks when off is important because, when used, it is connected to the amplifier's negative input. Any current acts like input bias current and will degrade accuracy. At the other extreme, the maximum current the clamp conducts when on determines how much overdrive the clamp will take and still keep the amplifier from saturating.

LOW SUPPLY OPERATION

The minimum supply voltage for proper operation of the LTC1052 is typically 4.0V ($\pm$2.0V). In single supply applications, PSRR is guaranteed down to 4.7V ($\pm$2.35V). This assures proper operation down to the minimum TTL specified voltage of 4.75V.

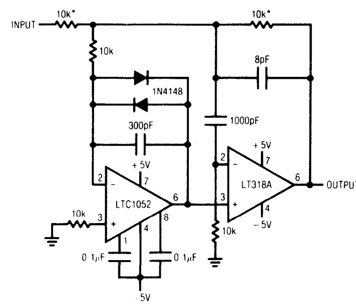
TYPICAL APPLICATIONS

5V Powered Ultra Precision Instrumentation Amplifier



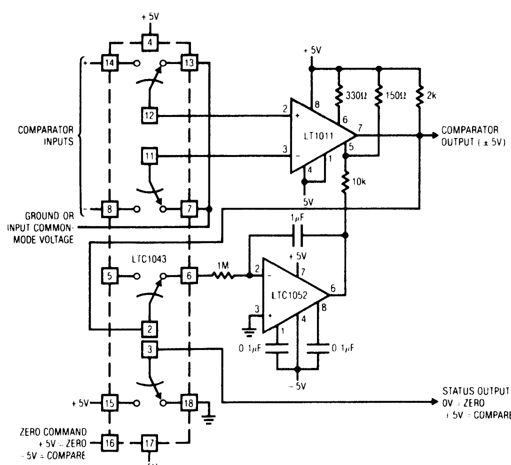
CIRCUITRY WITHIN DASHED LINES MAY BE DELETED IF OUTPUT DOES NOT HAVE TO SWING ALL THE WAY TO GROUND
DRIFT 50nV/°C
V_{OS} 3μV
GAIN $\frac{R2}{R1} + 1$
CMRR >120dB DC 20kHz
BANDWIDTH ≈ 10Hz

Fast Precision Inverter



*1% METAL FILM
FULL POWER BANDWIDTH = 2MHz
SLEW RATE = 40V/μs
SETTLING (10V STEP) = 12μs TO 0.01%
BIAS CURRENT DC = 30pA
OFFSET DRIFT = 50nV/°C
OFFSET VOLTAGE = 5μV

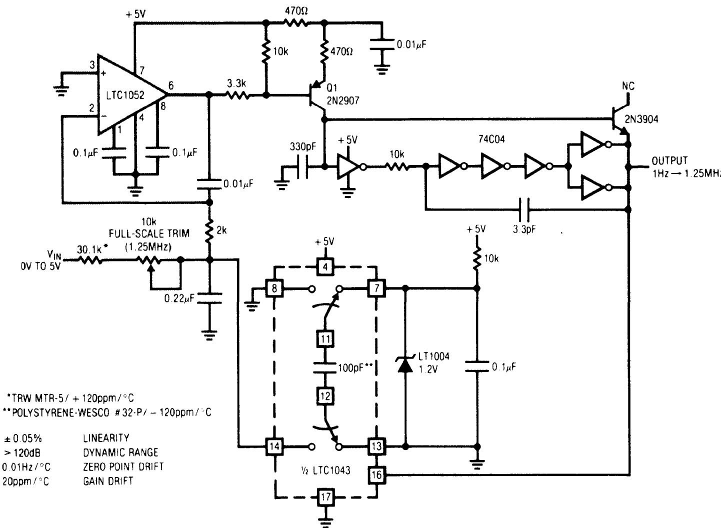
Offset Stabilized Comparator



TEXAS INSTRUMENTS

TYPICAL APPLICATIONS

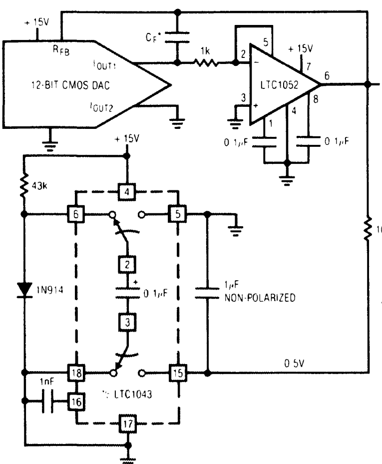
1Hz → 1.25MHz Voltage-to-Frequency Converter (+5V Supply)



*TRW MTR-5/ +120ppm/°C
**POLYSTYRENE-WESCO #32-P/ −120ppm/°C

±0.05%	LINEARITY
>120dB	DYNAMIC RANGE
0.01Hz/°C	ZERO POINT DRIFT
20ppm/°C	GAIN DRIFT

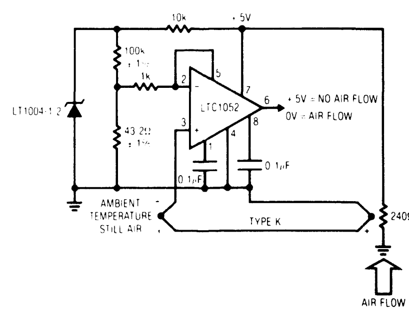
No V_{OS} Adjust* CMOS DAC Buffer—Single Supply



FOR HIGHER SPEED, SEE FAST PRECISION INVERTER UNDER TYPICAL APPLICATIONS

*OFFSET VOLTAGE CAUSES NONLINEARITY ERRORS. SEE "APPLICATION GUIDE TO CMOS MULTIPLYING D/A CONVERTERS" ANALOG DEVICES, INC

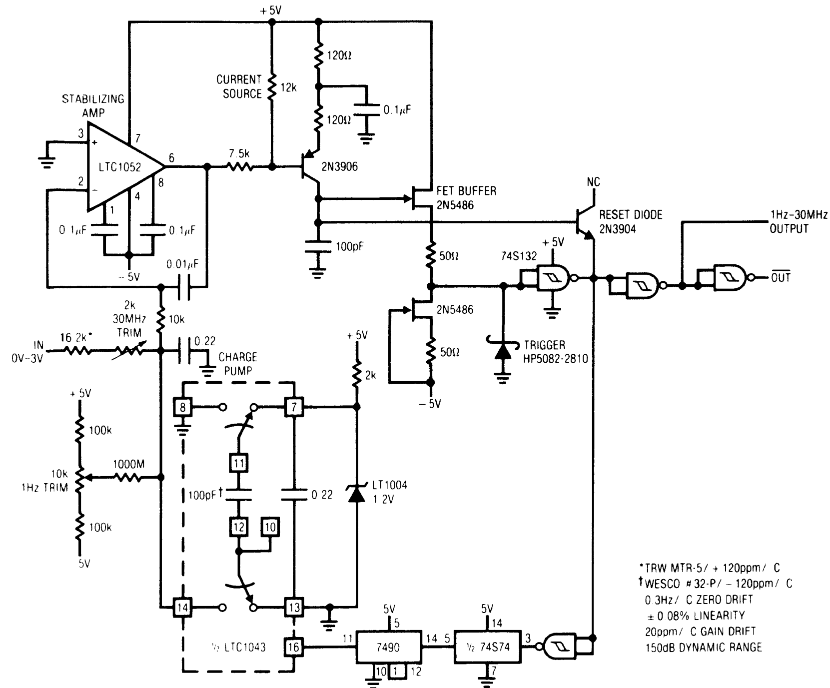
Air Flow Detector



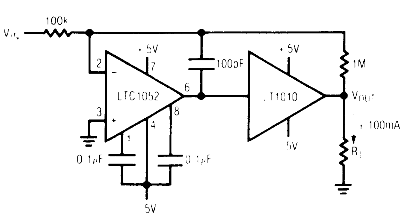
3 Operational Amplifiers

TYPICAL APPLICATIONS

1Hz → 30MHz Voltage-to-Frequency Converter

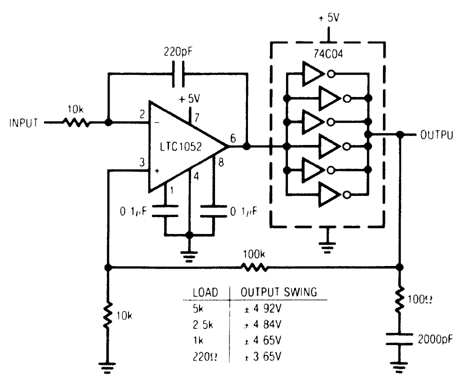


±100mA Output Drive



V_{OS} = 5μV
$V_{OS}/\Delta T$ = 50nV/°C
GAIN = 10
FULL POWER BANDWIDTH = 1kHz

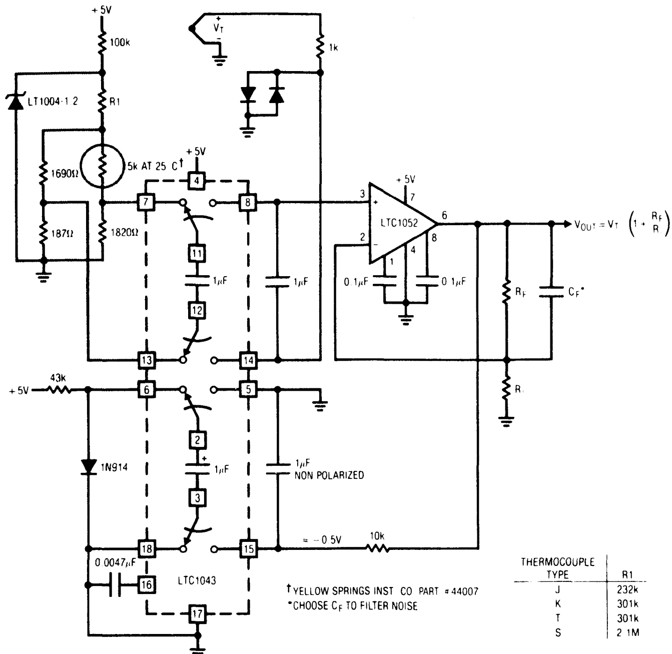
Increasing Output Current



LOAD	OUTPUT SWING
5k	± 4.92V
2.5k	± 4.84V
1k	± 4.65V
220Ω	± 3.65V

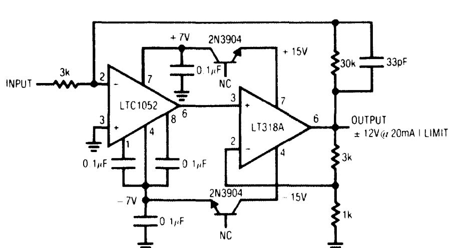
TYPICAL APPLICATIONS

Single +5V Thermocouple Amplifier with Cold Junction Compensation



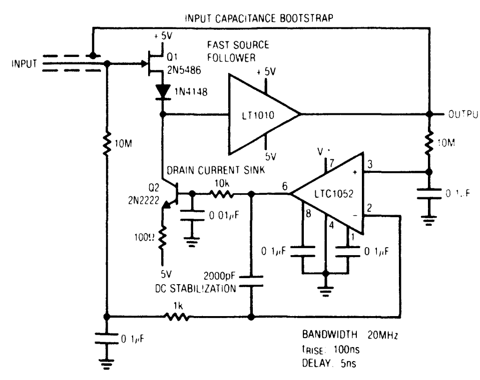
THERMOCOUPLE TYPE	R1
J	232k
K	301k
T	301k
S	2.1M

Increasing Output Current and Voltage ($V_{SUPPLY} = \pm 15V$)



STABLE FOR ALL GAINS, INVERTING AND NON-INVERTING. OBSERVE LTC1052 COMMON-MODE INPUT LIMITS

DC Stabilized FET Probe

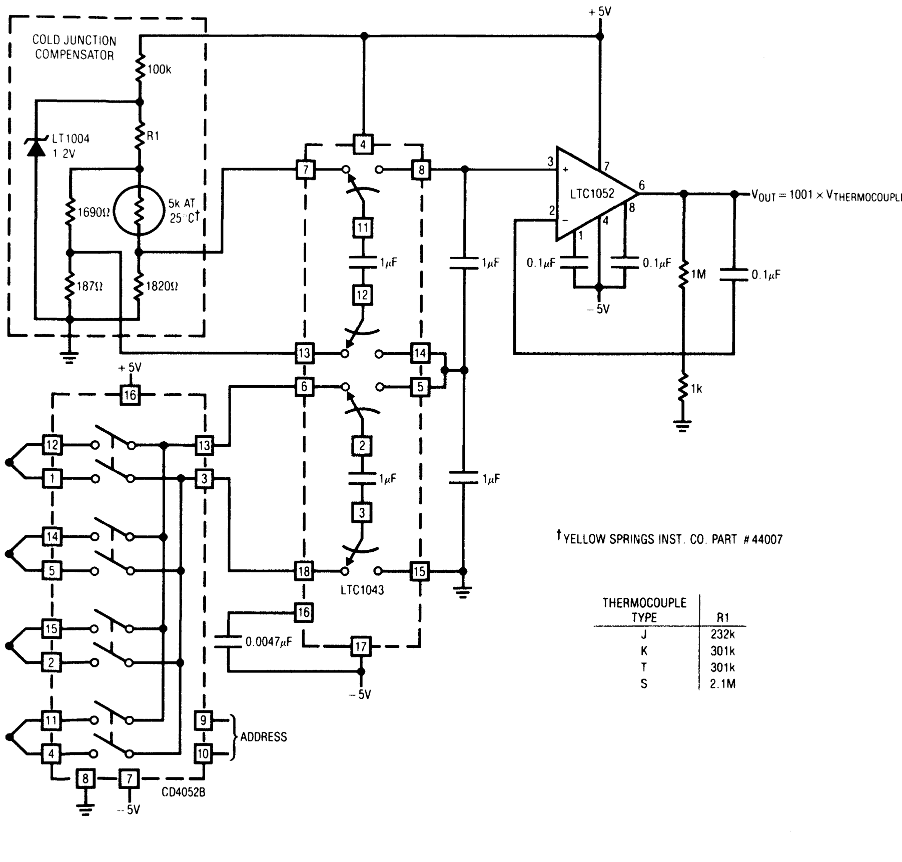


3

Operational Amplifiers

TYPICAL APPLICATIONS

Precision Multiplexed Differential Thermocouple Amplifier

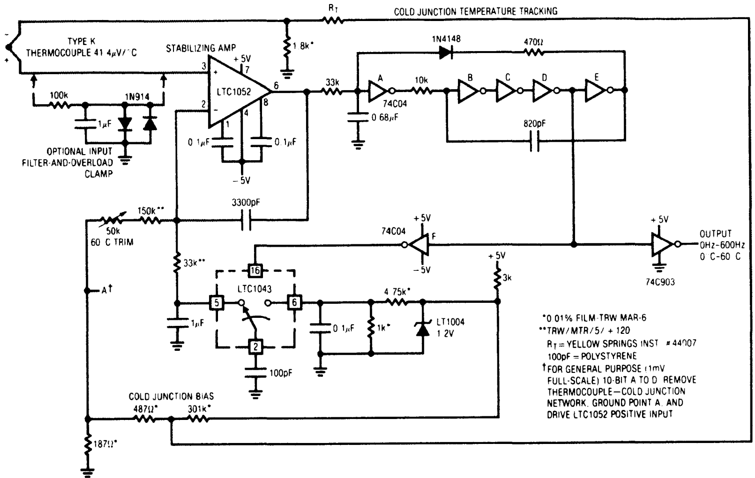


†YELLOW SPRINGS INST. CO. PART #44007

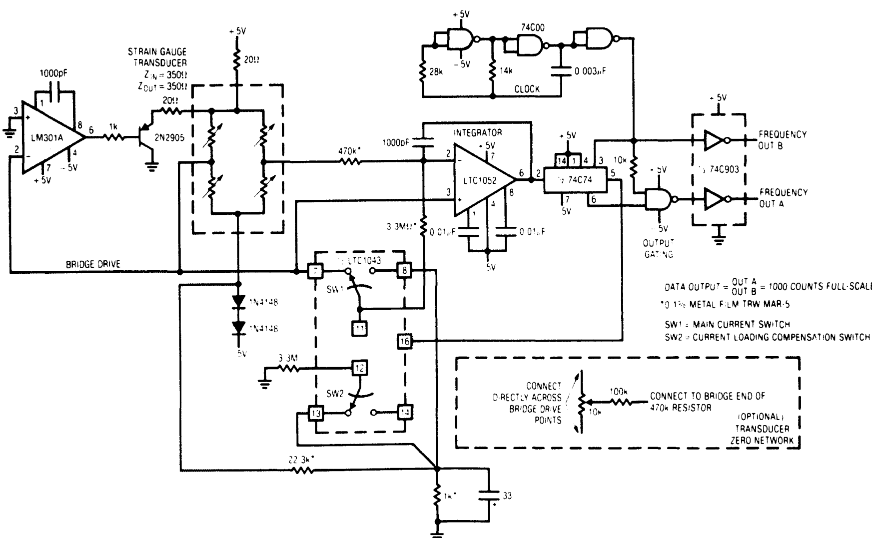
THERMOCOUPLE TYPE	R1
J	232k
K	301k
T	301k
S	2.1M

TYPICAL APPLICATIONS

Direct Thermocouple-to-Frequency Converter



Direct 10-Bit Strain Gauge Digitizer

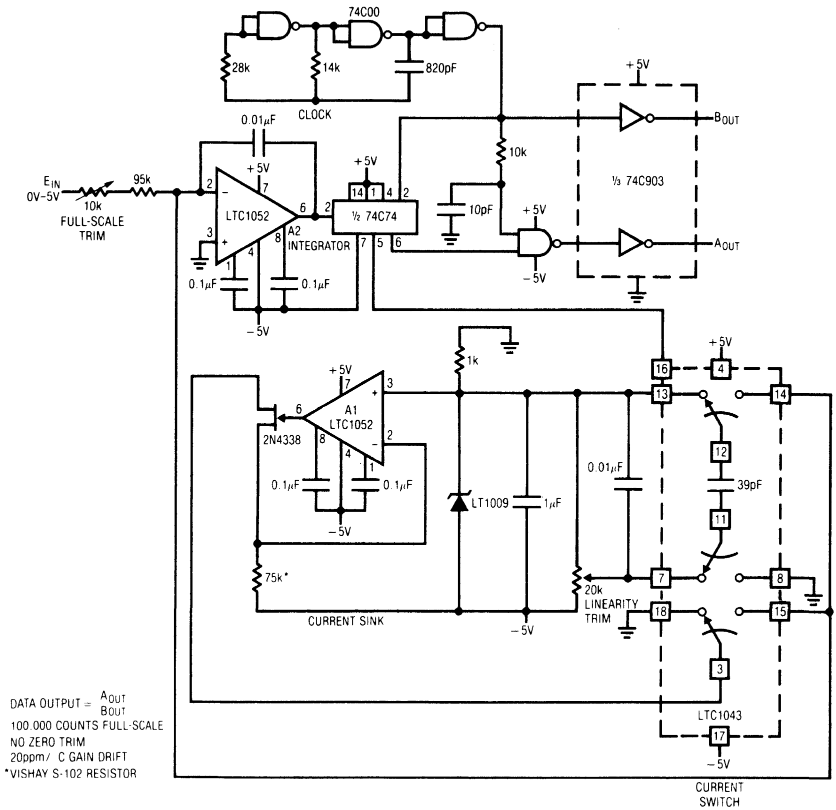


3

Operational Amplifiers

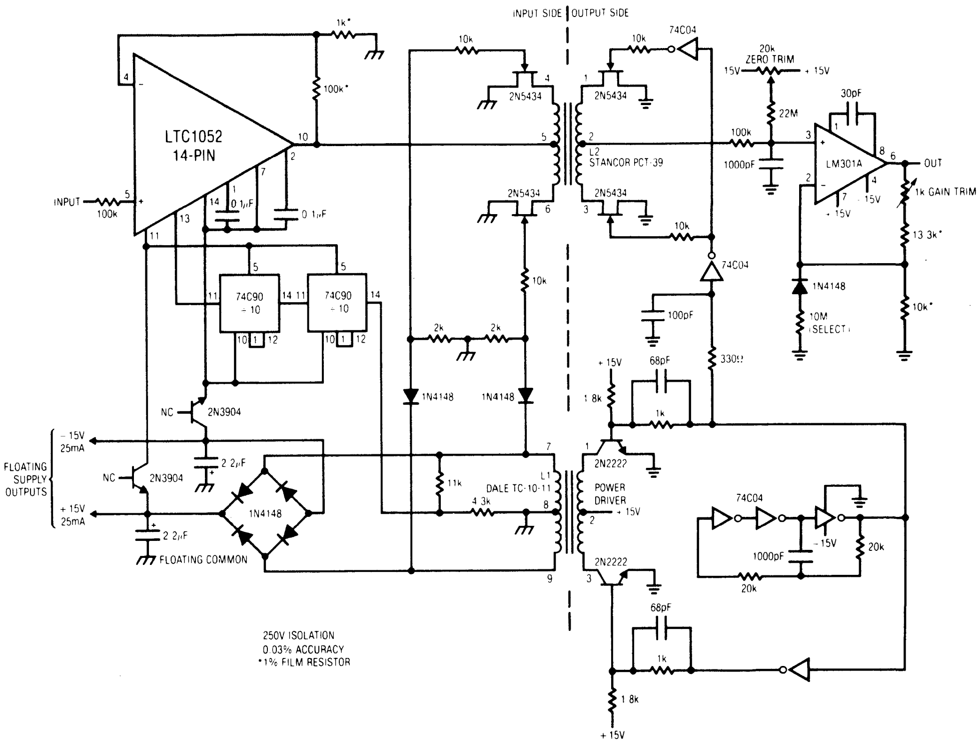
TYPICAL APPLICATIONS

16-Bit A → D Converter



TYPICAL APPLICATIONS

Precision Isolation Amplifier

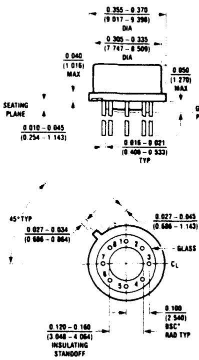


250V ISOLATION
0.03% ACCURACY
*1% FILM RESISTOR

PACKAGE DESCRIPTION

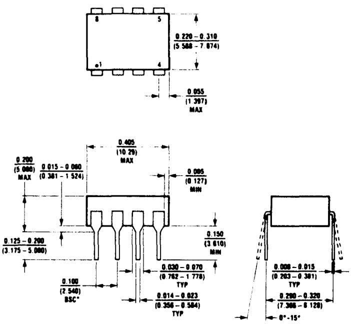
Dimensions in inches (millimeters) unless otherwise noted.

L Package
Metal Can



Tjmax	θjA	θjc
150°C	150°C/W	45°C/W

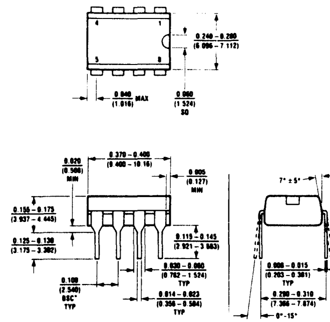
JG Package
8 Lead Hermetic Dip



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

Tjmax	θjA
150°C	100°C/W

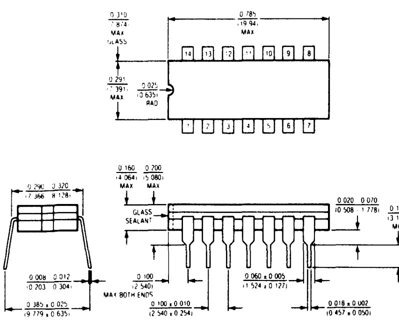
P Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

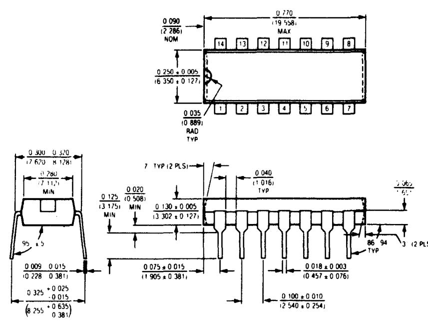
Tjmax	θjA
110°C	150°C/W

J Package
14-Lead Hermetic DIP



Tjmax	θjA
150°C	80°C/W

N Package
14-Lead Plastic



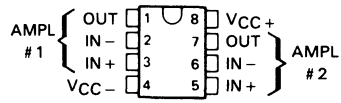
Tjmax	θjA
110°C	130°C/W

TYPES MC1558, MC1458
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

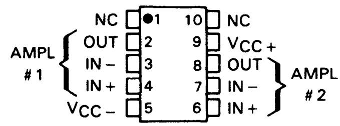
D972, FEBRUARY 1971—REVISED AUGUST 1983

- **Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-up**
- **Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558**

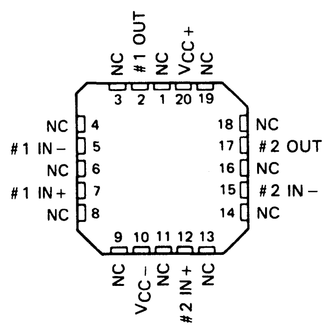
MC1558 . . . JG PACKAGE
MC1458 . . . D, JG, OR P PACKAGE
(TOP VIEW)



MC1558, MC1458 . . . U FLAT PACKAGE
(TOP VIEW)



MC1558 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

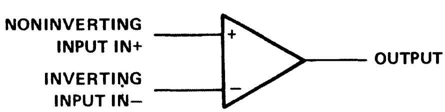
description

The MC1558 and MC1458 are dual general-purpose operational amplifiers with each half electrically similar to uA741 except that offset null capability is not provided.

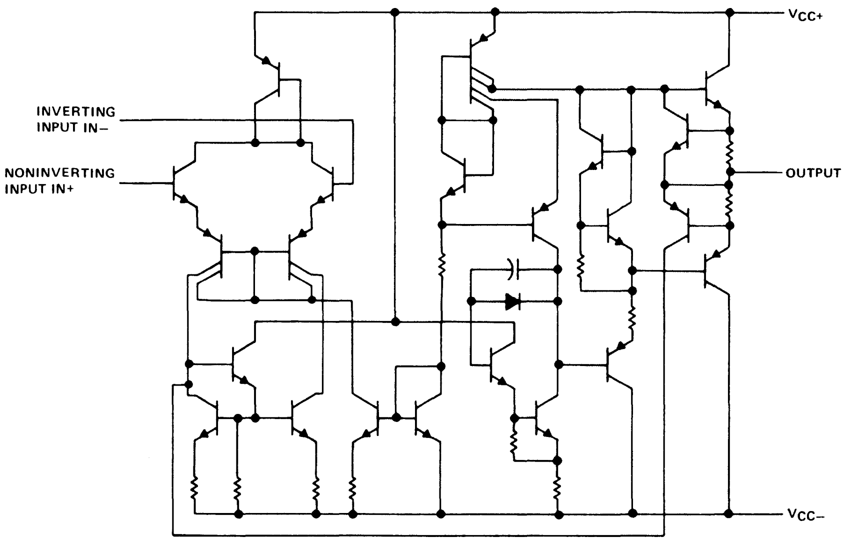
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The MC1558 is characterized for operation over the full military temperature range of −55°C to 125°C; the MC1458 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			MC1558	MC1458	UNIT
Supply voltage V_{CC+} (see Note 1)			22	18	V
Supply voltage V_{CC-} (see Note 1)			−22	−18	V
Differential input voltage (see Note 2)			±30	±30	V
Input voltage at either input (see Notes 1 and 3)			±15	±15	V
Duration of output short-circuit (see Note 4)			unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	Each amplifier		500	500	mW
	Total package	D, FK, JG, or P package	680	680	mW
		U package	675	675	mW
Operating free-air temperature range			−55 to 125	0 to 70	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FH, FK, JG or U package		300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package			260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG package, MC1558 chips are alloy mounted, MC1458 chips are glass mounted.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

	PARAMETER	TEST CONDITIONS†		MC1558 MIN	MC1558 TYP	MC1558 MAX	MC1458 MIN	MC1458 TYP	MC1458 MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	50	200		20	200		V/mV
			Full range	25			15			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	R_L = 2 kΩ, V_O ≥ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	A_{VD} = 1	25°C		65°			65°		
A_m	Gain margin		25°C		11			11		dB
r_i *	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0	25°C	70	90		70	90		dB
			Full Range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, V_O = 0	25°C		30	150		30	150	μV/V
			Full range			150			150	
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, R_S = 0, f = 1 kHz, BW = 1 Hz	25°C		45			45		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (both amplifiers)	No load, V_O = 0	25°C		3.4	5		3.4	5.6	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (both amplifiers)	No load, V_O = 0	25°C		100	150		100	170	mW
			Full range			200			200	
V_{o1}/V_{o2}	Crosstalk attenuation		25°C		120			120		dB

†All characteristics are specified under open-loop operating conditions with zero common-mode input voltage unless otherwise specified. Full range for MC1558 is −55°C to 125°C and for MC1458 is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

*For MC1558 this parameter is guaranteed but not tested.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MC1558			MC1458			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

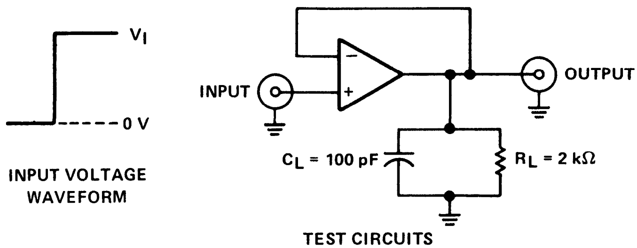


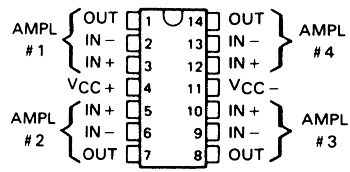
FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPES MC3503, MC3303, MC3403
QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

D2517, FEBRUARY 1979—REVISED SEPTEMBER 1983

- **Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Designed to be Interchangeable with Motorola MC3503, MC3303, MC3403**

MC3503 . . . J PACKAGE
MC3303, MC3403 . . . D, J, OR N PACKAGE
(TOP VIEW)

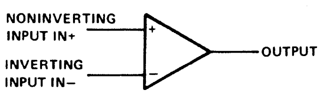


description

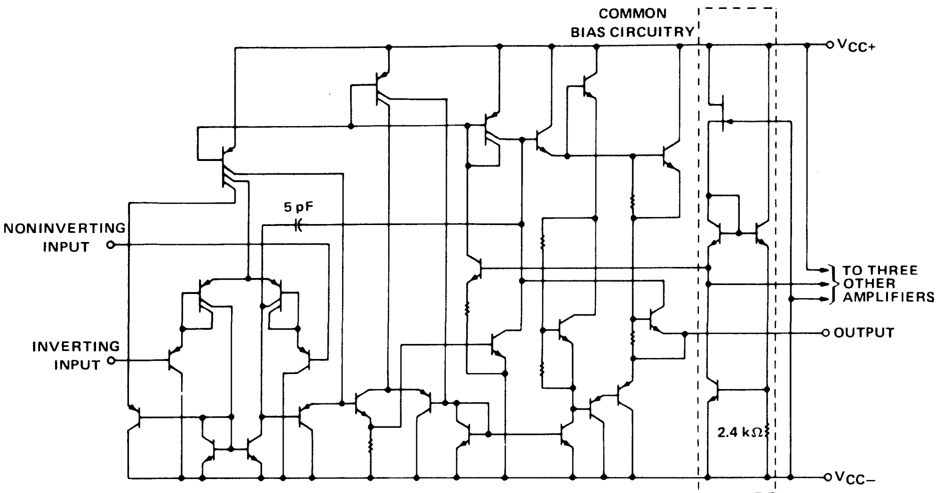
The MC3503, MC3303, and the MC3403 are quadruple operational amplifiers similar in performance to the uA741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 volts to 36 volts. Operation from split supplies is also possible provided the difference between the two supplies is 3 volts to 36 volts. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC} − 1.5 V. Quiescent supply currents are less than one-half those of the uA741.

The MC3503 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The MC3303 is characterized for operation from −40 °C to 85 °C, and the MC3403 is characterized for operation from 0° to 70°.

symbol (each amplifier)



schematic (each amplifier)



All component values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MC3503	MC3303	MC3403	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}		36	36	36	V
Differential input voltage (see Note 2)		±36	±36	±36	V
Input voltage (see Notes 1 and 3)		±18	±18	±18	V
Continuous total power dissipation at (or below) 25 °C free-air temperature (see Note 4)	D package		960	960	mW
	J package	1375	1025	1025	
	N package		875	875	
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. Neither input must ever be more positive then V_{CC+} or more negative than V_{CC-}.
4. For operation above 25 °C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, MC3503 chips are alloy mounted, MC3303 and MC3403 chips are glass mounted.

electrical characteristics at specified free-air temperature; $V_{CC+} = 14$ V, $V_{CC-} = 0$ V for MC3303; $V_{CC\pm} = \pm 15$ V for MC3403 and MC3503

PARAMETER		TEST CONDITIONS†		MC3503			MC3303			MC3403			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 5	25°C		2	5		2	8		2	10	mV
			Full range			6			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	See Note 5	Full range		10			10			10		μV/°C
I_{IO}	Input offset current	See Note 5	25°C		30	50		30	75		30	50	nA
			Full range			200			250			200	
α_{IIO}	Temperature coefficient of input offset current	See Note 5	Full range		50			50			50		pA/°C
I_{IB}	Input bias current	See Note 5	25°C		−0.2	−0.5		−0.2	−0.5		−0.2	−0.5	μA
			Full range			−1.5			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 13	V_{CC-} to 13.5		V_{CC-} to 12	V_{CC-} to 12.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±13.5		12	12.5		±12	±13.5		V
		$R_L = 2$ kΩ	25°C	±10	±13		10	12		±10	±13		
		$R_L = 2$ kΩ	Full range	±10			10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2$ kΩ	25°C	50	200		20	200		20	200		V/mV
			Full range	25			15			15			
B_{OM}	Maximum-output-swing bandwidth	$V_{OPP} = 20$ V, $A_{VD} = 1$, THD ≤ 5%, $R_L = 2$ kΩ	25°C		9			9			9		kHz
B_1	Unity-gain bandwidth	$V_O = 50$ mV, $R_L = 10$ kΩ	25°C		1			1			1		MHz
ϕ_m	Phase margin	$C_L = 200$ pF, $R_L = 2$ kΩ	25°C		60°			60°			60°		
r_i*	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75			75		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 2.5$ to ±15 V	25°C		30	150		30	150		30	150	μV/V
I_{OS}	Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	No load, See Note 5	25°C		2.8	4		2.8	7		2.8	7	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless other specified. Full range for T_A −55°C to 125°C for MC3503, −40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.

‡ The V_{ICR} limits are directly linked volt-for-volt to supply voltage, viz the positive limit is 2 volts less than V_{CC+}.

§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 5: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at $V_O = 0$ for MC3403 and MC3503, and $V_O = 7$ V for MC3303.

*For MC3503 this parameter is guaranteed but not tested.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MC3503			MC3303			MC3403			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V		2	5			10		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V		30	50			75		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V		−0.2	−0.5			−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	$V_{CC+}-1.7$			$V_{CC+}-1.7$			$V_{CC+}-1.7$			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	V_{CC} = ±15 V to ±2.5 V			150			150			150	μV/V
I_{CC}	Supply current	No load, V_O = 2.5 V		2.5	4		2.5	7		2.5	7	mA
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡Output will swing essentially to ground.

operating characteristics, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303; $V_{CC\pm}$ = ±15 V for MC3403 and MC3503; T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		0.6		V/μs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		μs
t_f	Fall time			0.35		μs
	Overshoot factor			20%		
	Crossover distortion	V_{IPP} = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

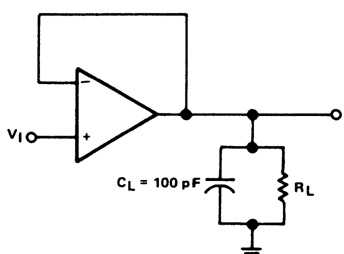


FIGURE 1—UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE AIR TEMPERATURE

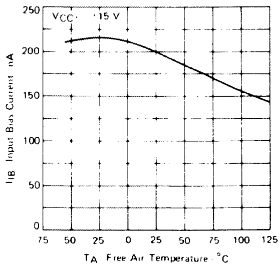


FIGURE 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

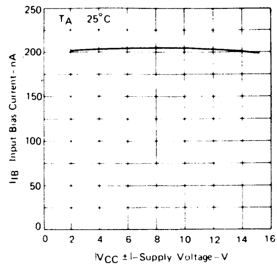


FIGURE 3

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

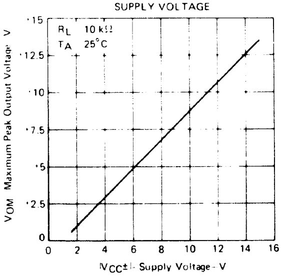


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

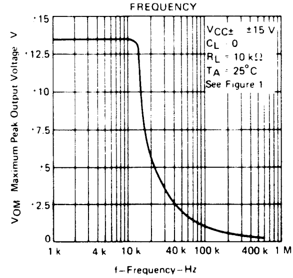


FIGURE 5

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

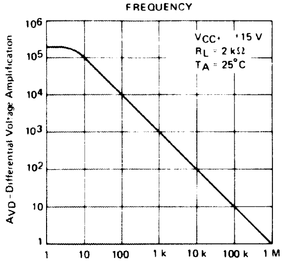


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

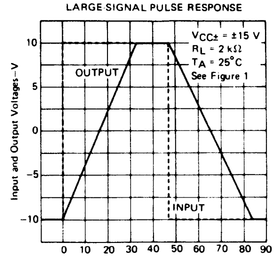


FIGURE 7

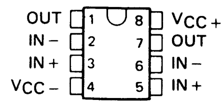
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPES NE5532, NE5532A
DUAL LOW-NOISE OPERATIONAL AMPLIFIERS

D2563, NOVEMBER 1979—REVISED AUGUST 1983

- **Equivalent Input Noise Voltage . . . . 5 nV/$\sqrt{Hz}$ Typ at 1 kHz**
- **Unity-Gain Bandwidth . . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio . . . . 100 dB Typ**
- **High DC Voltage Gain . . . . 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing . . . 32 V Typ with $V_{CC\pm}$ = ±18 V and R_L = 600 Ω**
- **High Slew Rate . . . . 9 V/μs Typ**
- **Wide Supply Voltage Range . . . ±3 V to ±22 V**
- **Designed to be Interchangeable with Signetics NE5532 and NE5532A**

NE5532, NE5532A . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

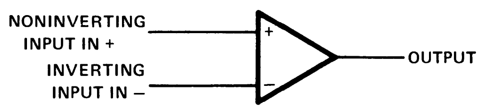


description

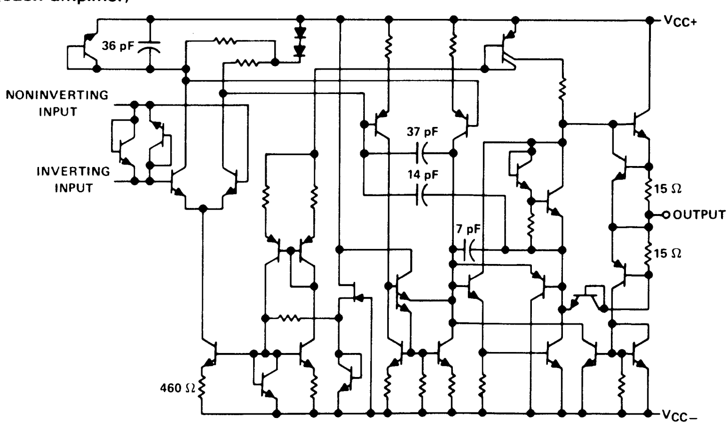
The NE5532 and NE5532A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are internally compensated for unity gain operation. The NE5532A has guaranteed maximum limits for equivalent input noise voltage.

The NE5532 and NE5532A are characterized for operation from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Input voltage, either input (see Notes 1 and 2)	$V_{CC\pm}$
Input current (see Note 3)	±10 mA
Duration of output short-circuit (see Note 4)	unlimited
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5):	
JG package	825 mW
P package	725 mW
Operating free-air temperature range: NE5532, NE5532A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in Section 2. In the JG package, chips are glass-mounted.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		NE5532, NE5532A MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	$T_A = 25°C$		0.5	4	mV
			$T_A = 0°C$ to $70°C$			5	
I_{IO}	Input offset current	$T_A = 25°C$			10	150	nA
		$T_A = 0°C$ to $70°C$				200	
I_{IB}	Input bias current	$T_A = 25°C$			200	800	nA
		$T_A = 0°C$ to $70°C$				1000	
V_{ICR}	Common-mode input voltage range			±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 600\ \Omega$	$V_{CC\pm}$ ±15 V	24	26		V
			$V_{CC\pm} = \pm 18$ V	30	32		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 600\ \Omega$, $V_O = \pm 10$ V	$T_A = 25°C$	15	50		V/mV
			$T_A = 0°C$ to $70°C$	10			
		$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	$T_A = 25°C$	25	100		
			$T_A = 0°C$ to $70°C$	15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz			2.2		V/mV
B_{OM}	Maximum-output-swing bandwidth	$R_L = 600\ \Omega$, $V_O = \pm 10$ V			140		kHz
		$R_L = 600\ \Omega$, $V_{CC\pm} = \pm 18$ V, $V_O = \pm 14$ V			100		
B_1	Unity-gain bandwidth	$R_L = 600\ \Omega$, $C_L = 100$ pF			10		MHz
r_i	Input resistance			30	300		kΩ
z_o	Output impedance	$A_{VD} = 30$ dB, $R_L = 600\ \Omega$, f = 10 kHz			0.3		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\,min}$		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$		80	100		dB
I_{OS}	Output short-circuit current				38		mA
I_{CC}	Total supply current	No load, $V_O = 0$			8	16	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$V_{o1} = 10$ V peak, f = 1 kHz			110		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	NE5532 MIN	TYP	MAX	NE5532A MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain			9			9		V/μs
	Overshoot factor	$V_I = 100$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_L = 100$ pF		10%			10%		
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	nV/√Hz
		f = 1 kHz		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		pA/√Hz
		f = 1 kHz		0.7			0.7		

3

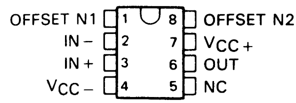
Operational Amplifiers

TYPES OP-07C, OP-07D, OP-07E
ULTRA-LOW-OFFSET-VOLTAGE OPERATIONAL AMPLIFIERS

D2757, OCTOBER 1983

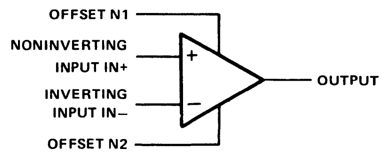
- Ultra-Low Offset Voltage . . . 30 μV Typ (OP-07E)
- Ultra-Low Offset Voltage Temperature Coefficient . . . 0.3 μV/°C Typ (OP-07E)
- Ultra-Low Noise
- No External Components Required
- Replaces Chopper Amplifiers at a Lower Cost
- Single-Chip Monolithic Fabrication
- Wide Input Voltage Range 0 to ±14 V Typ
- Wide Supply Voltage Range ±3 V to ±18 V
- Essentially Equivalent to Fairchild μA714 Operational Amplifiers
- Direct Replacement for PMI OP-07C, OP-07D, OP-07E

D, JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

symbol

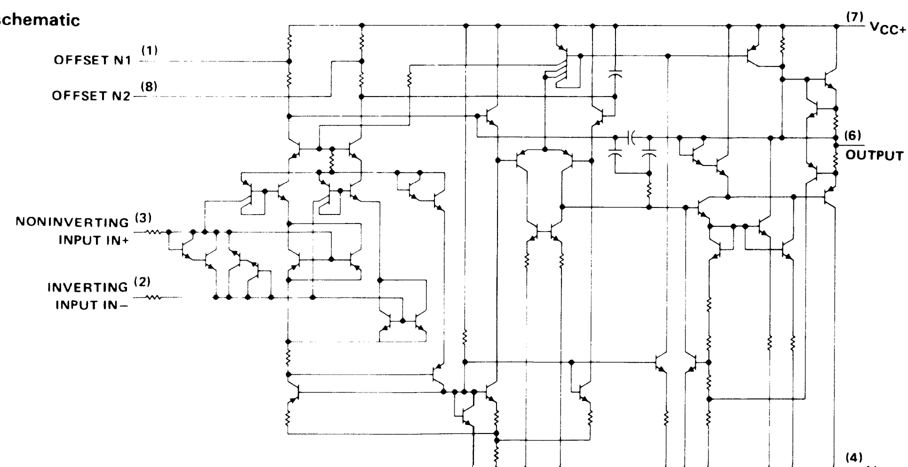


description

These devices represent a breakthrough in operational amplifier performance. Low offset and long-term stability are achieved by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, no external components are required for offset nulling and frequency compensation. The true differential input, with a wide input voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP-07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

These devices are characterized for operation from 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	22 V
Supply voltage V_{CC-}	−22 V
Differential input voltage (see Note 2)	±30 V
Input voltage (either input, see Note 3)	±22 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the JG package, these chips are glass-mounted.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		OP-7C MIN	OP-7C TYP	OP-7C MAX	OP-7D MIN	OP-7D TYP	OP-7D MAX	OP-7E MIN	OP-7E TYP	OP-7E MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		60	150		60	150		30	75	μV
			0°C to 70°C		85	250		85	250		45	130	
α_{VIO}*	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	0°C to 70°C		0.5	1.8		0.7	2.5		0.3	1.3	μV/°C
	Long-term drift of input offset voltage	See Note 6			0.4			0.5			0.3		μV/mo
	Offset adjustment range	$R_S = 20\ k\Omega$, See Figure 1	25°C		±4			±4			±4		mV
I_{IO}	Input offset current		25°C		0.8	6		0.8	6		0.5	3.8	nA
			0°C to 70°C		1.6	8		1.6	8		0.9	5.3	
α_{IIO}	Temperature coefficient of input offset current		0°C to 70°C		12	50		12	50		8	35	pA/°C
I_{IB}	Input bias current		25°C		±1.8	±7		±2	±12		±1.2	±4	nA
			0°C to 70°C		±2.2	±9		±3	±14		±1.5	±5.5	
α_{IIB}*	Temperature coefficient of input bias current		0°C to 70°C		18	50		18	50		13	35	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	±13	±14		±13	±14		±13	±14		V
			0°C to 70°C	±13	±13.5		±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	$R_L \geq 10\ k\Omega$	25°C	±12	±13		±12	±13		±12.5	±13		V
		$R_L \geq 2\ k\Omega$	25°C	±11.5	±12.8		±11.5	±12.8		±12	±12.8		
		$R_L \geq 1\ k\Omega$	25°C		±12			±12		±10.5	±12		
		$R_L \geq 2\ k\Omega$	0°C to 70°C	±11	±12.6		±11	±12.6		±12	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 3$ V, $V_O = \pm 0.5$ V, $R_L \geq 500\ k\Omega$	25°C	100	400			400		150	400		V/mV
		$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	25°C	120	400		120	400		200	500		
			0°C to 70°C	100	400		100	400		180	450		
B_1*	Unity gain bandwidth		25°C	0.4	0.6		0.4	0.6		0.4	0.6		MHz
r_i*	Input resistance		25°C	8	33		7	31		15	50		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 13$ V, $R_S = 50\ \Omega$	25°C	100	120		94	110		106	123		dB
			0°C to 70°C	97	120		94	106		103	123		
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm 3$ V to ± 18 V, $R_S = 50\ \Omega$	25°C		7	32		7	32		5	20	μV/V
			0°C to 70°C		10	51		10	51		7	32	
P_D	Power dissipation	$V_O = 0$, No load	25°C		80	150		80	150		75	120	mW
		$V_{CC\pm} = \pm 3$ V, $V_O = 0$, No load	25°C		4	8		4	8		4	6	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

*These parameters are guaranteed but not tested.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		OP-7C			OP-7D			OP-7E			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_n	Equivalent input noise voltage	$T_A = 25°C$	f = 10 Hz		10.5	20		10.5	20		10.3	18	nV/√Hz
			f = 100 Hz		10.2	13.5		10.3	13.5		10.0	13	
			f = 1 kHz		9.8	11.5		9.8	11.5		9.6	11	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, $T_A = 25°C$			0.38	0.65		0.38	0.65		0.35	0.6	μV
I_n	Equivalent input noise current	$T_A = 25°C$	f = 10 Hz		0.35	0.9		0.35	0.9		0.32	0.8	pA/√Hz
			f = 100 Hz		0.15	0.27		0.15	0.27		0.14	0.23	
			f = 1 kHz		0.13	0.18		0.13	0.18		0.12	0.17	
I_{NPP}	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz, $T_A = 25°C$			15	35		15	35		14	30	pA
SR	Slew rate	$R_L \geq 2$ kΩ, $T_A = 25°C$		0.1	0.3		0.1	0.3		0.1	0.3		V/μs

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

3

Operational Amplifiers

TYPICAL APPLICATION DATA

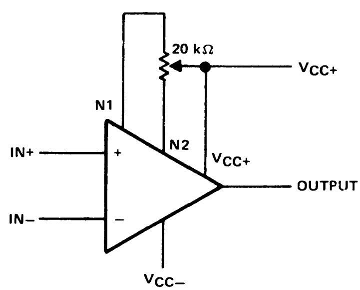


FIGURE 1—INPUT OFFSET VOLTAGE NULL CIRCUIT

MAY 1987

FEATURES

- $3.8nV/\sqrt{Hz}$ *max* 1kHz Noise
- $5.5nV/\sqrt{Hz}$ *max* 10Hz Noise
- Very Low Peak-to-Peak Noise, 80nV Typical
- $25\mu V$ *max* Offset Voltage
- $0.6\mu V/°C$ *max* Drift with Temperature
- $11V/\mu sec$ *min* Slew Rate (OP-37)
- 1 Million *min* Voltage Gain

APPLICATIONS

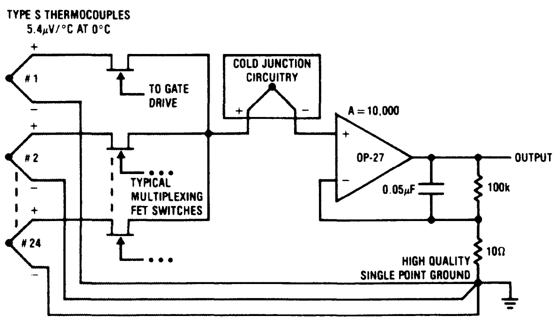
- Low Level Transducer Amplifiers
- Precision Threshold Detectors
- Tape Head Preamplifiers
- Microphone Preamplifiers
- Direct Coupled Audio Gain Stages

DESCRIPTION

The OP-27/OP-37 series of operational amplifiers combine outstanding noise performance with excellent precision and high speed specifications. The wideband noise is only $3nV/\sqrt{Hz}$, and with the 1/f noise corner at 2.7Hz, low noise is maintained for all low frequency instrumentation applications. Precision DC specifications match or exceed the best available op amps: offset voltage is $10\mu V$, drift with temperature and time are $0.2\mu V/°C$ and $0.2\mu V$/month, respectively; common mode rejection is 126dB, voltage gain is two million. The unity gain compensated OP-27 is an order of magnitude faster than other precision op amps. The decompensated OP-37 is even faster at a gain-bandwidth product of 63MHz and $17V/\mu sec$ slew rate. These characteristics plus Linear Technology's advanced process and test techniques make the OP-27/37 an excellent choice for performance and reliability in all low noise, precision amplifier applications. In addition, Linear's OP-37 is completely latch-up free in high gain, large capacitive feedback configurations. The accurate, microvolt, low noise signal handling capabilities of the OP-27/37 are taken advantage of in the multiplexed thermocouple application shown.

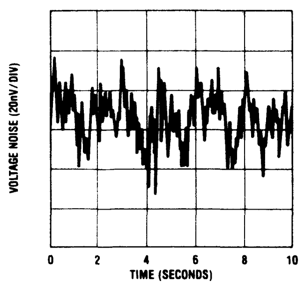
For applications requiring higher performance, see the LT1007 and LT1037 data sheets.

Low Noise, Multiplexed Thermocouple Amplifier



If 24 channels are multiplexed per second, and the output is required to settle to 0.1% accuracy, the amplifier's bandwidth cannot be limited to less than 30Hz. Yet the noise contribution of the OP-27 will still be only $0.11\mu Vp\text{-}p$, which is equivalent to an error of only 0.02°C.

0.1Hz to 10Hz Noise



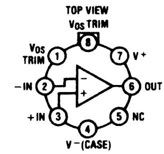
ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

TEXAS INSTRUMENTS

ABSOLUTE MAXIMUM RATINGS

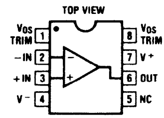
Supply Voltage . . . . ± 22V
Internal Power Dissipation 500mW
Input Voltage . . . . Equal to Supply Voltage
Output Short Circuit Duration . . . . Indefinite
Differential Input Current (Note 8) . . . . ± 25mA
Lead Temperature (Soldering, 10 sec.) . . . . 300°C
Operating Temperature Range
  OP-27/OP-37 A, C . . . . −55°C to 125°C
  OP-27/OP-37 E, G . . . . −25°C to 85°C
Junction Temperature Range
  OP-27/OP-37 A, C . . . . −55°C to 150°C
  OP-27/OP-37 E, G . . . . −25°C to 125°C
Storage Temperature Range
  OP-27/OP-37 A, C, E, G . . . . −65°C to 150°C

PACKAGE/ORDER INFORMATION



METAL CAN L PACKAGE

ORDER PART NUMBER	
OP-27AL	OP-37AL
OP-27CL	OP-37CL
OP-27EL	OP-37EL
OP-27GL	OP-37GL



HERMETIC DIP JG PACKAGE
PLASTIC DIP P PACKAGE

ORDER PART NUMBER	
OP-27AJG	OP-37EJG
OP-27CJG	OP-37GJG
OP-27EJG	OP-27EP
OP-27GJG	OP-27GP
OP-37AJG	OP-37EP
OP-37CJG	OP-37GP

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-27A,E/OP-37A,E MIN	TYP	MAX	OP-27C,G/OP-37C,G MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	25		30	100	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Offset Voltage Stability	(Note 2)		0.2	1.0		0.4	2.0	μV/Mo
I_{OS}	Input Offset Current			7	35		12	75	nA
I_B	Input Bias Current			± 10	± 40		± 15	± 80	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 3 and 5)		0.08	0.18		0.09	0.25	μVp-p
	Input Noise Voltage Density	f_o = 10Hz (Note 3) f_o = 30Hz (Note 3) f_o = 1000Hz (Note 3)		3.5 3.1 3.0	5.5 4.5 3.8		3.8 3.3 3.2	8.0 5.6 4.5	nV/√Hz nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_o = 10Hz (Notes 3 and 6) f_o = 30Hz (Notes 3 and 6) f_o = 1000Hz (Notes 3 and 6)		1.7 1.0 0.4	4.0 2.3 0.6		1.7 1.0 0.4	 0.6	pA/√Hz pA/√Hz pA/√Hz
	Input Resistance—Common Mode			3			2		GΩ
	Input Voltage Range		± 11.0	± 12.3		± 11.0	± 12.3		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ± 11V	114	126		100	120		dB
PSRR	Power Supply Rejection Ratio	V_S = ± 4V to ± 18V	100	120		94	118		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ± 10V $R_L \geq 1k\Omega$, V_O = ± 10V $R_L = 600\Omega$, V_O = ± 1V V_S = ± 4V (Note 4)	1000 800 250	1800 1500 700		700 200	1500 1500 500		V/mV V/mV V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	± 12.0 ± 10.0	± 13.8 ± 11.5		± 11.5 ± 10.0	± 13.5 ± 11.5		V V
SR	Slew Rate OP-27 OP-37	$R_L \geq 2k\Omega$ (Note 4) $A_{VCL} \geq 5$ (Note 4)	1.7 11	2.8 17		1.7 11	2.8 17		V/μs V/μs
GBW	Gain-Bandwidth Product OP-27 OP-37	f_o = 100kHz (Note 4) f_o = 10kHz (Note 4) f_o = 1MHz ($A_{VCL} \geq 5$)	5.0 45	8.0 63 40		5.0 45	8.0 63 40		MHz MHz MHz
Z_O	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		70			70		Ω
P_d	Power Dissipation			90	140		100	170	mW

TEXAS INSTRUMENTS

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-27A/OP-37A MIN	TYP	MAX	OP-27C/OP-37C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	60		70	300	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.6		0.4	1.8	μV/°C
I_{OS}	Input Offset Current		●		15	50		30	135	nA
I_B	Input Bias Current		●		±20	±60		±35	±150	nA
	Input Voltage Range		●	±10.3	±11.5		±10.2	±11.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	108	122		94	116		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	96	116		86	110		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	600	1200		300	800		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±11.5	±13.5		±10.5	±13.0		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-25°C \leq T_A \leq 85°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-27E/OP-37E MIN	TYP	MAX	OP-27G/OP-37G MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		20	50		55	220	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.6		0.4	1.8	μV/°C
I_{OS}	Input Offset Current		●		10	50		20	135	nA
I_B	Input Bias Current		●		±14	±60		±25	±150	nA
	Input Voltage Range		●	±10.5	±11.8		±10.5	±11.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	110	124		96	118		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	97	118		90	114		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	750	1500		450	1000		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±11.7	±13.6		±11.0	±13.3		V

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV—refer to typical performance curve.

Note 3: Sample tested. Contact factory for 100% testing of 10Hz voltage noise.

Note 4: Parameter is guaranteed by design and is not tested.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester in Applications Information section.

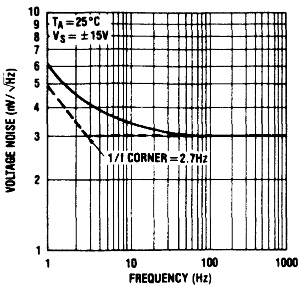
Note 6: See test circuit for current noise measurement in Applications Information section.

Note 7: The Average Input Offset Drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ.

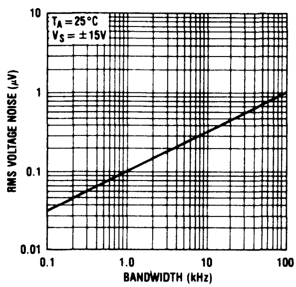
Note 8: The OP-27/37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

TYPICAL PERFORMANCE CHARACTERISTICS

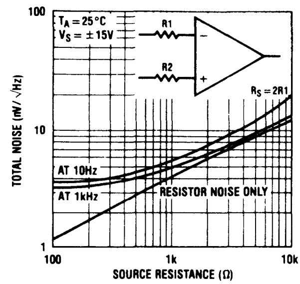
Voltage Noise vs Frequency



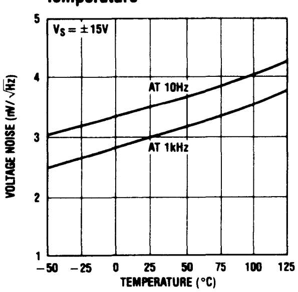
Input Wideband Voltage Noise vs Bandwidth (0.1Hz to Frequency Indicated)



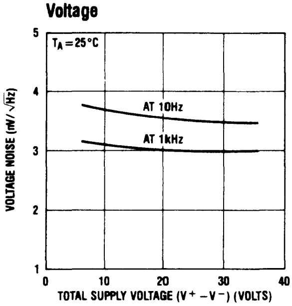
Total Noise vs Source Resistance



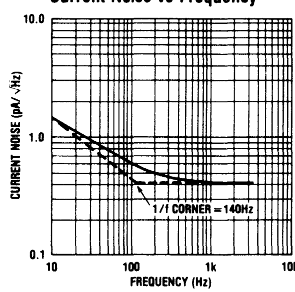
Voltage Noise vs Temperature



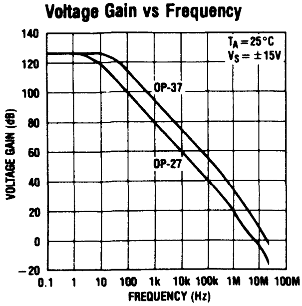
Voltage Noise vs Supply Voltage



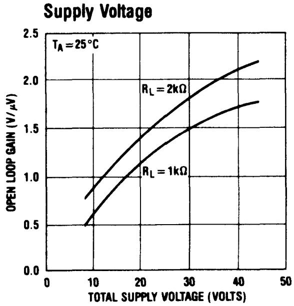
Current Noise vs Frequency



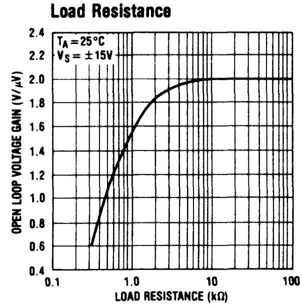
Voltage Gain vs Frequency



Open Loop Voltage Gain vs Supply Voltage

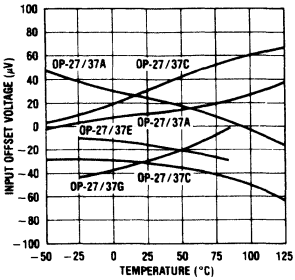


Open Loop Voltage Gain vs Load Resistance

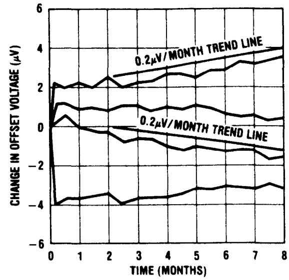


TYPICAL PERFORMANCE CHARACTERISTICS

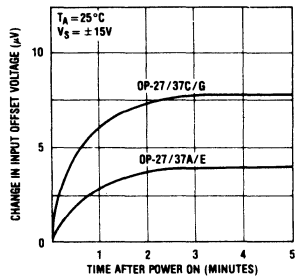
Offset Voltage Drift of Representative Units



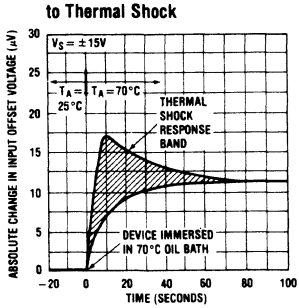
Long Term Drift of Representative Units



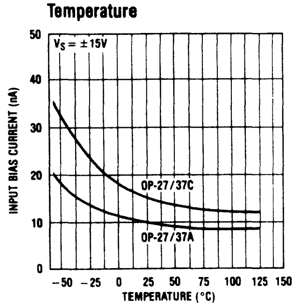
Warm-Up Drift



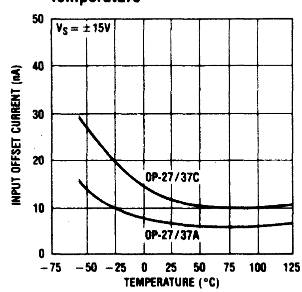
Offset Voltage Change Due to Thermal Shock



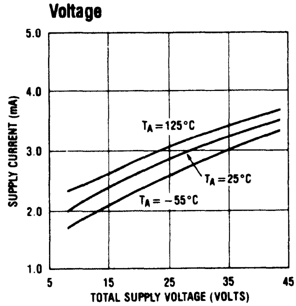
Input Bias Current vs Temperature



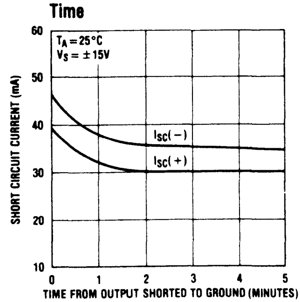
Input Offset Current vs Temperature



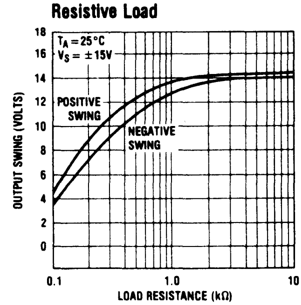
Supply Current vs Supply Voltage



Short Circuit Current vs Time

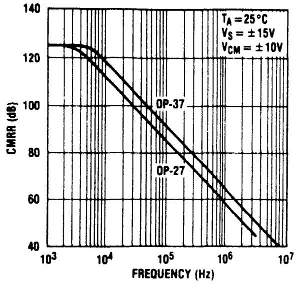


Maximum Output Swing vs Resistive Load

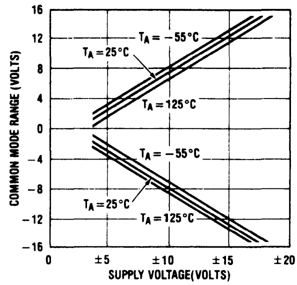


TYPICAL PERFORMANCE CHARACTERISTICS

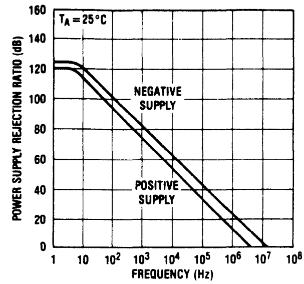
Common Mode Rejection vs Frequency



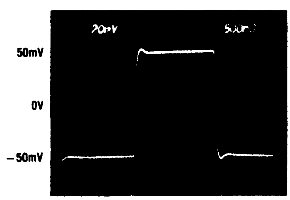
Common Mode Input Range vs Supply Voltage



PSRR vs Frequency

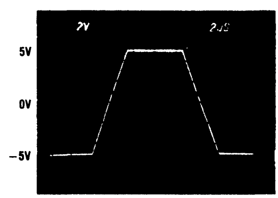


OP-27 Small Signal Transient Response



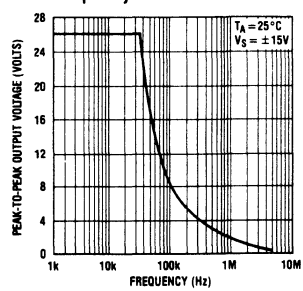
$A_{VCL} = +1$, $V_S = \pm 15V$
$C_L = 15pF$

OP-27 Large Signal Transient Response

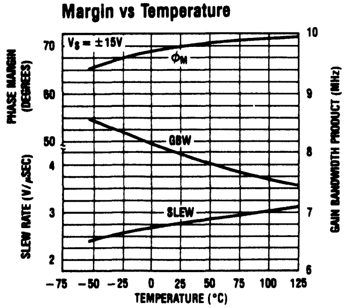


$A_{VCL} = -1$, $V_S = \pm 15V$

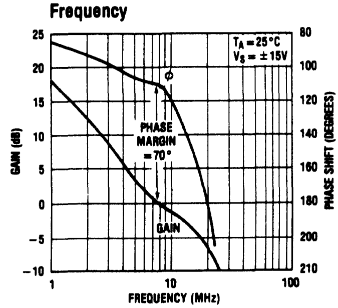
OP-27 Maximum Undistorted Output vs Frequency



OP-27 Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature

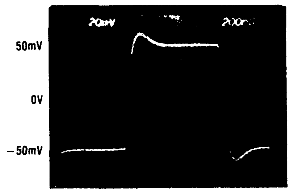


OP-27 Gain, Phase Shift vs Frequency



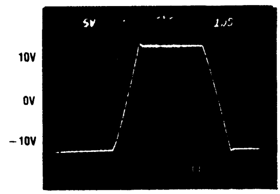
TYPICAL PERFORMANCE CHARACTERISTICS

OP-37 Small Signal Transient Response



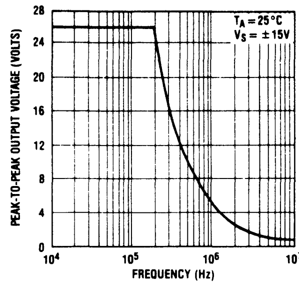
$A_{VCL} = +5$, $V_S = \pm 15V$
$C_L = 15pF$

OP-37 Large Signal Response

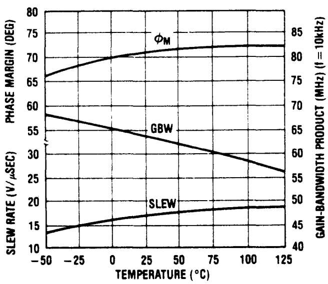


$A_{VCL} = +5$, $V_S = \pm 15V$

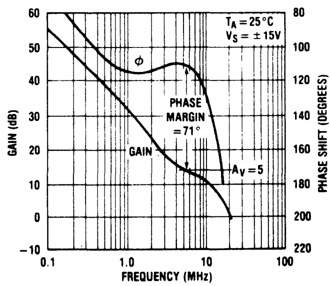
OP-37 Maximum Undistorted Output vs Frequency



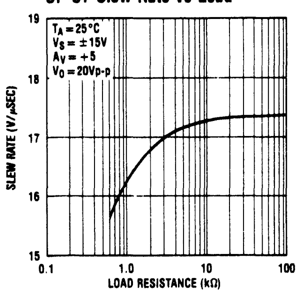
OP-37 Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature



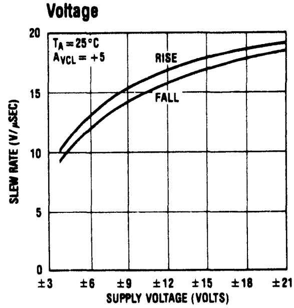
OP-37 Gain, Phase Shift vs Frequency



OP-37 Slew Rate vs Load



OP-37 Slew Rate vs Supply Voltage



APPLICATIONS INFORMATION

General

The OP-27/37 series devices may be inserted directly into OP-07, OP-05, 725, and 5534 sockets with or without removal of external compensation or nulling components. In addition, the OP-27/37 may be fitted to 741 sockets with the removal or modification of external nulling components.

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the OP-27/OP-37 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 80nV peak-to-peak noise performance of the OP-27/37 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

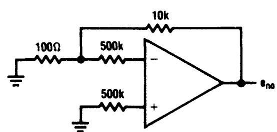
(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also ''feedthrough'' to increase the observed noise.

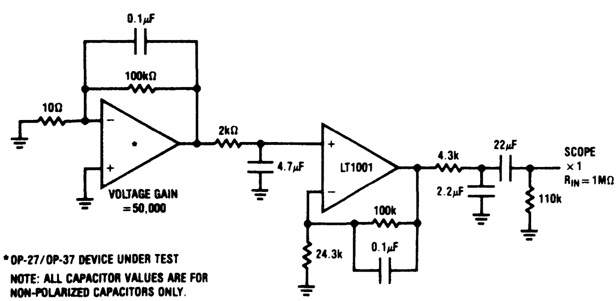
A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured and calculated by the following formula:

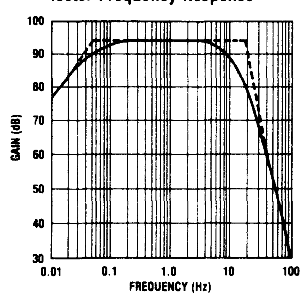
$$i_n = \frac{\left[e^2_{no} - (130\text{nV})^2\right]^{1/2}}{1\text{M}\Omega \times 100}$$



0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz p-p Noise Tester Frequency Response



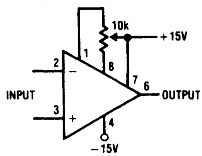
TEXAS INSTRUMENTS

APPLICATIONS INFORMATION

Offset Voltage Adjustment

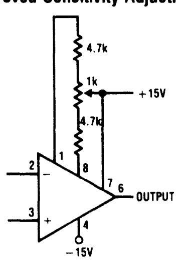
The input offset voltage of the OP-27/37, and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 10k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C.

Standard Adjustment



The adjustment range with a 10k pot is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of ±200μV.

Improved Sensitivity Adjustment

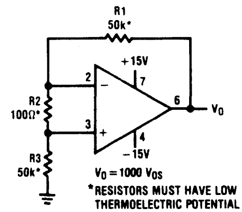


Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

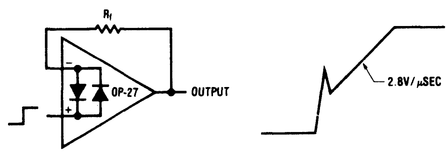
The circuit shown to measure offset voltage is also used as the burn-in configuration for the OP-27/37, with the supply voltages increased to ±20V, R1 = R3 = 10k, R2 = 200Ω, A_V = 100.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



Unity Gain Buffer Applications (OP-27 Only)

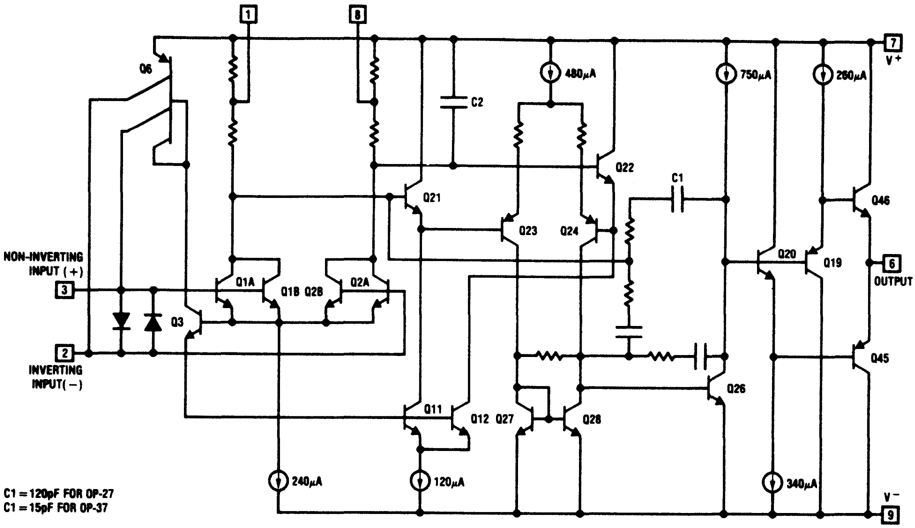
When $R_f \le 100\Omega$ and the input is driven with a fast, large signal pulse (> 1V), the output waveform will look as shown in the pulsed operation diagram.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_f \ge 500\Omega$, the output is capable of handling the current requirements ($I_L \le 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

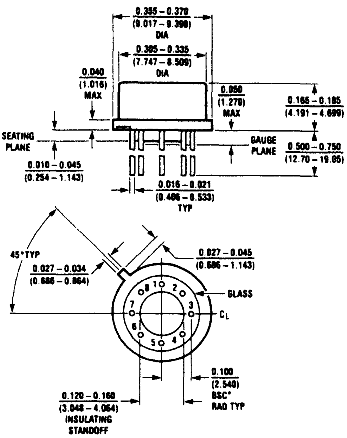
As with all operational amplifiers when $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_f will eliminate this problem.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

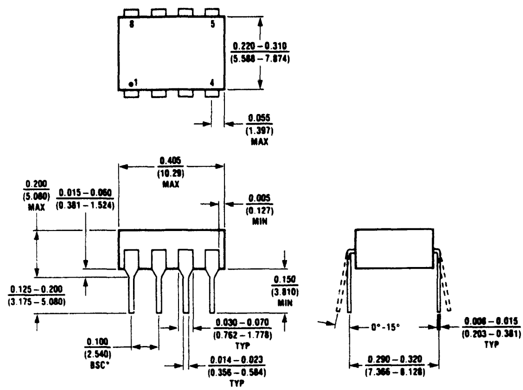
L Package
Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

$T_J$max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

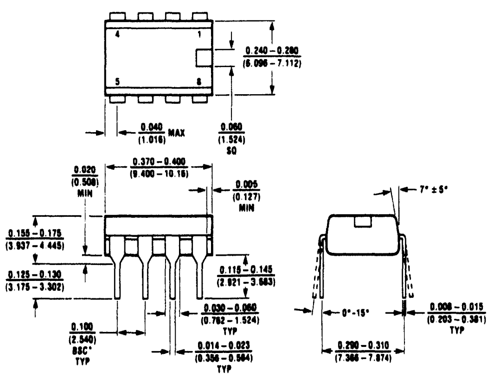
JG Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
°LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_J$max	θ_{ja}
150°C	100°C/W

P Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
°LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

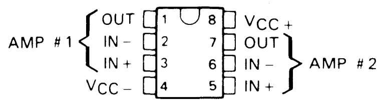
$T_J$max	θ_{ja}
100°C	130°C/W

TYPE RC4559
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

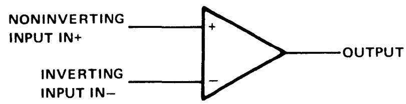
D2785, OCTOBER 1983

- **Matched Gain and Offset Between Amplifiers**
- **Unity-Gain Bandwidth . . . 3 MHz Min**
- **Slew Rate . . . 1.5 V/ns Min**
- **Low Equivalent Input Noise Voltage . . . 2 μV/$\sqrt{\text{Hz}}$ Max (20 Hz to 20 kHz)**
- **No Frequency Compensation Required**
- **No Latch Up**
- **Wide Common-Mode Voltage Range**
- **Low Power Consumption**
- **Designed to be Interchangeable with Raytheon RC4559**

D OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The RC4559 is a dual high-performance operational amplifier. The high common-mode input voltage and the absence of latch-up make this amplifier ideal for low-noise signal applications such as audio preamplifiers and signal conditioners. This amplifier features a guaranteed dynamic performance and output drive capability that far exceeds that of the general-purpose type amplifiers.

The RC4559 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	18 V
Supply voltage V_{CC-} (see Note 1)	−18 V
Differential input voltage (see Note 2)	±30 V
Input voltage (any input, see Notes 1 and 3)	±15 V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)	unlimited
Continuous total dissipation	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ADVANCE INFORMATION

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	25°C		2	6	mV
			0°C to 70°C			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100	nA
			0°C to 70°C			200	
I_{IB}	Input bias current	$V_O = 0$	25°C		40	250	nA
			0°C to 70°C			500	
V_I	Input voltage range		25°C	±12	±13		V
V_{OM}	Maximum peak output voltage swing	$R_L \geq 3$ kΩ	25°C	±12	±13		V
		$R_L = 600$ Ω	25°C	±9.5	±10		
		$R_L \geq 2$ kΩ	0°C to 70°C	±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2$ kΩ	25°C	20	300		V/mV
			0°C to 70°C	15			
B_{OM}	Maximum output-swing bandwidth	$V_{OPP} = 20$ V, $R_L = 2$ kΩ	25°C	24	32		kHz
B_1	Unity-gain bandwidth		25°C	3	4		MHz
r_i	Input resistance		25°C	0.3	1		MΩ
CMRR	Common-mode rejection ratio	$V_O = 0$	25°C	80	100		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_O = 0$	25°C		10	75	μV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 1$ kΩ, f = 20 Hz to 20 kHz	25°C		1.4	2	μV
I_n	Equivalent input noise current	f = 20 Hz to 20 kHz	25°C		25		pA
I_{CC}	Supply current (both amplifiers)	No load, No signal	25°C		3.3	5.6	mA
			0°C		4	6.6	
			70°C		3	5	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $R_S = 1$ kΩ, f = 10 kHz	25°C		90		dB
			25°C		90		

†All characteristics are specified under open-loop operation, unless otherwise noted.

matching characteristics at $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$		±0.2		mV
I_{IO}	Input offset current	$V_O = 0$		±7.5		nA
I_{IB}	Input bias current	$V_O = 0$		±15		nA
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2$ kΩ		±1		dB

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

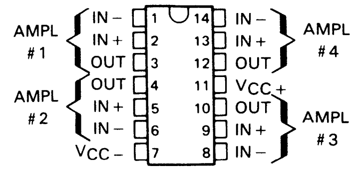
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ,		80		μs
	Overshoot	$C_L = 100$ pF		18%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF	1.5	2		V/μs

TYPES RM4136, RV4136, RC4136
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

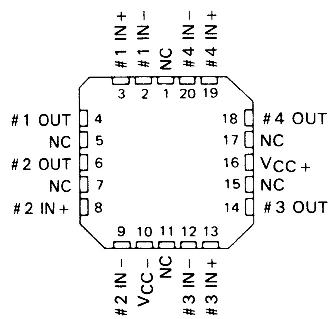
D2142, MARCH 1976—REVISED SEPTEMBER 1983

- Continuous-Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers
- Designed to be Interchangeable with Raytheon RM4136, RV4136, and RC4136
- Low Noise . . . 8 nV/$\sqrt{Hz}$ Typ at 1 kHz

D, J, OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)



RM4136 FK CHIP CARRIER PACKAGE (TOP VIEW)



NC—No internal connection

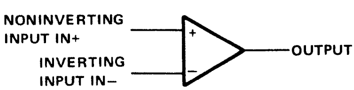
description

The RM4136, RV4136, and RC4136 are quad high-performance operational amplifiers with each amplifier electrically similar to uA741 except that offset null capability is not provided.

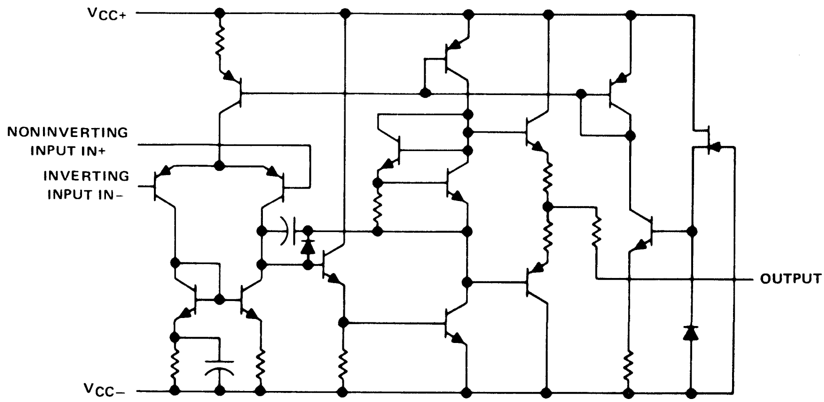
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RM4136 is characterized for operation over the full military temperature range of −55 °C to 125 °C, the RV4136 is characterized for operation from −40 °C to 85 °C, and the RC4136 is characterized for operation from 0 °C to 70 °C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RM4136	RV4136	RC4136	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		800	800	800	mW
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, J, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, RM4136 chips are alloy-mounted; RV4136 and RC4136 chips are glass-mounted.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		RM4136			RV4136			RC4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.5	4		0.5	6		0.5	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	150		5	200		5	200	nA
			Full range			500			500			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		140	400		140	500		140	500	nA
			Full range			1500			1500			800	
V_I	Input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		±12	±14		V
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	50	350		20	300		20	300		V/mV
			Full range	25			15			15			
B_1	Unity-gain bandwidth		25°C		3.5			3			3		MHz
r_i *	Input resistance		25°C	0.3	5		0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50$ Ω	25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		30	150		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, BW = 1 Hz, f = 1 kHz, $R_S = 100$ Ω	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (All four amplifiers)	$V_O = 0$, No load	25°C		5	11.3		5	11.3		5	11.3	mA
			MIN T_A		6	13.3		6	13.7		6	13.7	
			MAX T_A		4.5	10		4.5	10		4.5	10	
P_D	Total power dissipation (All four amplifiers)	$V_O = 0$, No load	25°C		150	340		150	340		150	340	mW
			MIN T_A		180	400		180	400		180	400	
			MAX T_A		135	300		135	300		135	300	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, f = 10 kHz, $R_S = 1$ kΩ	25°C		105			105			105		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for RM4136, −40°C to 85°C for RV4136, and 0°C to 70°C for RC4136.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	RM4136			RV4136, RC4136			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF		0.13			0.13		μs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF		1.7			1.7		V/μs

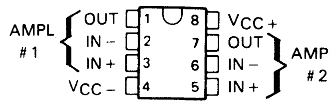
*For RM4136 this parameter is guaranteed but not tested.

TYPES RM4558, RV4558, RC4558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

D2141, MARCH 1976—REVISED FEBRUARY 1984

- Continuous-Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Unity Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers
- Low Noise . . . 8 nV/√Hz Typ at 1 kHz
- Designed to be Interchangeable with Raytheon RM4558, RV4558, and RC4558

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



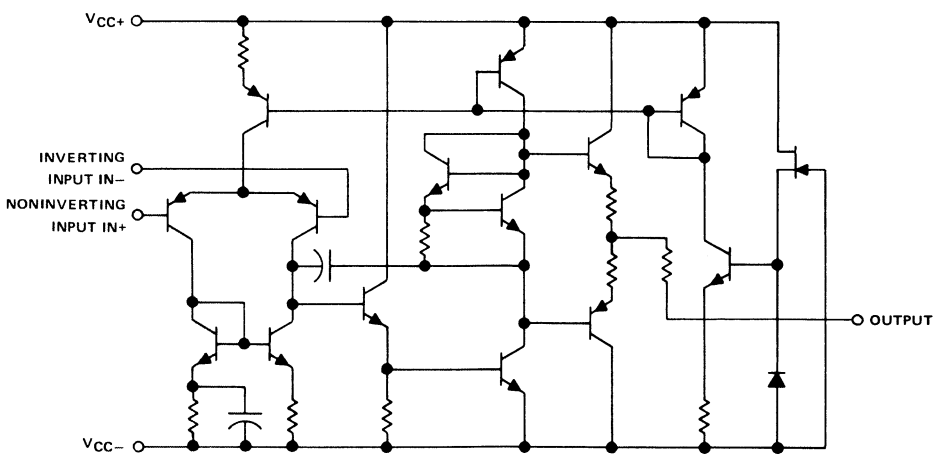
description

The RM4558, RV4558, and RC4558 are dual general-purpose operational amplifiers with each half electrically similar to uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RM4558 is characterized for operation over the full military temperature range of −55 °C to 125 °C; the RV4558 is characterized for operation from −40 °C to 85 °C; and the RC4558 is characterized for operation from 0 °C to 70 °C.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RM4558	RV4558	RC4558	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		680	680	680	mW
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG packages, RM4558 chips are alloy mounted; RV4558 and RC4558 chips are glass mounted.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $C_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		RM4558			RV4558			RC4558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.5	5		0.5	6		0.5	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	200		5	200		5	200	nA
			Full range			500			500			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		140	500		140	500		150	500	nA
			Full range			1500			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		±12	±14		V
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	50	350		20	300		20	300		V/mV
			Full range	25			15			15			
B_1	Unity-gain bandwidth		25°C	2	3.5			3			3		MHz
r_i *	Input resistance		25°C	0.3	5		0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio		25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 15$ V to ±9 V	25°C		30	150		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 100$ Ω, f = 1 kHz, BW = 1 Hz	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (Both amplifiers)	No load, $V_O = 0$	25°C		2.5	5.6		2.5	5.6		2.5	5.6	mA
			MIN T_A		3	6.6		3	6.6		3	6.6	
			MAX T_A		2	5		2.3	5		2.3	5	
P_D	Total power dissipation (Both amplifiers)	No load, $V_O = 0$	25°C		75	170		75	170		75	170	mW
			MIN T_A		90	200		90	200		90	200	
			MAX T_A		60	150		70	150		70	150	
V_{o1}/V_{o2}	Crosstalk attenuation — Open loop	$R_S = 1$ kΩ, f = 10 kHz	25°C		85			85			85		dB
	Crosstalk attenuation — $A_{VD} = 100$		25°C		105			105			105		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is 55°C to 125°C for RM4558, 40°C to 85°C for RV4558, and 0°C to 70°C for RC4558.

*For RM4558 this parameter is guaranteed but not tested.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	RM4558			RV4558			RC4558			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ,		0.13			0.13			0.13		ns
	Overshoot	$C_L = 100$ pF		5%			5%			5%		
SR*	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF	1.1	1.7		1.1	1.7		1.1	1.7		V/µs

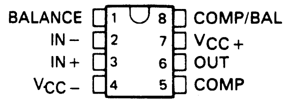
*For RM4558 this parameter is guaranteed but not tested.

TYPES SE5534, SE5534A, NE5534, NE5534A
LOW-NOISE OPERATIONAL AMPLIFIERS

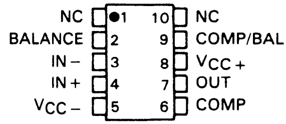
D2532, JULY 1979—REVISED AUGUST 1983

- **Equivalent Input Noise Voltage 3.5 nV/$\sqrt{Hz}$ Typ**
- **Unity-Gain Bandwidth . . . . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio 100 dB Typ**
- **High DC Voltage Gain . . . . 100 V/mV Typ**
- **Peak-to-Peak Output Voltage Swing 32 V Typ with $V_{CC\pm}$ = ±18 V and R_L = 600 Ω**
- **High Slew Rate . . . . 13 V/μs Typ**
- **Wide Supply Voltage Range ±3 V to ±20 V**
- **Low Harmonic Distortion**
- **Designed to be Interchangeable with Signetics SE5534, SE5534A, NE5534, and NE5534A**

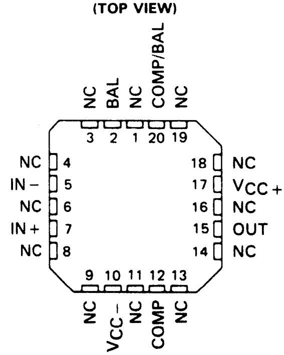
SE5534, SE5534A . . . JG
NE5534, NE5534A . . . JG or P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SE5534, SE5534A
U FLAT PACKAGE
(TOP VIEW)

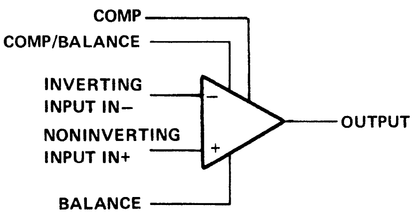


SE5534, SE5534A
FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



description

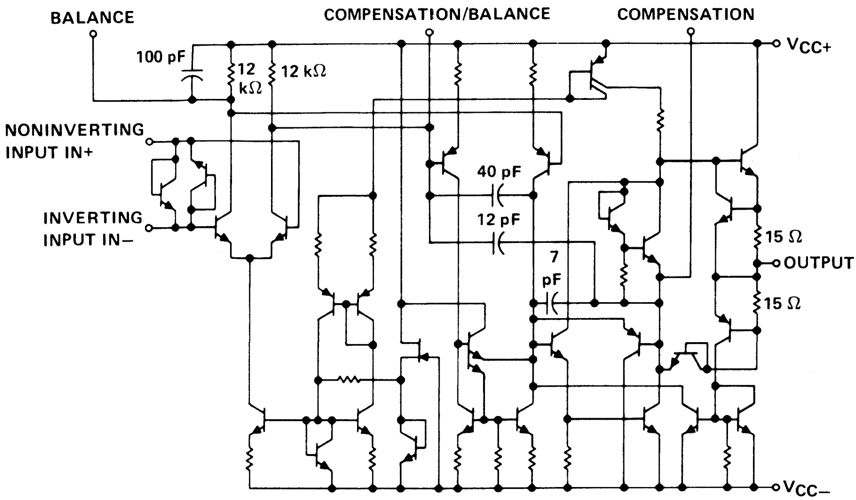
The SE5534, SE5534A, NE5534, and NE5534A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

These operational amplifiers are internally compensated for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between COMP and COMP/BAL. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability.

The SE5534A and NE5534A have guaranteed maximums on equivalent input noise voltage.

The SE5534 and SE5534A are characterized for operation over the full military temperature range of −55°C to 125°C; the NE5534 and NE5534A are characterized for operation from 0°C to 70°C.

schematic



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)		22 V
Supply voltage, V_{CC-} (see Note 1)		−22 V
Input voltage either input (see Notes 1 and 2)		V_{CC+}
Input current (see Note 3)		±10 mA
Duration of output short-circuit (see Note 4)		unlimited
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		
	FK package (see Note 6)	1375 mW
	SE5534, SE5534A in JG package	1050 mW
	NE5534, NE5534A in JG package	825 mW
	P package	725 mW
	U package	675 mW
Operating free-air temperature range:	SE5534, SE5534A	−55°C to 125°C
	NE5534, NE5534A	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK, JG, or U package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves, Section 2. In the JG package, SE5534 and SE5534A chips are alloy-mounted; NE5534 and NE5534A chips are glass-mounted.
6. For FK package, power rating and derating factor will vary with actual mounting technique used. The value stated here is believed to be conservative.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SE5534, SE5534A			NE5534, NE5534A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		0.5	2		0.5	4	mV
			T_A = full range			3			5	
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		10	200		20	300	nA
			T_A = full range			500			400	
I_{IB}	Input bias current	$V_O = 0$	$T_A = 25°C$		400	800		500	1500	nA
			T_A = full range			1500			2000	
V_{ICR}	Common-mode input voltage range			±12	±13		±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 600\ \Omega$	$V_{CC\pm} = \pm 15$ V	24	26		24	26		V
			$V_{CC\pm} = \pm 18$ V	30	32		30	32		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 600\ \Omega$	$T_A = 25°C$	50	100		25	100		V/mV
			T_A = full range	25			15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz	$C_C = 0$		6			6		V/mV
			$C_C = 22$ pF		2.2			2.2		
B_{OM}	Maximum-output-swing bandwidth	$V_O = \pm 10$ V,	$C_C = 0$		200			200		kHz
		$V_O = \pm 10$ V,	$C_C = 22$ pF		95			95		
		$V_{CC\pm} = \pm 18$ V, $R_L = 600\ \Omega$,	$V_O = \pm 14$ V, $C_C = 22$ pF		70			70		
B_1	Unity-gain bandwidth	$C_C = 22$ pF,	$C_L = 100$ pF		10			10		MHz
r_i *	Input resistance			50	100		30	100		kΩ
z_o	Output impedance	$A_{VD} = 30$ dB, $C_C = 22$ pF,	$R_L = 600\ \Omega$, f = 10 kHz		0.3			0.3		Ω
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = V_{ICR}$ min,	80	100		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 9$ V to ±15 V, $V_O = 0$,	$R_S = 50\ \Omega$	86	100		80	100		dB
I_{OS}	Output short-circuit current				38			38		mA
I_{CC}	Supply current	No load, $V_O = 0$	$T_A = 25°C$		4	6.5		4	8	mA
			T_A = full range			9				

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for $T_A = -55°C$ to 125°C for SE5534 and SE5534A and 0°C to 70°C for NE5534 and NE5534A.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	SE5534, NE5534			SE5534A, NE5534A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$C_C = 0$		13			13		V/μs
		$C_C = 22$ pF		6			6		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 22$ pF, $C_L = 100$ pF		20			20		ns
	Overshoot factor			20%			20%		
t_r	Rise time	$V_I = 50$ mV, $A_{VD} = 1$, $R_L = 600\ \Omega$, $C_C = 47$ pF, $C_L = 500$ pF		50			50		ns
	overshoot factor			35%			35%		
V_n	Equivalent input * noise voltage	f = 30 Hz		7			5.5	7	$nV/\sqrt{Hz}$
		f = 1 kHz		4			3.5	4.5	
I_n	Equivalent input noise current	f = 30 Hz		2.5			1.5		$pA/\sqrt{Hz}$
		f = 1 kHz		0.6			0.4		
F	Average noise figure	$R_S = 5$ kΩ, f = 10 Hz to 20 kHz					0.9		dB

*For SE5534 and SE5534A these parameters guaranteed but not tested.

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT BIAS CURRENT and INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

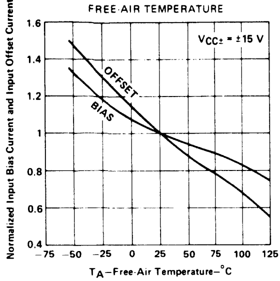


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

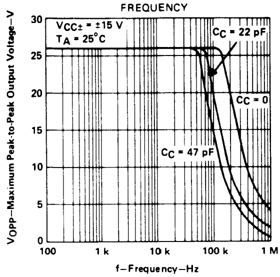


FIGURE 2

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

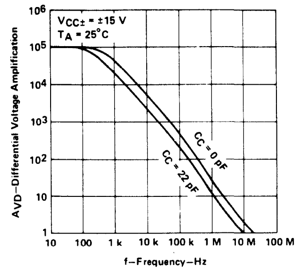


FIGURE 3

NORMALIZED SLEW RATE and UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

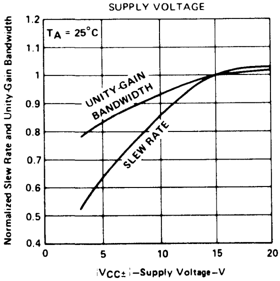


FIGURE 4

NORMALIZED SLEW RATE and UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

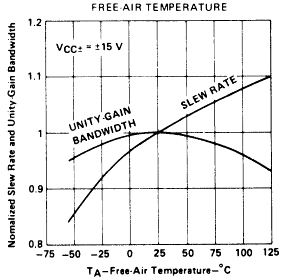


FIGURE 5

TOTAL HARMONIC DISTORTION vs FREQUENCY

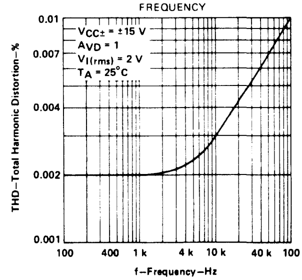


FIGURE 6

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

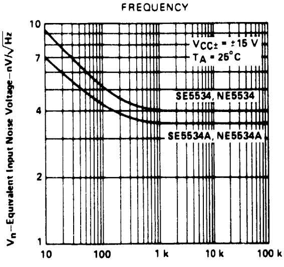


FIGURE 7

EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

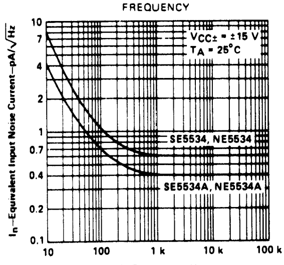


FIGURE 8

TOTAL EQUIVALENT INPUT NOISE VOLTAGE vs SOURCE RESISTANCE

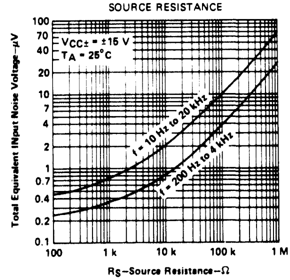


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

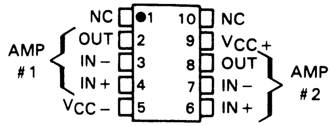
3 Operational Amplifiers

TYPES TL022M, TL022C
DUAL LOW-POWER OPERATIONAL AMPLIFIERS

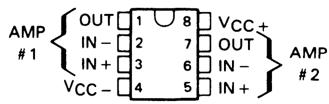
D1661, SEPTEMBER 1973—REVISED AUGUST 1983

- **Very Low Power Consumption**
- **Power Dissipation with ±2-V Supplies . . . 170 μW Typ**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Input Offset Voltage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Popular Dual Op-Amp Pin-Out**

TL022M . . . U FLAT PACKAGE
(TOP VIEW)



TL022C . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



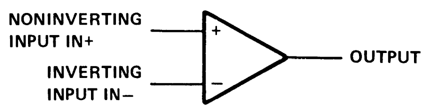
NC—No internal connection

description

The TL022 is a dual low-power operational amplifier designed to replace higher power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use.

The TL022M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL022C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			TL022M	TL022C	UNIT
Supply voltage V_{CC+} (see Note 1)			22	18	V
Supply voltage V_{CC-} (see Note 1)			−22	−18	V
Differential input voltage (see Note 2)			±30	±30	V
Input voltage (any input, see Notes 1 and 3)			±15	±15	V
Duration of output short-circuit (see Note 4)			unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature range (see Note 5)	Each amplifier		500	500	mW
	Total package	JG or P package	680	680	mW
		U package	675	675	mW
Operating free-air temperature range			−55 to 125	0 to 70	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		JG or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL022M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the JG package, TL022M chips are alloy-mounted; TI022C chips are glass-mounted.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current	$V_O = 0$	25°C		50	100		100	250	nA
			Full range			250			400	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10$ kΩ	25°C	20	26		20	26		V
		$R_L \geq 10$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplication	$R_L \geq 10$ kΩ, $V_O = \pm 10$ V	25°C	72	86		60	80		dB
			Full range	72			60			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V, $R_S = 50\ \Omega$	25°C		30	150		30	200	μV/V
			Full range			150			200	
V_n	Equivalent input noise voltage	$A_{VD} = 20$ dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (both amplifiers)	No load, $V_O = 0$	25°C		130	200		130	250	μA
			Full range			200			250	
P_D	Total dissipation (both amplifiers)	No load, $V_O = 0$	25°C		3.9	6		3.9	7.5	mW
			Full range			6			7.5	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for TL022M is −55°C to 125°C and for TL022C is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10$ kΩ,		0.3			0.3		μs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10$ kΩ, See Figure 1		0.5			0.5		V/μs

3 Operational Amplifiers

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TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

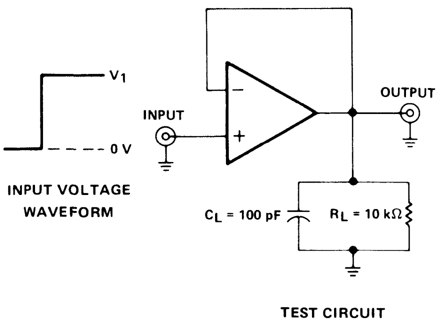


FIGURE 1–RISE TIME, OVERSHOOT FACTOR, AND SLEW RATE

TYPICAL CHARACTERISTICS

TOTAL POWER DISSIPATED
vs
SUPPLY VOLTAGE

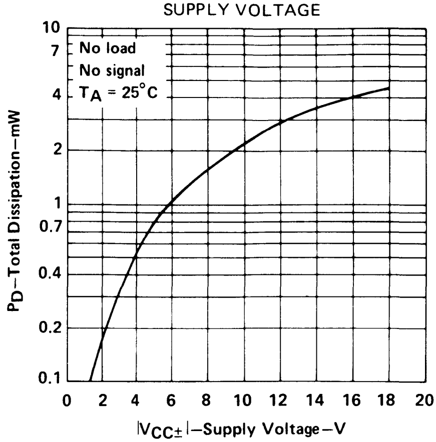
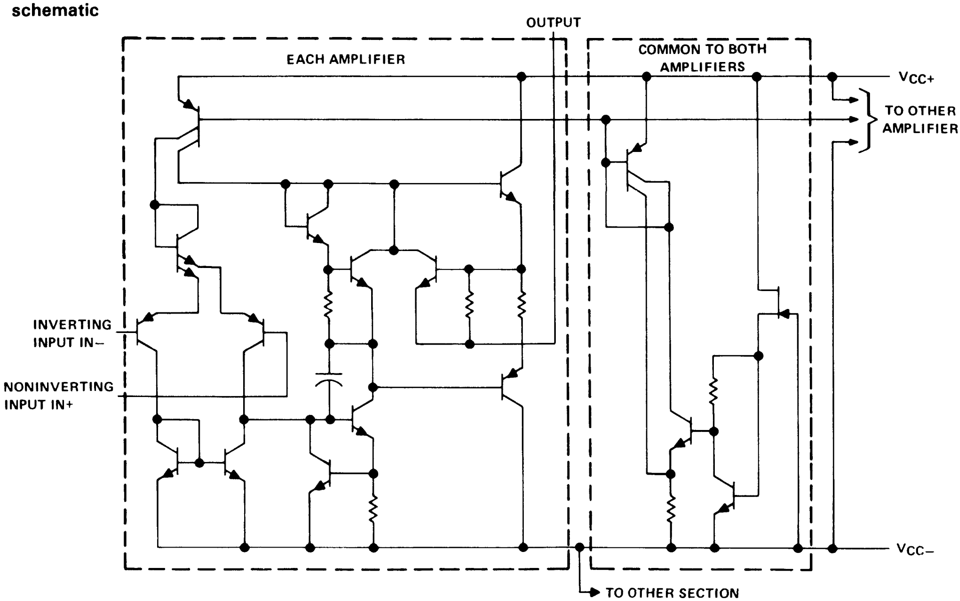


FIGURE 2

schematic



JULY 1988

- **Maximum Offset Voltage . . . 800 µV**
- **High Slew Rate . . . 2.9 V/µs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 6.5 mW Typ**
- **Output Short-Circuit Protection**

description

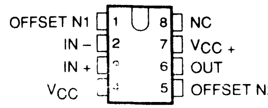
The TL031 and TL031A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low power consumption make the TL031 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL031 has been designed to be functionally compatible and pin compatible with the TL061.

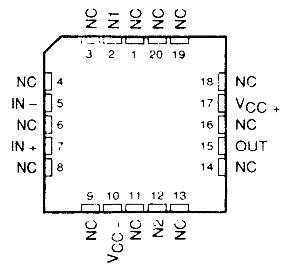
Two offset voltage grades are available:
TL031 (1.5 mV max) and TL031A (800 µV max).

A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

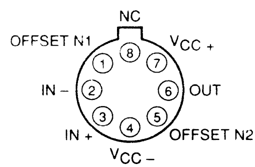
D, JG, or P PACKAGE (TOP VIEW)



FK PACKAGE (TOP VIEW)

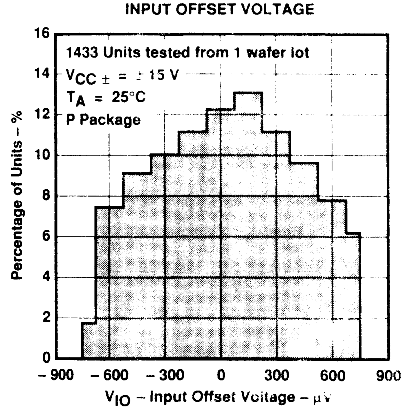


L PACKAGE (TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case
NC – No internal connection

DISTRIBUTION OF TL031A INPUT OFFSET VOLTAGE



AVAILABLE OPTIONS

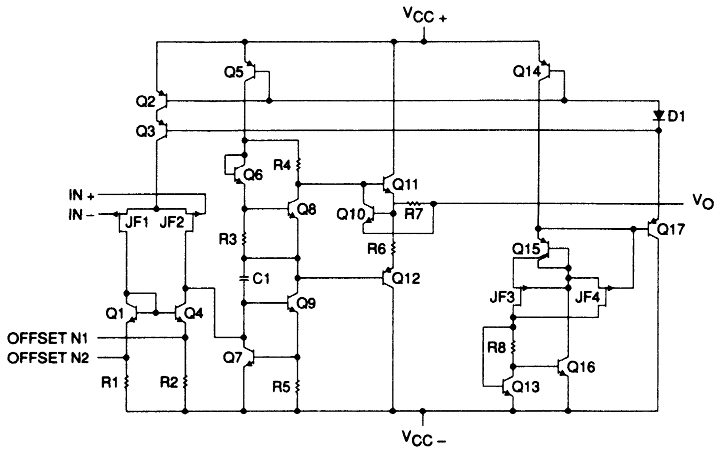
T_A	V_{IO}max at 25°C	PACKAGE: Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)	Metal Can (L)
0°C to 70°C	0.8 mV	TL031ACD	TL031ACP	TL031ACJG	——	TL031ACL
	1.5 mV	TL031CD	TL031CP	TL031CJG	——	TL031CL
− 40°C to 85°C	0.8 mV	TL031AID	TL031AIP	TL031AIJG	——	TL031AIL
	1.5 mV	TL031ID	TL031IP	TL031IJG	——	TL031IL
− 55°C to 125°C	0.8 mV	——	——	TL031AMJG	TL031AMFK	TL031AML
	1.5 mV	——	——	TL031MJG	TL031MFK	TL031ML

NOTE 1: D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TL031CDR).

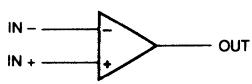
description (continued)

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic



symbol



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 2) .... 18 V
Supply voltage, V_{CC-} (see Note 2) .... – 18 V
Differential input voltage (see Note 3) .... ± 30 V
Input voltage range, V_I (any input, see Notes 2 and 4) .... ± 15 V
Input current, I_I (each input) .... ± 1 mA
Output current, I_O .... ± 80 mA
Total current into V_{CC+} terminal .... 160 mA
Total current out of V_{CC-} terminal .... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 5) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M- suffix .... – 55°C to 125°C
I- suffix .... – 40°C to 85°C
C- suffix .... 0°C to 70°C
Storage temperature range .... – 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package .... 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
5. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.1 mW/°C	421 mW	344 mW	140 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX			I- SUFFIX			C- SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	V
Input voltage, V_I	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS			$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
				T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031C	25°C		0.54	3.5		0.5	1.5	mV
				Full range			4.5			2.5	
			TL031AC	25°C		0.41	2.8		0.34	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL031C	25°C to 70°C		7.1			5.9		µV/°C
			TL031AC	25°C to 70°C		7.1			5.9	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_l = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 7		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation	No load, $V_O = 0$		25°C		1.9	2.5		6.5	8.4	mW
				0°C		1.8	2.5		6.3	8.4	
				70°C		1.9	2.5		6.3	8.4	
I_{CC}	Supply current	No load, $V_O = 0$		25°C		192	250		217	280	µA
				0°C		184	250		211	280	
				70°C		189	250		210	280	

NOTES: 6. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	TYP	MAX	$V_{CC\pm} = \pm15$ V MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/µs
				0°C		1.8		1.5	2.6		
				70°C		2.2		2	3.2		
SR−	Negative slew rate at unity gain			25°C		3.9		3.5	5.1		V/µs
				0°C		3.7		3.2	4.9		
				70°C		4		3.2	5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
				0°C		134			127		
				70°C		150			142		
t_f	Fall time			25°C		138			132		ns
				0°C		134			127		
				70°C		150			142		
	Overshoot factor			25°C		11%			5%		
				0°C		10%			4%		
				70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9) — TL031C	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
			f = 1 kHz			41			41		
	TL031AC		f = 10 Hz	25°C		61			61		
			f = 1 kHz			41			41	60	
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
				0°C		1			1.1		
				70°C		1			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
				0°C		61°			65°		
				70°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031I	25°C		0.54	3.5		0.5	1.5	mV
				Full range			5.3			3.3	
			TL031AI	25°C		0.41	2.8		0.34	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL031I	25°C to 85°C		6.5			6.2		µV/°C
			TL031AI	25°C to 85°C		6.5			6.2	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.2	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10$ kΩ, See Note 7		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation	No load, $V_O = 0$		25°C		1.9	2.5		6.5	8.4	mW
				−40°C		1.4	2.5		5.4	8.4	
				85°C		1.9	2.5		6.2	8.4	
I_{CC}	Supply current	No load, $V_O = 0$		25°C		192	250		217	280	µA
				−40°C		144	250		181	280	
				85°C		189	250		207	280	

NOTES: 6. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/μs
					− 40°C		1.5		1.5	2.1		
					85°C		2.3		2	3.3		
SR −	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					− 40°C		3.4		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					− 40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					− 40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					− 40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL031I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AI		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					− 40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					− 40°C		60°			65°		
					85°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL031M	25°C		0.54	3.5		0.5	1.5	mV
				Full range			6.5			4.5	
			TL031AM	25°C		0.41	2.8		0.34	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL031M	25°C to 125°C		5.1			4.3		µV/°C
			TL031AM	25°C to 125°C		5.1			4.3		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 7		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	4	12.9		5	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		75	94		
				125°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation	No load, $V_O = 0$		25°C		1.9	2.5		6.5	8.4	mW
				−55°C		1.1	2.5		4.7	8.4	
				125°C		1.8	2.5		5.8	8.4	
I_{CC}	Supply current	No load, $V_O = 0$		25°C		192	250		217	280	µA
				−55°C		114	250		156	280	
				125°C		178	250		197	280	

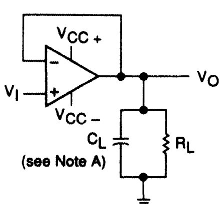
NOTE 7. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8	25°C		2		2	2.9		V/μs
			– 55°C		1.4		1.2	1.9		
			125°C		2.4		2	3.5		
SR –	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/μs
			– 55°C		3.2		3.2	4.6		
			125°C		4.1		3.2	4.7		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			– 55°C		142			123		
			125°C		166			158		
t_f	Fall time		25°C		138			132		ns
			– 55°C		142			123		
			125°C		166			158		
	Overshoot factor		25°C		11%			5%		
			– 55°C		16%			6%		
			125°C		14%			8%		
V_n	Equivalent input noise voltage, TL031M	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		61			61		nV/√Hz
		f = 1 kHz			41			41		
	TL031AM	f = 10 Hz	25°C		61			61		
		f = 1 kHz			41			41		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			– 55°C		1			1.1		
			125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			– 55°C		57°			64°		
			125°C		59°			62°		

NOTE 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

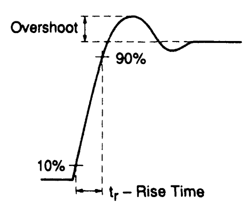


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

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PARAMETER MEASUREMENT INFORMATION

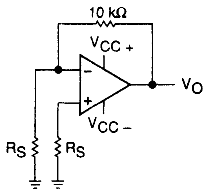
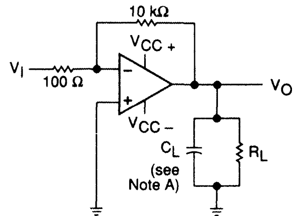


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

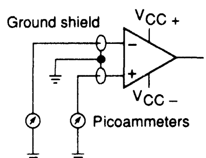


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL031 and TL031A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test is performed which measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet your application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE

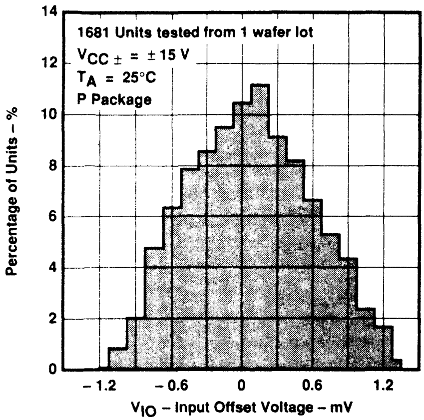

FIGURE 6

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

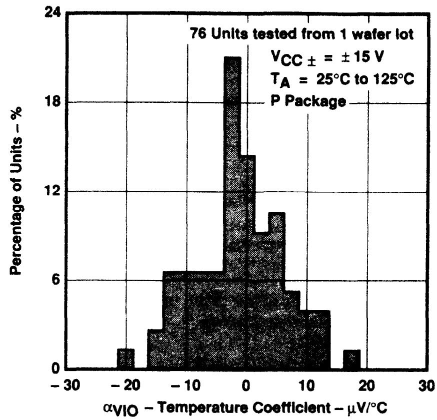

FIGURE 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

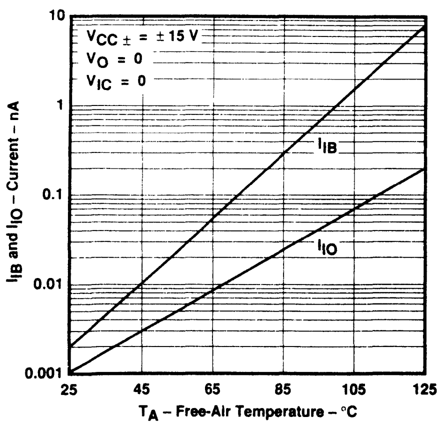

FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

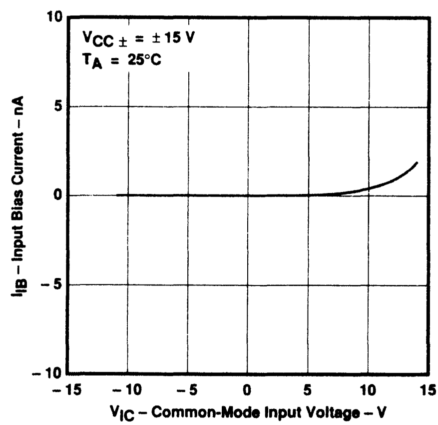

FIGURE 9

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TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

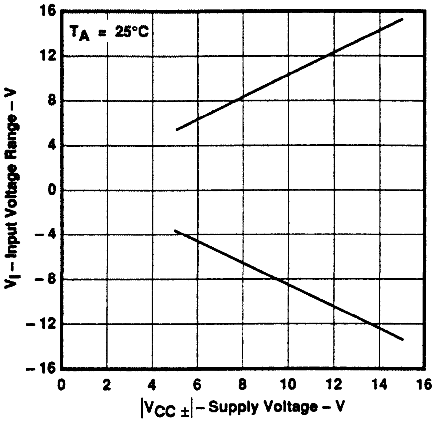

FIGURE 10

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

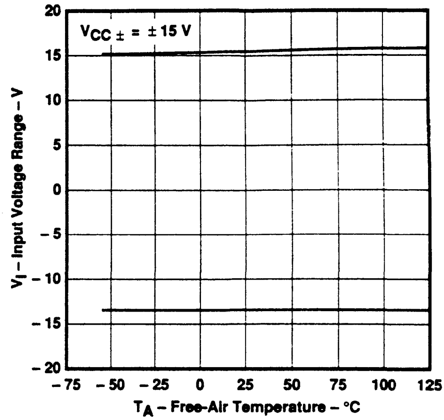

FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

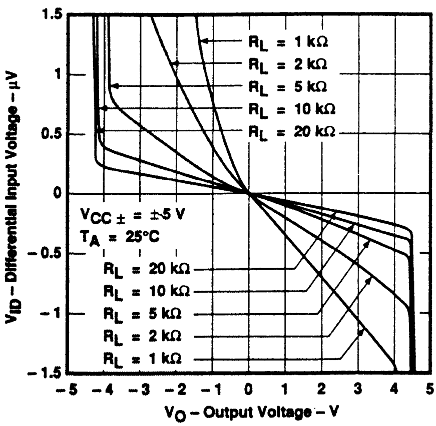

FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

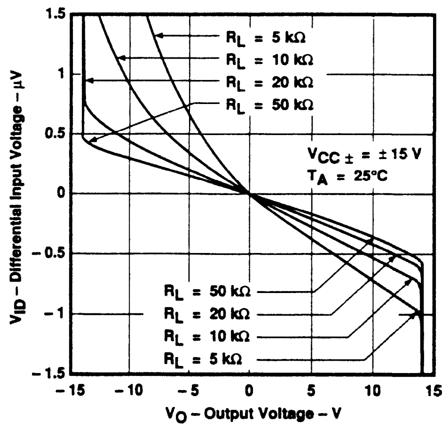

FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

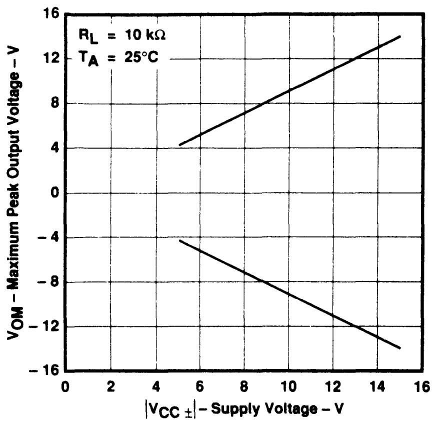

FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

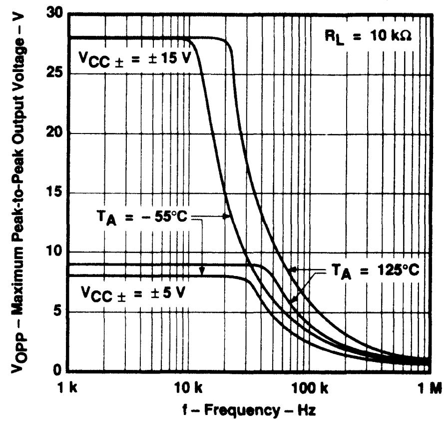

FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

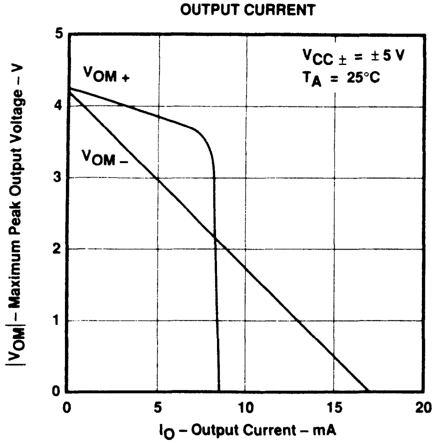

FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

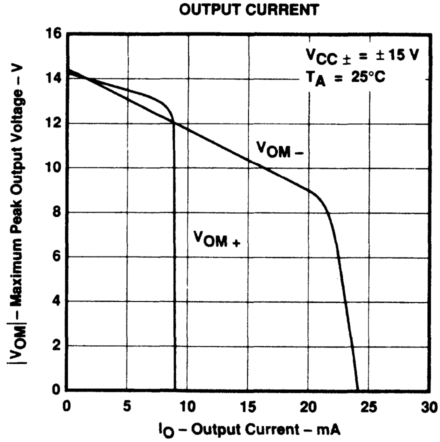

FIGURE 17

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Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

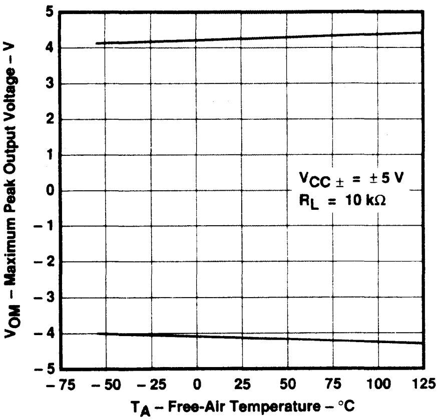

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

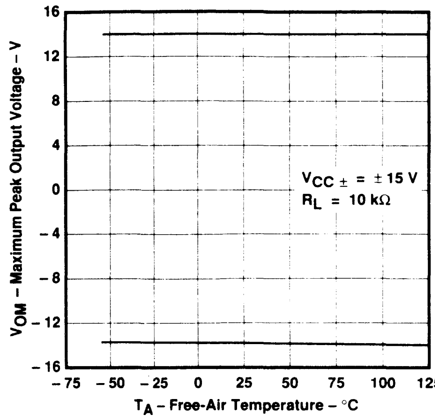

FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

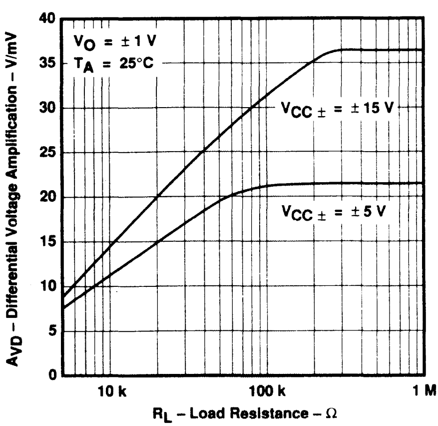

FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

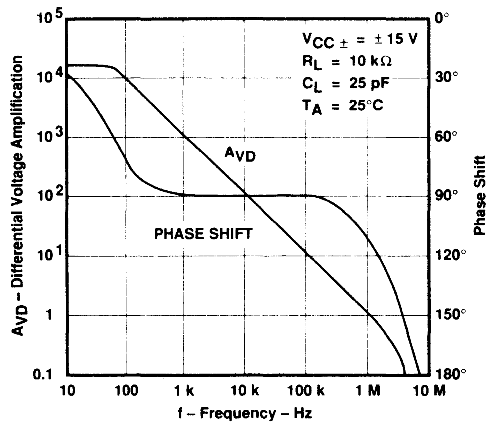

FIGURE 21

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Operational Amplifiers

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

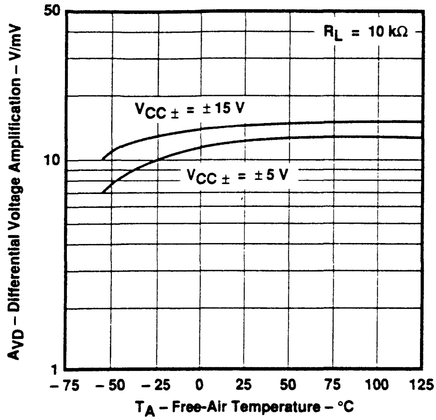


FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

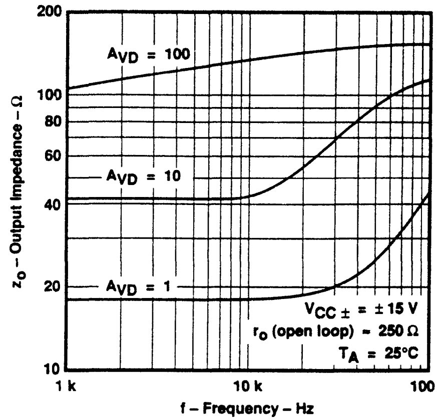


FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

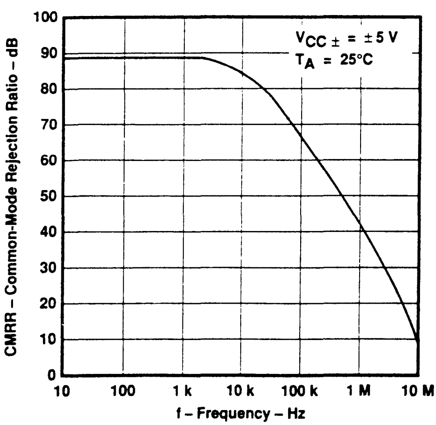


FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

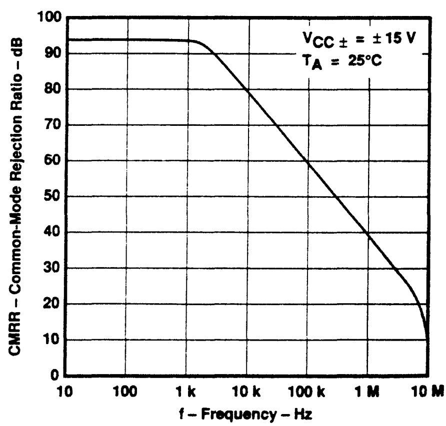


FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

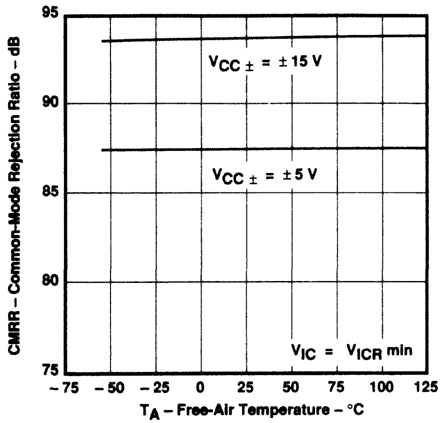


FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

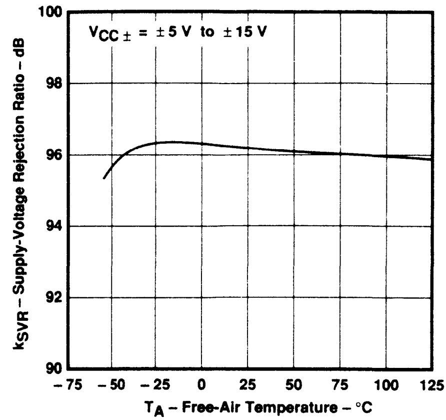


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

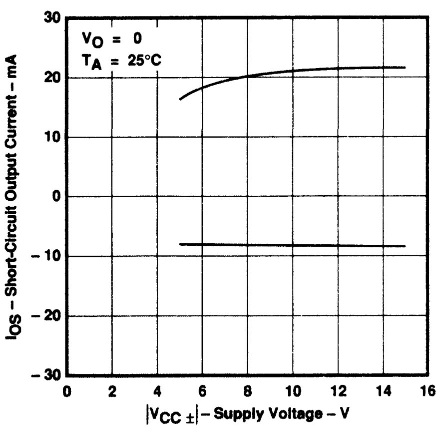


FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

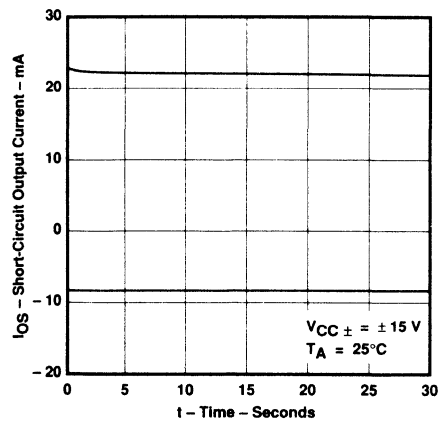


FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

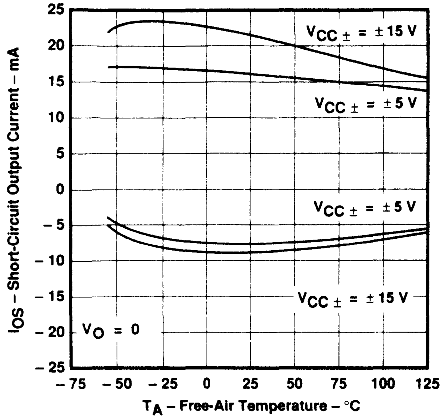


FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

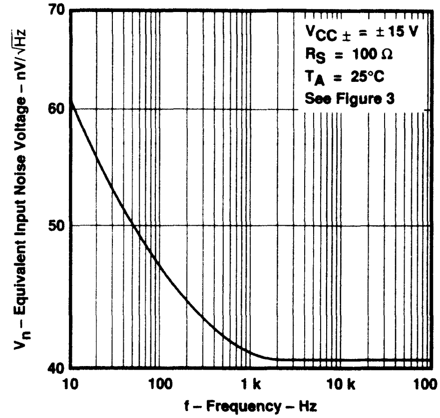


FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

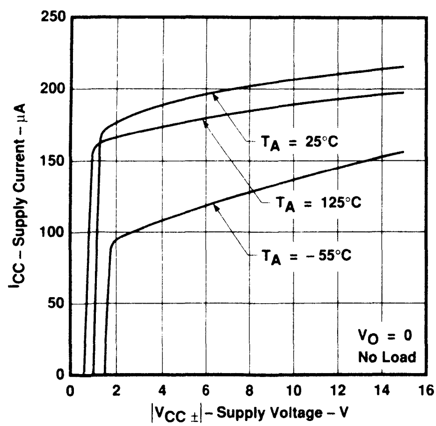


FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

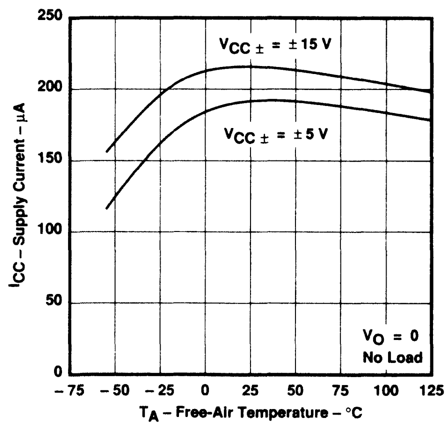


FIGURE 33

TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

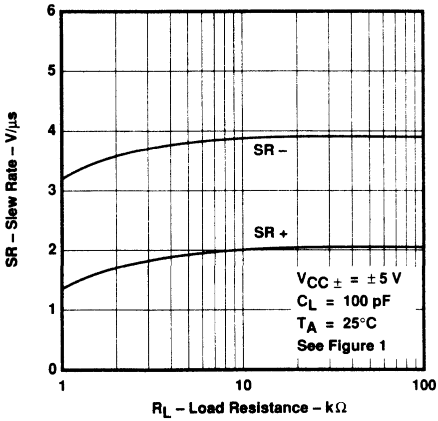


FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

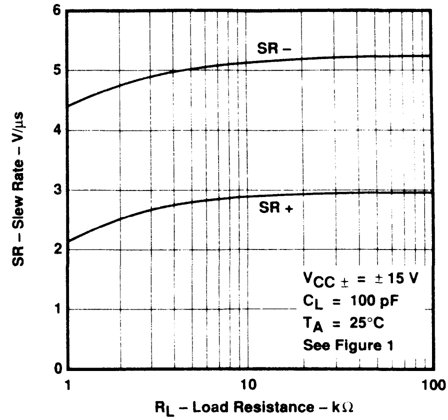


FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

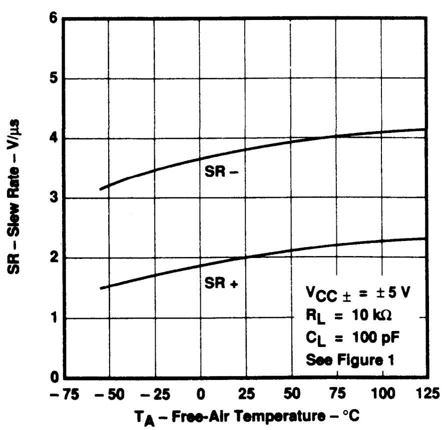


FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

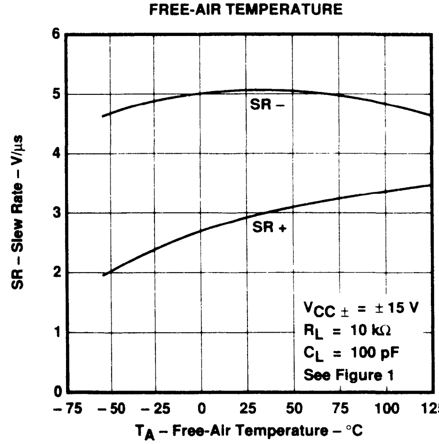


FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

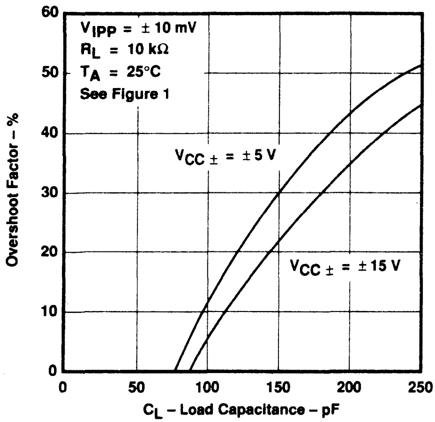


FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

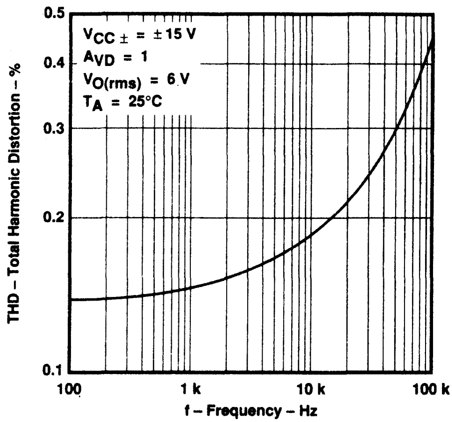


FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

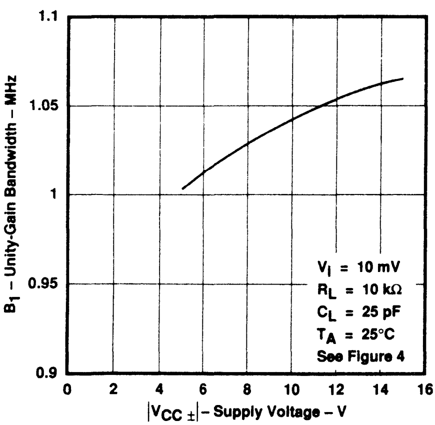


FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

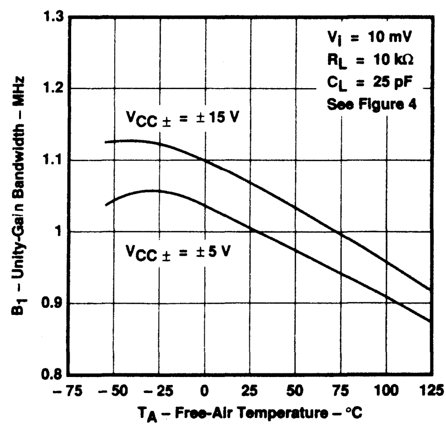


FIGURE 41

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

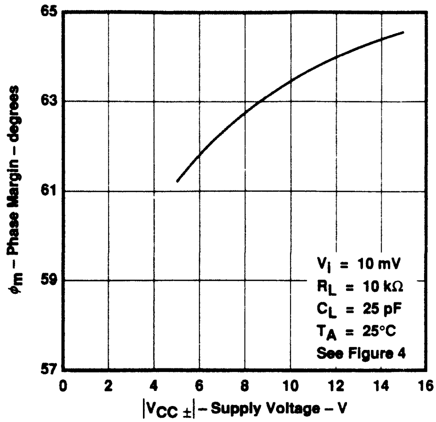


FIGURE 42

PHASE MARGIN vs LOAD CAPACITANCE

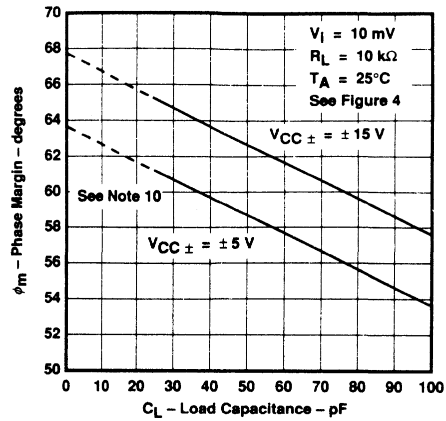


FIGURE 43

PHASE MARGIN vs FREE-AIR TEMPERATURE

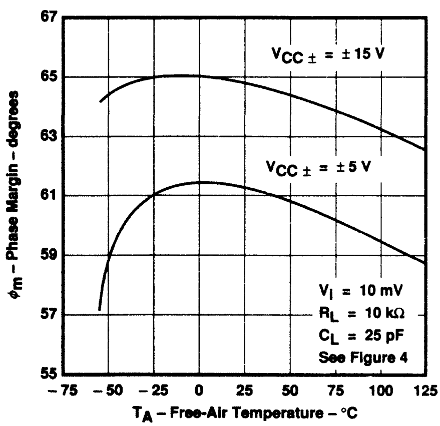


FIGURE 44

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

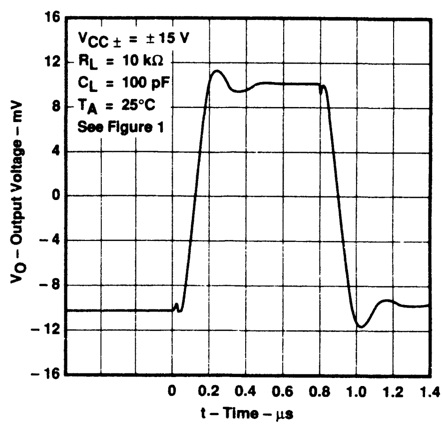


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

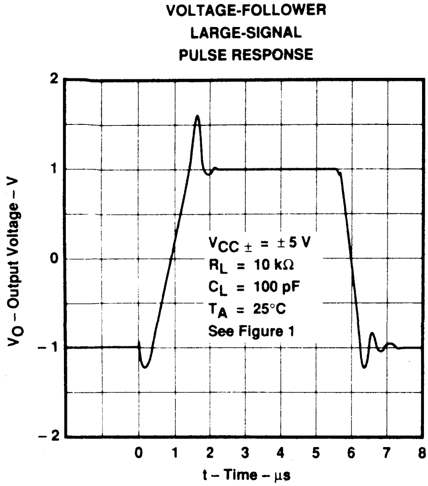


FIGURE 46

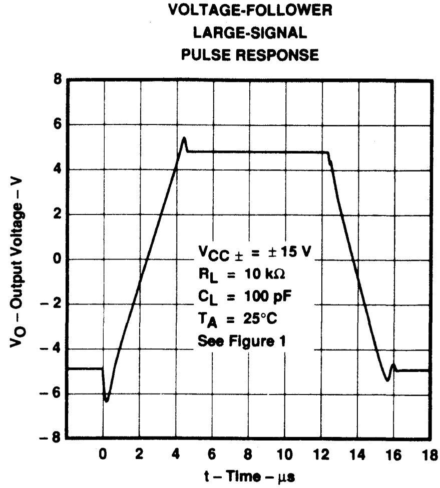


FIGURE 47

TYPICAL APPLICATION DATA

input characteristics

The TL031 and TL031A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL031 and TL031A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

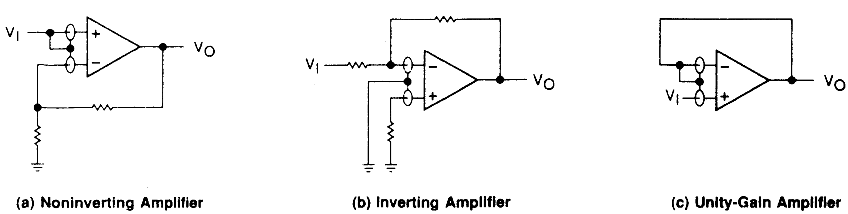
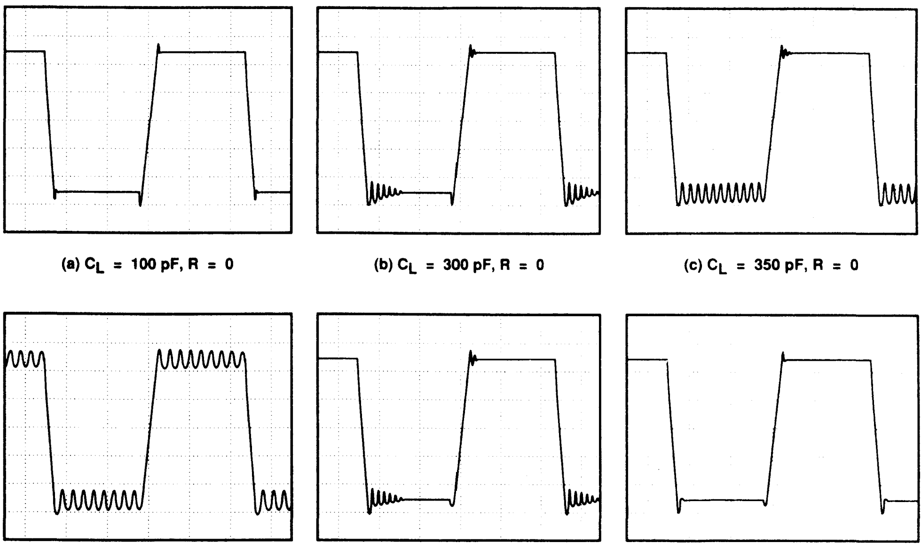


FIGURE 48. USE OF GUARD RINGS

TYPICAL APPLICATION DATA

output characteristics

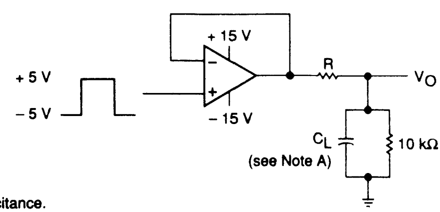
All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL031 and TL031A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

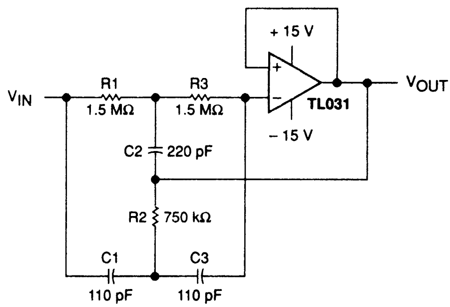
TYPICAL APPLICATION DATA

high-Q notch filter

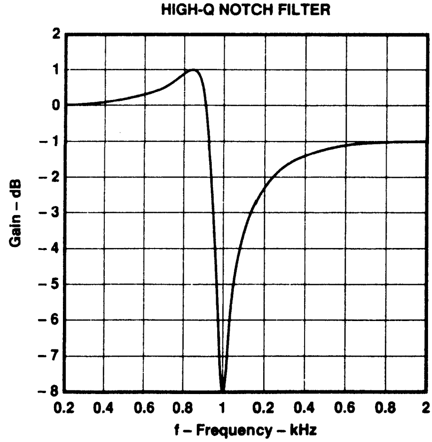
In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. This circuit provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown below, the center frequency is 1 kHz. Note that C1 = C3 = C2 ÷ 2 and also that R1 = R3 = 2 × R2. The center frequency can be modified by varying these values. When adjusting the center frequency, be sure that the operational amplifier still has sufficient gain at the frequency of interest.



HIGH-Q NOTCH FILTER



TYPICAL APPLICATION DATA

transimpedance amplifier

The low power precision TL031 allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL031A greatly simplify the design of a transimpedance amplifier. At room temperature this design achieves ten bit accuracy with an error of less than ½ LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F\left(\frac{R1 + R2}{R2}\right)$$

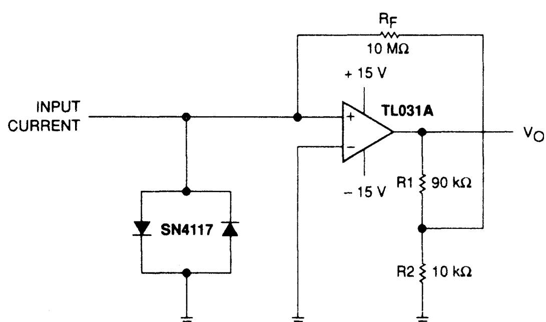
Using the resistor values shown in the schematic, for a ± 1-nA input current, the output voltage equals − 0.1 V. If the V_O limit for the TL031A is measured to be 12 V, the maximum input current for these resistor values is 120 nA. Similarly, one LSB on a ten bit scale corresponds to 12 mV of output voltage or 120 pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = \left[V_{IO} - R_F(I_{IN} + I_{IB})\right]\left(\frac{R1 + R2}{R2}\right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard NPN diodes. Instead, use low-leakage SN4117 JFETs connected as diodes across the TL031A inputs.

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using nigh quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.



TYPICAL APPLICATION DATA

4- to 20-mA current loops

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The first circuit requires three wires from the transmitting to receiving circuitry while the second variation requires only two wires but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL031A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL031A is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA}$$

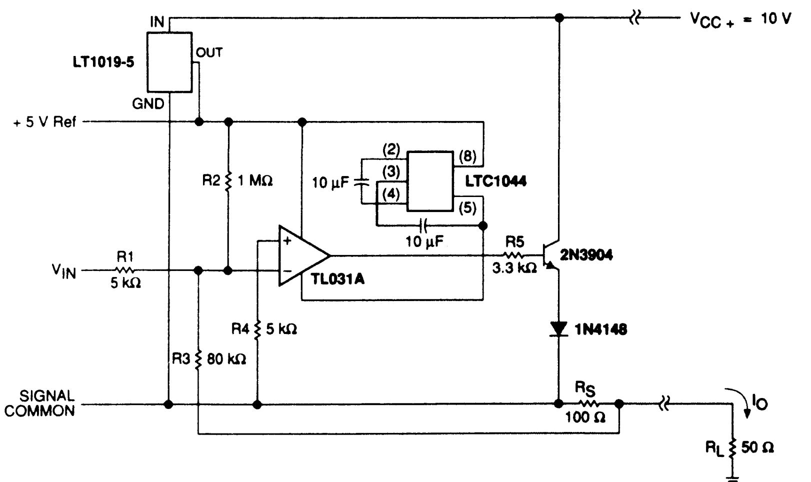
The circuits presently provide 4 to 20 mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3 the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL031A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA} - 0.17 \times V_{IO}$$

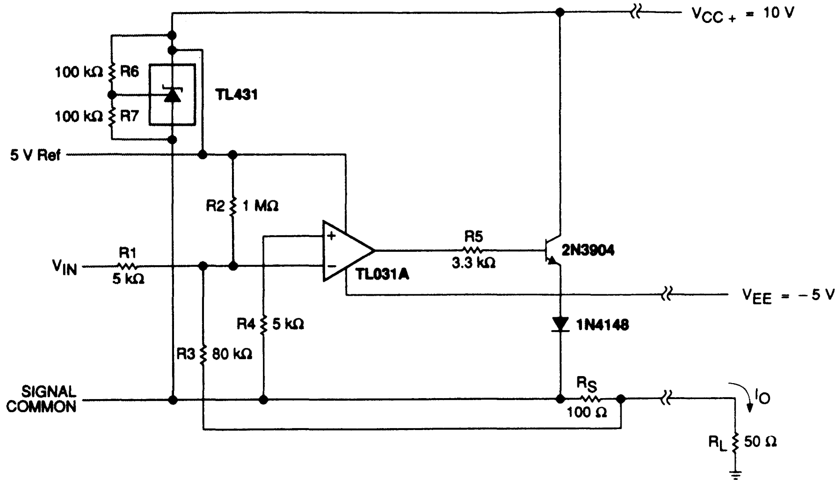
For example, an offset voltage of 1mV will decrease the output current by 0.17 mA..

Thanks to the low power consumption of the TL031A, both circuits have at least 2 mA available to drive the actual sensor from the 5-V reference node.



2 WIRE 4- TO 20-mA CURRENT LOOP

TYPICAL APPLICATION DATA



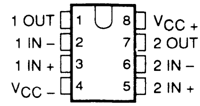
3 WIRE 4- TO 20-mA CURRENT LOOP

ENHANCED JFET LOW-POWER LOW-OFFSET DUAL OPERATIONAL AMPLIFIERS

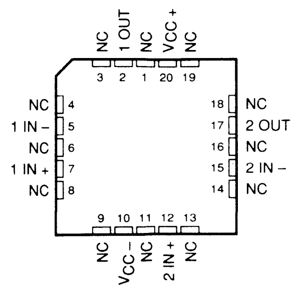
JULY 1988

- **Maximum Offset Voltage . . . 800 μV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 13 mW Typ**
- **Output Short-Circuit Protection**

D, JG, or P PACKAGE (TOP VIEW)

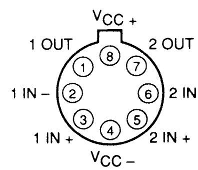


FK PACKAGE (TOP VIEW)



NC – No internal connection

L PACKAGE (TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case

description

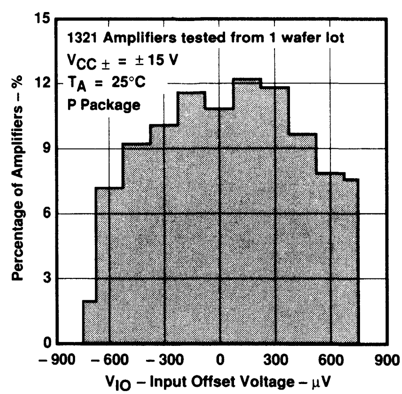
The TL032 and TL032A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low power consumption make the TL032 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL032 has been designed to be functionally compatible and pin compatible with the TL062.

Two offset voltage grades are available: TL032 (1.5 mV max) and TL032A (800 μV max).

A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

DISTRIBUTION OF TL032A INPUT OFFSET VOLTAGE



AVAILABLE OPTIONS

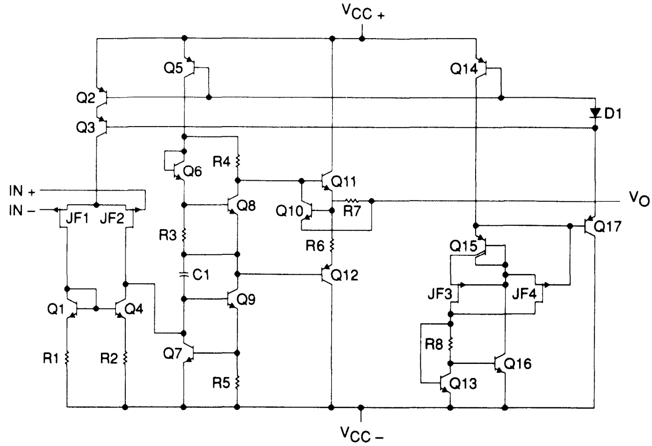
T_A	V_{IO}max at 25°C	PACKAGE: Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)	Metal Can (L)
0°C to 70°C	0.8 mV	TL032ACD	TL032ACP	TL032ACJG	——	TL032ACL
	1.5 mV	TL032CD	TL032CP	TL032CJG	——	TL032CL
− 40°C to 85°C	0.8 mV	TL032AID	TL032AIP	TL032AIJG	——	TL032AIL
	1.5 mV	TL032ID	TL032IP	TL032IJG	——	TL032IL
− 55°C to 125°C	0.8 mV	——	——	TL032AMJG	TL032AMFK	TL032AML
	1.5 mV	——	——	TL032MJG	TL032MFK	TL032ML

NOTE 1: D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TL032CDR).

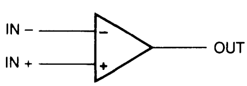
description (continued)

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 2) . . . . . . 18 V
Supply voltage, V_{CC-} (see Note 2) . . . . . . – 18 V
Differential input voltage (see Note 3) . . . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 2 and 4) . . . . . . ± 15 V
Input current, I_I (each input) . . . . . . ± 1 mA
Output current, I_O (each output) . . . . . . ± 80 mA
Total current into V_{CC+} terminal . . . . . . 160 mA
Total current out of V_{CC-} terminal . . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 5) . . . . . . Unlimited
Continuous total dissipation . . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M- suffix . . . . . . – 55°C to 125°C
I- suffix . . . . . . – 40°C to 85°C
C- suffix . . . . . . 0°C to 70°C
Storage temperature range . . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . . 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
5. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.1 mW/°C	421 mW	344 mW	140 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX			I- SUFFIX			C- SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	V
Input voltage, V_I	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032C	25°C		0.69	3.5		0.57	1.5	mV
				Full range			4.5			2.5	
			TL032AC	25°C		0.53	2.8		0.39	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL032C	25°C to 70°C		11.5			10.8		µV/°C
			TL032AC	25°C to 70°C		11.5			10.8	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 7		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				0°C		3.7	5		12.7	17	
				70°C		3.8	5		12.6	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434	560	µA
				0°C		368	500		422	560	
				70°C		378	500		420	560	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTES: 6. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8	25°C		2		2	2.9		V/μs
			0°C		1.8		1.5	2.6		
			70°C		2.2		2	3.2		
SR −	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/μs
			0°C		3.7		3.2	4.9		
			70°C		4		3.2	5		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			0°C		134			127		
			70°C		150			142		
t_f	Fall time		25°C		138			132		ns
			0°C		134			127		
			70°C		150			142		
	Overshoot factor		25°C		11%			5%		
			0°C		10%			4%		
			70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9), TL032C	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		49			49		nV/√Hz
		f = 1 kHz			41			41		
	TL032AC	f = 10 Hz	25°C		49			49		
		f = 1 kHz			41			41	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			0°C		1			1.1		
			70°C		1			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			0°C		61°			65°		
			70°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS			$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
				T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032I	25°C		0.69	3.5		0.57	1.5	mV
				Full range			5.3			3.3	
			TL032AI	25°C		0.53	2.8		0.39	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL032I	25°C to 85°C		11.4			10.8		μV/°C
			TL032AI	25°C to 85°C		11.4			10.8	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 7		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				−40°C		2.9	5		10.9	17	
				85°C		3.7	5		12.4	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434	560	μA
				−40°C		288	500		362	560	
				85°C		372	500		414	560	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTES: 6. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.
7. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR +	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/μs
					−40°C		1.5		1.5	2.1		
					85°C		2.3		2	3.3		
SR −	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					−40°C		3.4		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL032I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AI		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−40°C		60°			65°		
					85°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL032M	25°C		0.69	3.5		0.57	1.5	mV
				Full range			6.5			4.5	
			TL032AM	25°C		0.53	2.8		0.39	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL032M	25°C to 125°C		9.7			9.7		µV/°C
			TL032AM	25°C to 125°C		9.7			9.7		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	− 1.5 to 4	− 3.4 to 5.4		− 11.5 to 14	− 13.4 to 15.4		V
				Full range	− 1.5 to 4			− 11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ		25°C	3	4.3		13	14		V
				− 55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ		25°C	− 3	− 4.2		− 12.5	− 13.9		V
				− 55°C	− 3	− 4		− 12.5	− 13.8		
				125°C	− 3	− 4.3		− 12.5	− 14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10$ kΩ, See Note 7		25°C	4	12		5	14.3		V/mV
				− 55°C	3	7.1		4	10.4		
				125°C	4	12.9		5	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				− 55°C	70	87		75	94		
				125°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				− 55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, $V_O = 0$		25°C		3.8	5		13	17	mW
				− 55°C		2.3	5		9.4	17	
				125°C		3.6	5		11.8	17	
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		384	500		434	560	µA
				− 55°C		228	500		312	560	
				125°C		356	500		394	560	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

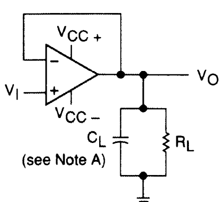
NOTE 7. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR+	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/µs
					−55°C		1.4		1.2	1.9		
					125°C		2.4		2	3.5		
SR−	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/µs
					−55°C		3.2		3.2	4.6		
					125°C		4.1		3.2	4.7		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL032M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AM		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

NOTE 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

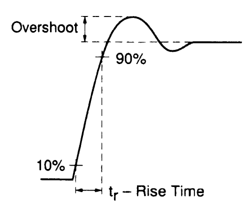


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

PARAMETER MEASUREMENT INFORMATION

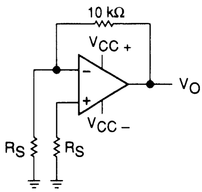
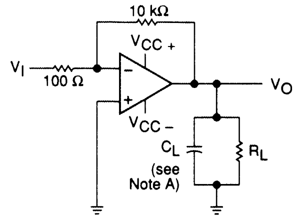


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

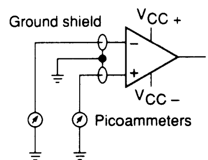


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL032 and TL032A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test is performed which measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sampie-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet your application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

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3 Operational Amplifiers

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE

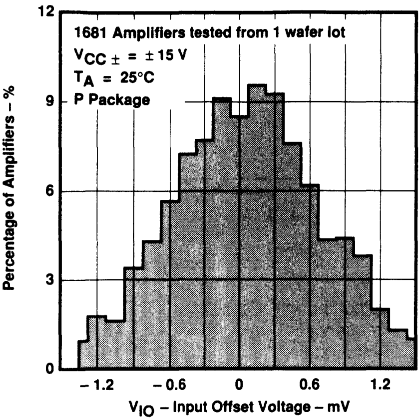


FIGURE 6

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

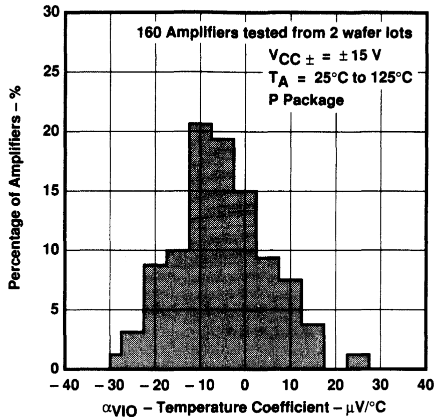


FIGURE 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

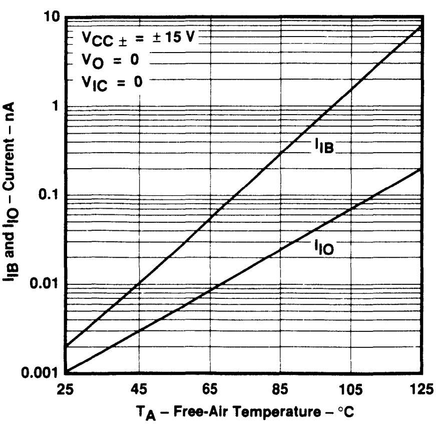


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

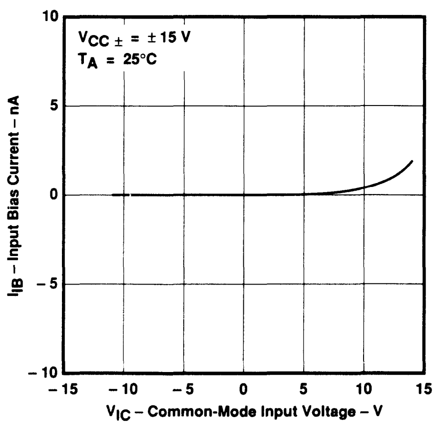


FIGURE 9

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

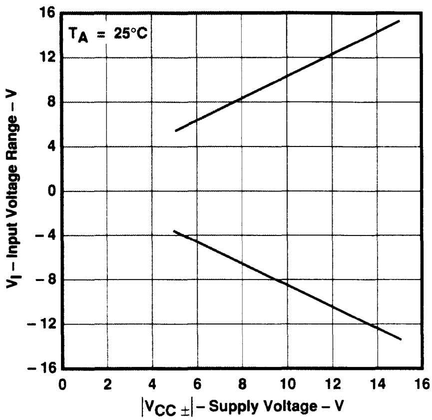


FIGURE 10

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

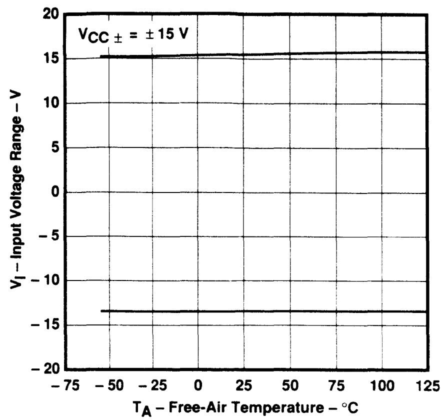


FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

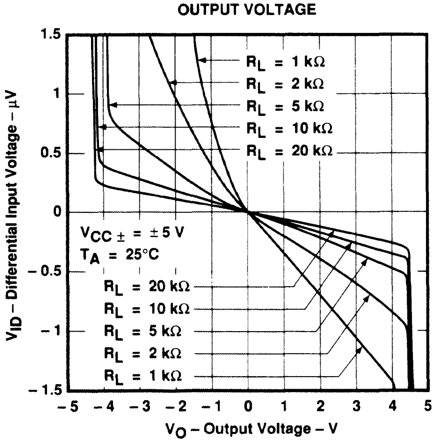


FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

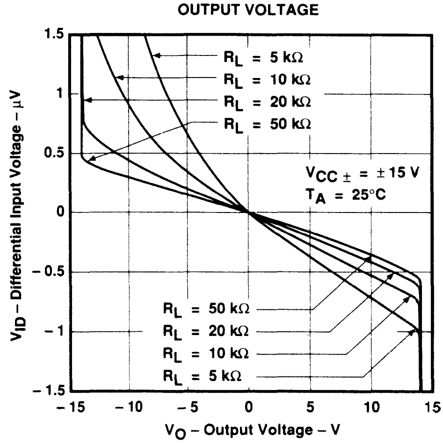


FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

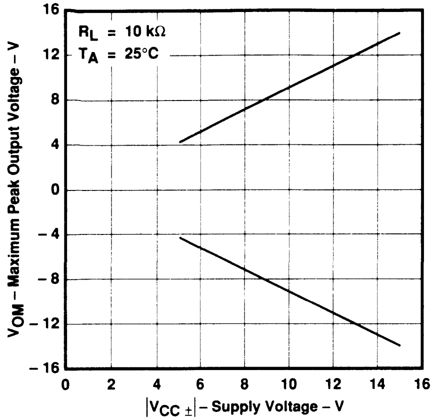


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

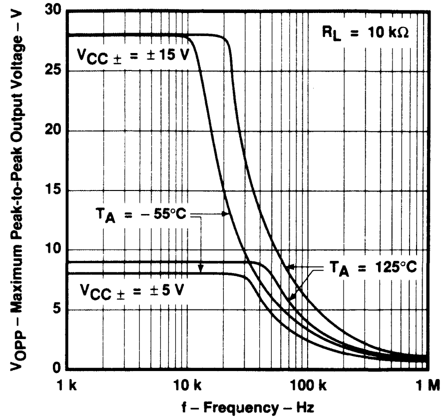


FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

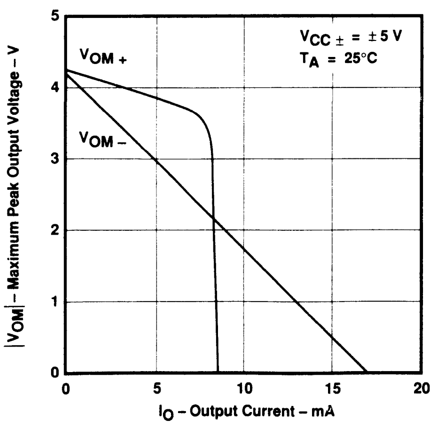


FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

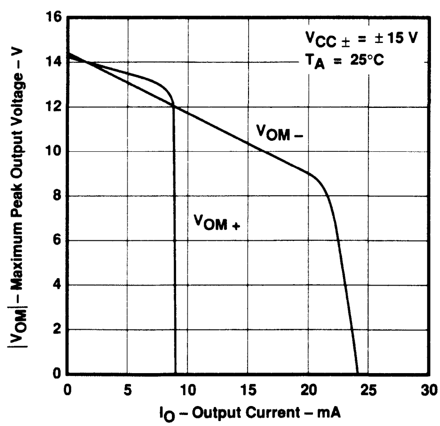


FIGURE 17

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

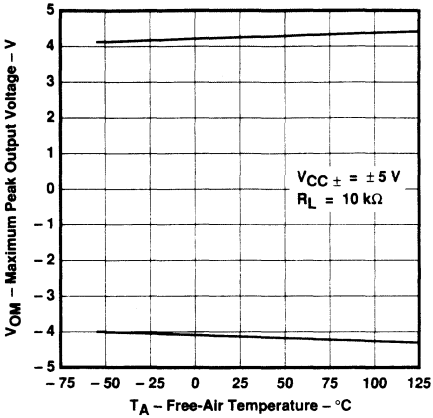


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

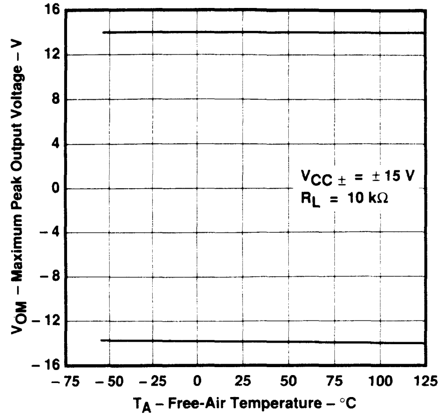


FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

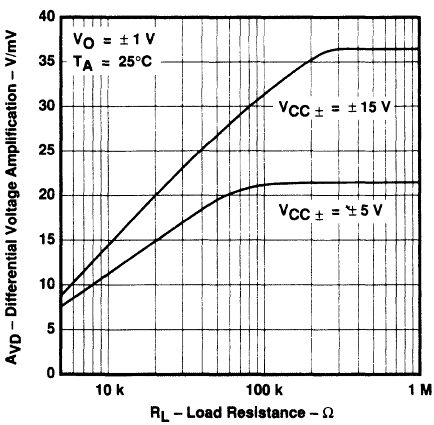


FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

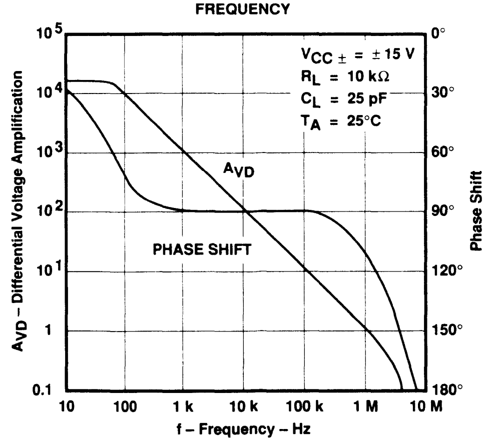


FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

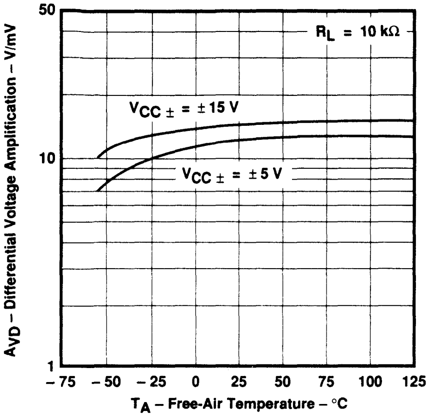


FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

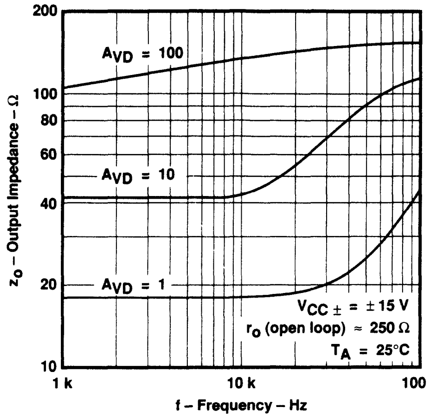


FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

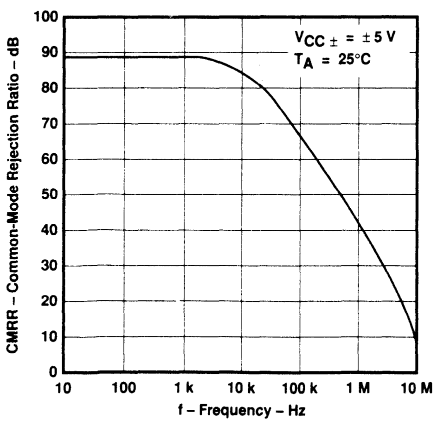


FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

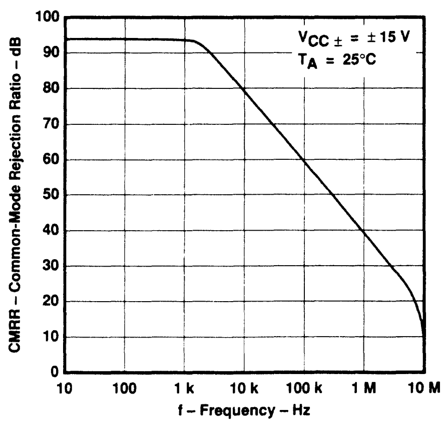


FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

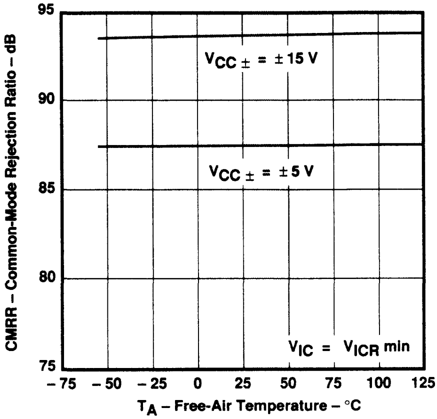


FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

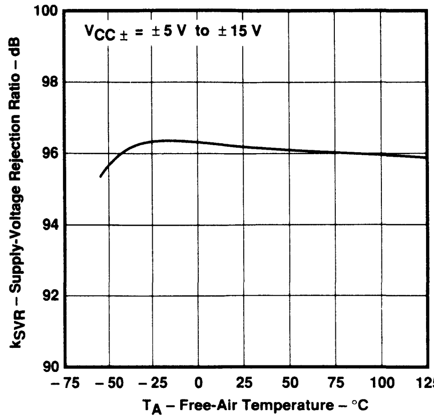


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

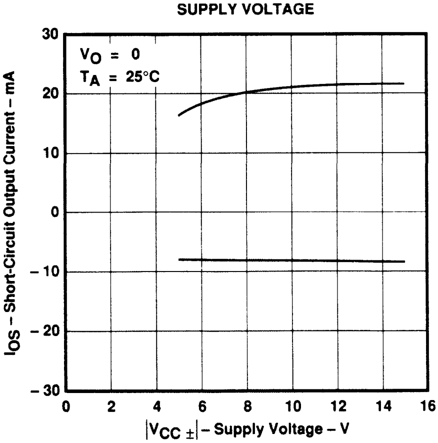


FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

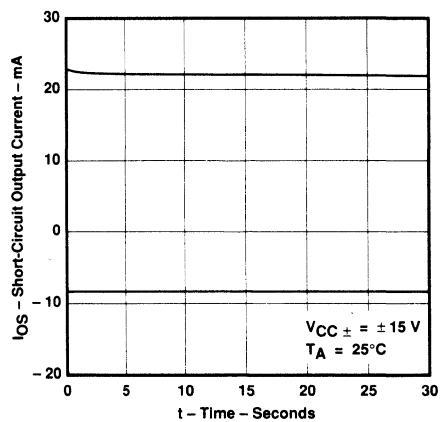


FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

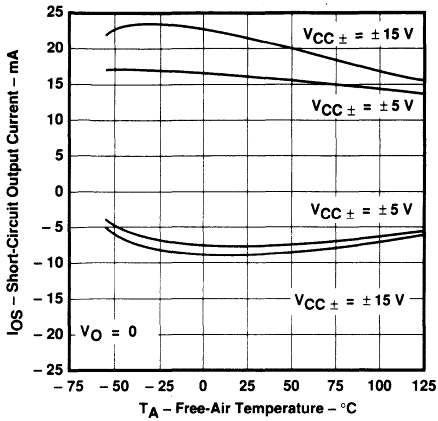


FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

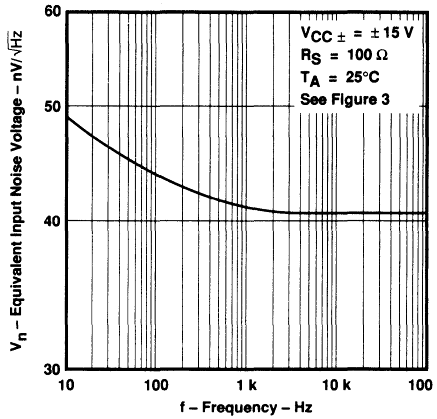


FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

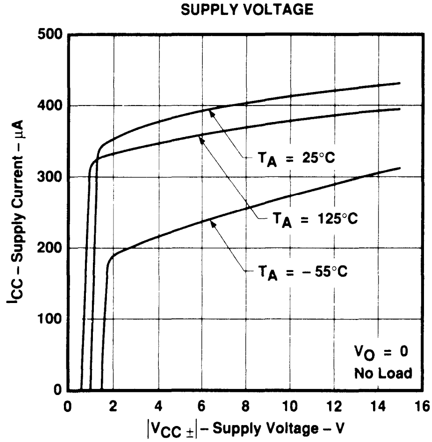


FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

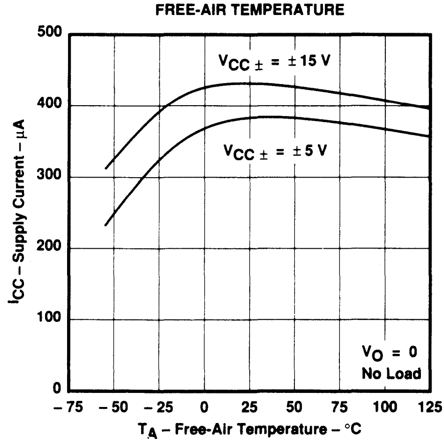


FIGURE 33

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

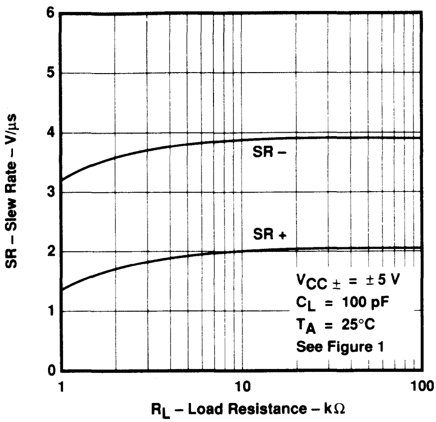


FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

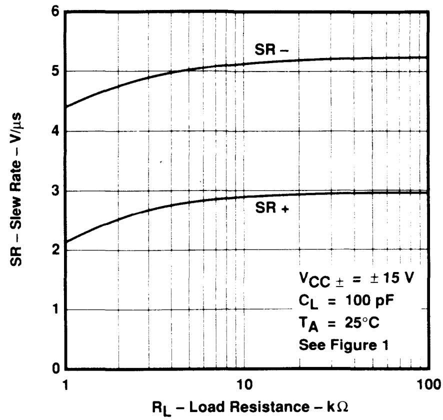


FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

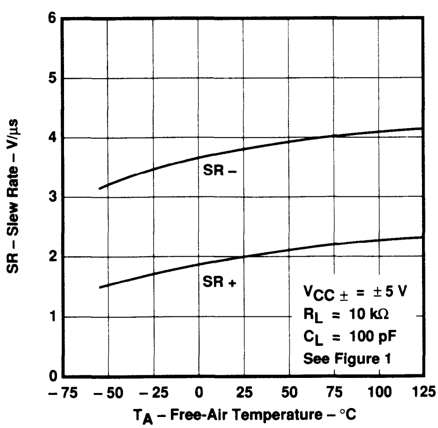


FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

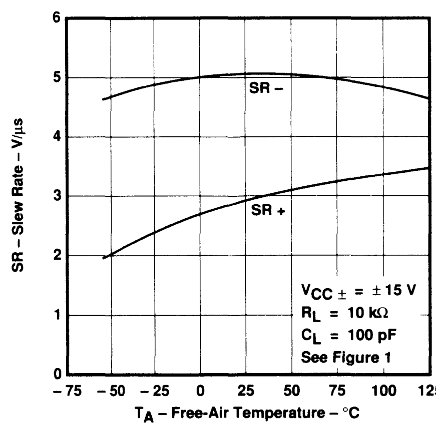


FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

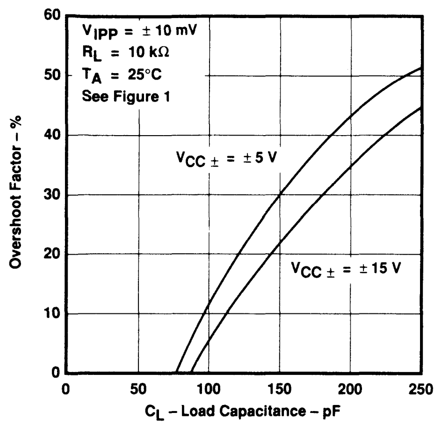


FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

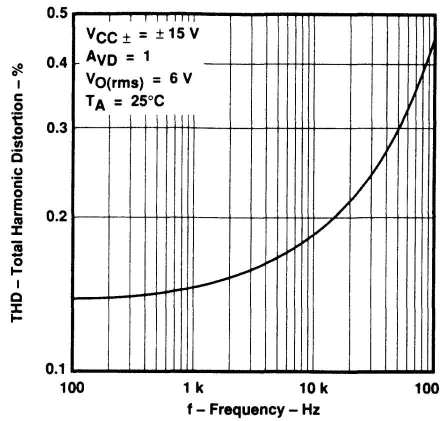


FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

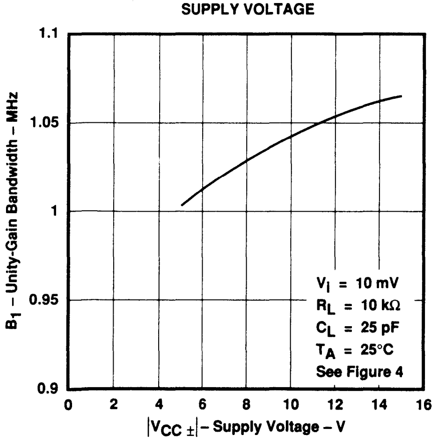


FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

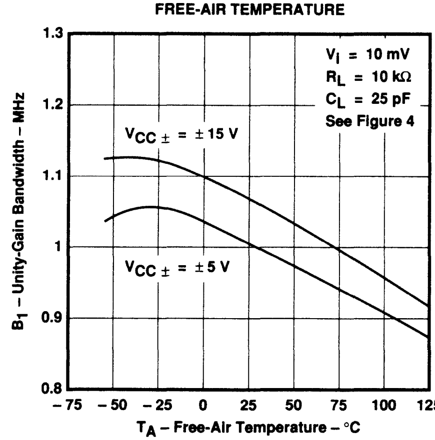


FIGURE 41

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

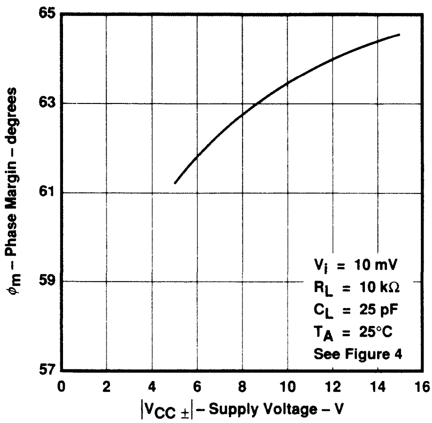


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

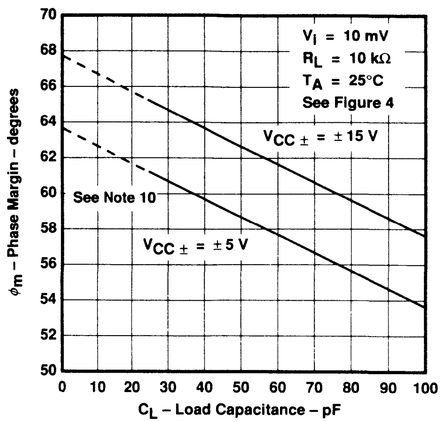


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

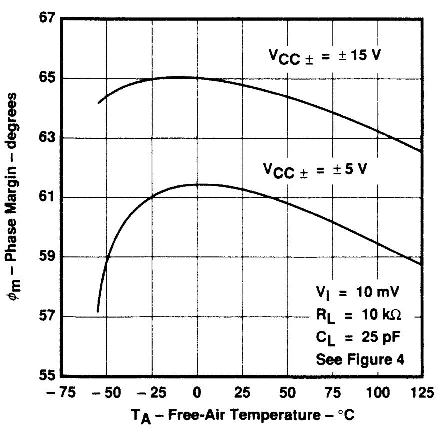


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

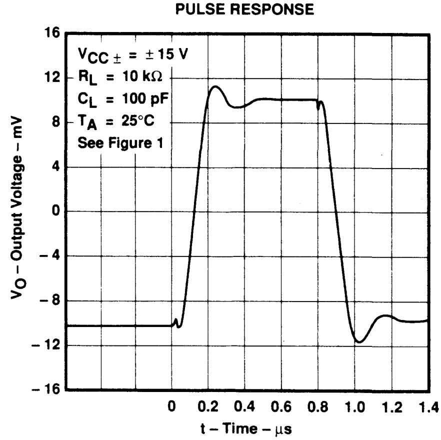


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

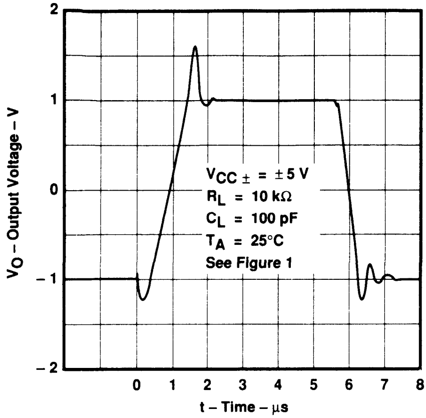


FIGURE 46

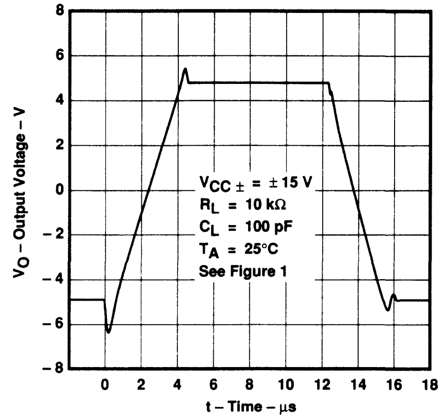


FIGURE 47

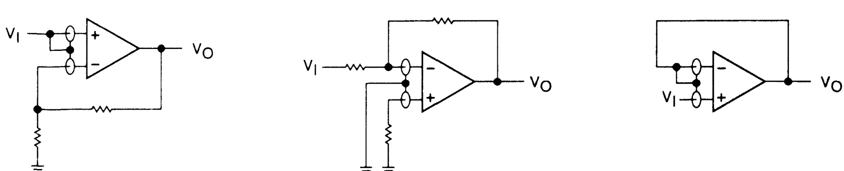
TYPICAL APPLICATION DATA

input characteristics

The TL032 and TL032A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL032 and TL032A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



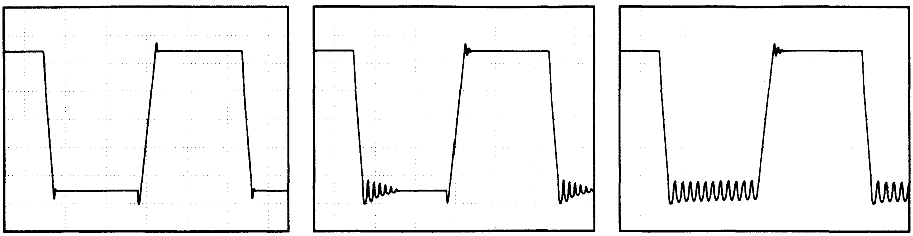
(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

FIGURE 48. USE OF GUARD RINGS

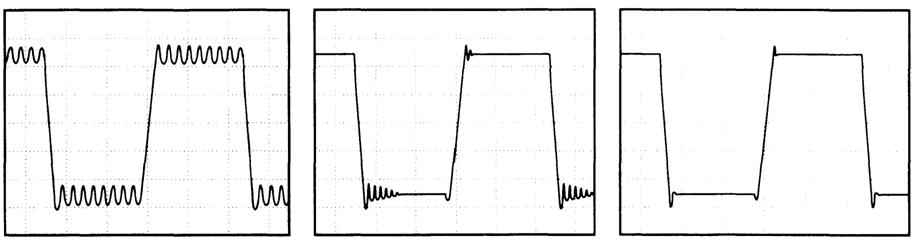
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL032 and TL032A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

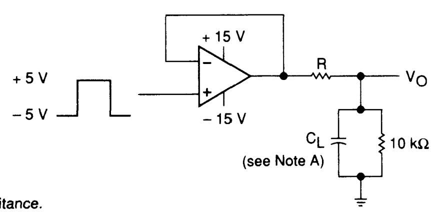


(a) C_L = 100 pF, R = 0 **(b)** C_L = 300 pF, R = 0 **(c)** C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 **(e)** C_L = 1000 pF, R = 50 Ω **(f)** C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

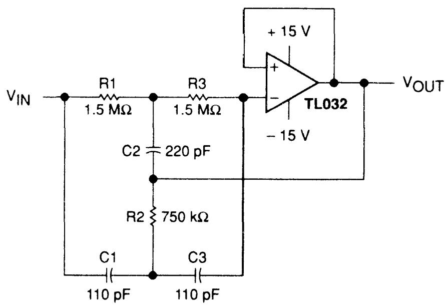
TYPICAL APPLICATION DATA

high-Q notch filter

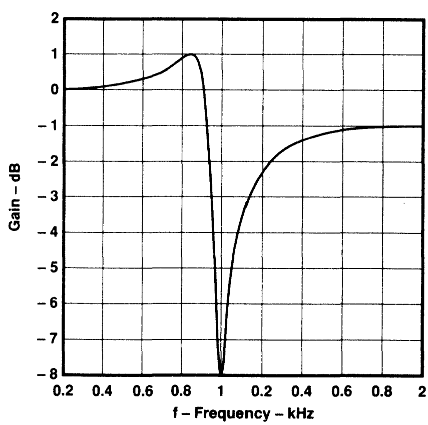
In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. This circuit provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown below, the center frequency is 1 kHz. Note that C1 = C3 = C2 ÷ 2 and also that R1 = R3 = 2 × R2. The center frequency can be modified by varying these values. When adjusting the center frequency, be sure that the operational amplifier still has sufficient gain at the frequency of interest.



HIGH-Q NOTCH FILTER



TYPICAL APPLICATION DATA

2 wire 4- to 20-mA current loop

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications the most feasible method involves converting voltage information to a current before transmission. The following circuit benefits from the high input impedance of the TL032A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the TL032A's non-inverting input is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA}$$

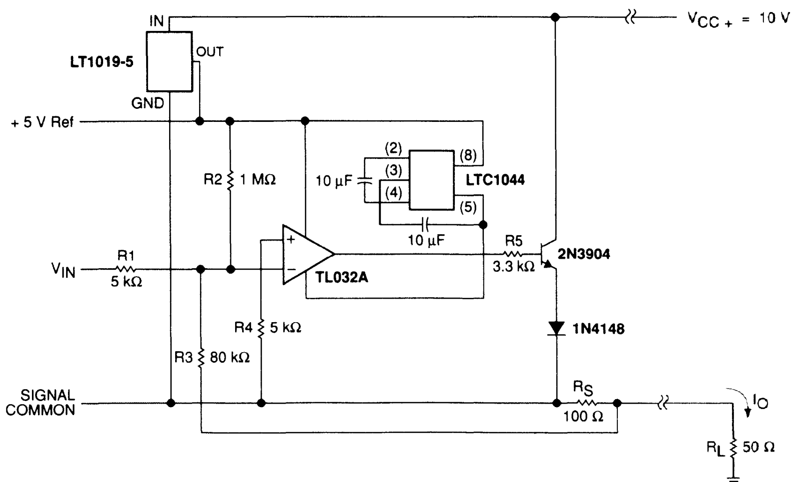
The current presently provides 4 to 20 mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3 the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL032A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\,V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\text{ mA} - 0.17 \times V_{IO}$$

For example, an offset voltage of 1 mV will decrease the output current by 0.17 mA.

Thanks to the low-power consumption of the TL032A, this circuit has at least 2 mA available to drive the actual sensor from the 5-V reference node.

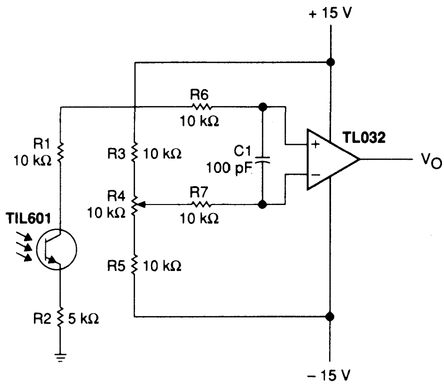


TYPICAL APPLICATION DATA

low-level light detector preamplifier

Applications that need to detect small currents require high input impedance operational amplifiers; otherwise, the bias currents of the operational amplifier will camoflauge the current being monitored. Phototransistors provide a current that is proportional to the light reaching the transistor. The TL032 allows even the small currents resulting from low-level light to be detected.

In this circuit if there is no light, the phototransistor will be off and the output will be high. As light is detected, the operational amplifier output will begin pulling low. Adjusting R4 will both compensate for offset voltage of the amplifier and also adjust the point of light detection by the amplifier.

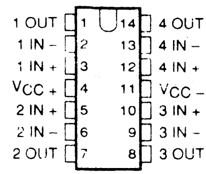


ENHANCED JFET LOW-POWER LOW-OFFSET QUAD OPERATIONAL AMPLIFIERS

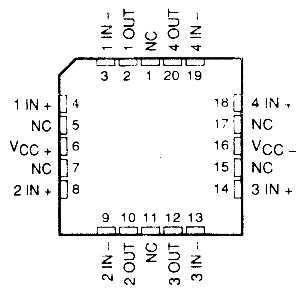
JULY 1988

- **Maximum Offset Voltage . . . 1.5 mV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 26 mW Typ**
- **Output Short-Circuit Protection**
- **Monolithic Construction**

D, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

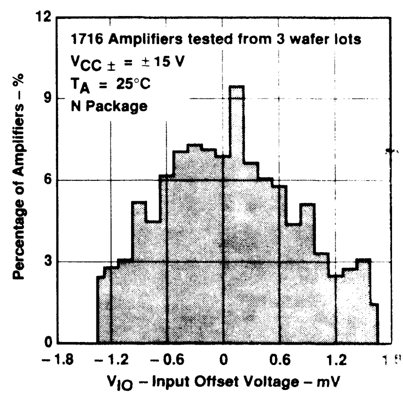
The TL034 and TL034A quadruple operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low power consumption make the TL034 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL034 has been designed to be functionally compatible and pin compatible with the TL064.

Two offset voltage grades are available:
TL034 (4 mV max) and TL034A (1.5 mV max).

A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

DISTRIBUTION OF TL034A INPUT OFFSET VOLTAGE



AVAILABLE OPTIONS

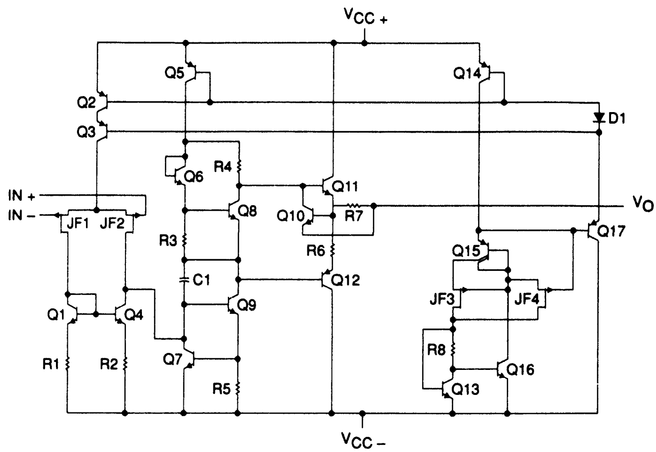
T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	1.5 mV	TL034ACD	TL034ACN	TL034ACJ	—
	4 mV	TL034CD	TL034CN	TL034CJ	—
– 40°C to 85°C	1.5 mV	TL034AID	TL034AIN	TL034AIJ	—
	4 mV	TL034ID	TL034IN	TL034IJ	—
– 55°C to 125°C	1.5 mV	—	—	TL034AMJ	TL034AMFK
	4 mV	—	—	TL034MJ	TL034MFK

NOTE 1: D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TL034CDR).

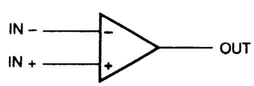
description (continued)

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 2) . . . 18 V
Supply voltage, V_{CC-} (see Note 2) . . . – 18 V
Differential input voltage (see Note 3) . . . ± 30 V
Input voltage range, V_I (any input, see Notes 2 and 4) . . . ± 15 V
Input current, I_I (each input) . . . ± 1 mA
Output current, I_O (each output) . . . ± 80 mA
Total current into V_{CC+} terminal . . . 160 mA
Total current out of V_{CC-} terminal . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 5) . . . Unlimited
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M- suffix . . . – 55°C to 125°C
I- suffix . . . – 40°C to 85°C
C- suffix . . . 0°C to 70°C
Storage temperature range . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
5. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M- SUFFIX			I- SUFFIX			C- SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	V
Input voltage, V_I	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034C	25°C		0.91	6		0.79	4	mV
				Full range			8.2			6.2	
			TL034AC	25°C		0.7	3.5		0.58	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL034C	25°C to 70°C		11.6			12		μV/°C
			TL034AC	25°C to 70°C		11.6			12	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 7		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				0°C		7.4	10		25.3	34	
				70°C		7.6	10		25.2	34	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		0.87	1.12	mA
				0°C		0.74	1		0.85	1.12	
				70°C		0.76	1		0.84	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTES: 6. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8	25°C		2		2	2.9		V/μs
			0°C		1.8		1.5	2.6		
			70°C		2.2		2	3.2		
SR −	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/μs
			0°C		3.7		3.2	4.9		
			70°C		4		3.2	5		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			0°C		134			127		
			70°C		150			142		
t_f	Fall time		25°C		138			132		ns
			0°C		134			127		
			70°C		150			142		
	Overshoot factor		25°C		11%			5%		
			0°C		10%			4%		
			70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9) — TL034C	R_S = 100 Ω, See Figure 3; f = 10 Hz	25°C		83			83		nV/√Hz
	TL034C	f = 1 kHz			43			43		
	TL034AC	f = 10 Hz	25°C		83			83		
	TL034AC	f = 1 kHz			43			43	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			0°C		1			1.1		
			70°C		1			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			0°C		61°			65°		
			70°C		60°			64°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS			$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
				T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034I	25°C		0.91	6		0.79	4	mV
				Full range			9.3			7.3	
			TL034AI	25°C		0.7	3.5		0.58	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL034I	25°C to 85°C		11.5			11.6		µV/°C
			TL034AI	25°C to 85°C		11.5			11.6	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, See Note 7		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				−40°C		5.8	10		21.7	34	
				85°C		7.4	10		24.8	34	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		0.87	1.12	mA
				−40°C		0.58	1		0.72	1.12	
				85°C		0.74	1		0.83	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTES: 6. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8	25°C		2		2	2.9		V/µs
			– 40°C		1.5		1.5	2.1		
			85°C		2.3		2	3.3		
SR –	Negative slew rate at unity gain		25°C		3.9		3.5	5.1		V/µs
			– 40°C		3.4		3.2	4.8		
			85°C		4.1		3.2	4.9		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2	25°C		138			132		ns
			– 40°C		132			123		
			85°C		154			146		
t_f	Fall time		25°C		138			132		ns
			– 40°C		132			123		
			85°C		154			146		
	Overshoot factor		25°C		11%			5%		
			– 40°C		12%			5%		
			85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9), TL034I	R_S = 100 Ω, See Figure 3, f = 10 Hz	25°C		83			83		nV/√Hz
		f = 1 kHz			43			43		
	TL034AI	f = 10 Hz	25°C		83			83		
		f = 1 kHz			43			43	60	
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		1			1.1		MHz
			– 40°C		1			1.1		
			85°C		0.9			1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4	25°C		61°			65°		
			– 40°C		60°			65°		
			85°C		60°			64°		

NOTES: 8. For $V_{CC\pm}$ = ± 5 V, V_{IPP} = ± 1 V; for $V_{CC\pm}$ = ± 15 V, V_{IPP} = ± 5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL034M	25°C		0.91	6		0.78	4	mV
				Full range			11			9	
			TL034AM	25°C		0.7	3.5		0.58	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL034M	25°C to 125°C		10.6			10.9		µV/°C
			TL034AM	25°C to 125°C		10.6			10.9		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	$R_L = 10$ kΩ, See Note 7		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	4	12.9		5	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	70	87		75	94		dB
				−55°C	70	87		75	94		
				125°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, $V_O = 0$		25°C		7.7	10		26	34	mW
				−55°C		4.6	10		18.7	34	
				125°C		7.1	10		23.6	34	
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		0.77	1		0.87	1.12	mA
				−55°C		0.46	1		0.62	1.12	
				125°C		0.71	1		0.79	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

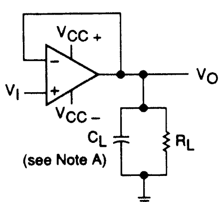
NOTE 7. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR+	Positive slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		2		2	2.9		V/µs
				−55°C		1.4		1.2	1.9		
				125°C		2.4		2	3.5		
SR−	Negative slew rate at unity gain			25°C		3.9		3.5	5.1		V/µs
				−55°C		3.2		3.2	4.6		
				125°C		4.1		3.2	4.7		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
				−55°C		142			123		
				125°C		166			158		
t_f	Fall time			25°C		138			132		ns
				−55°C		142			123		
				125°C		166			158		
	Overshoot factor			25°C		11%			5%		
				−55°C		16%			6%		
				125°C		14%			8%		
V_n	Equivalent input noise voltage, TL034M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
			f = 1 kHz			43			43		
	Equivalent input noise voltage, TL034AM		f = 10 Hz	25°C		83			83		
			f = 1 kHz			43			43		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
				−55°C		1			1.1		
				125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
				−55°C		57°			64°		
				125°C		59°			62°		

NOTE 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

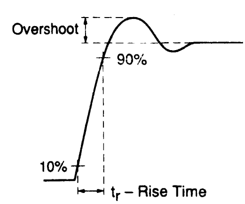


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

PARAMETER MEASUREMENT INFORMATION

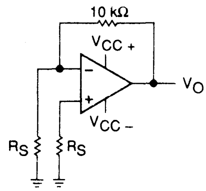
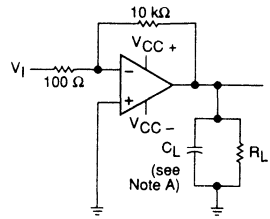


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

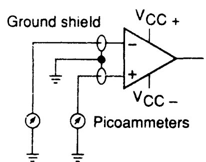


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL034 and TL034A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test is performed which measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet your application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

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CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	24, 25 26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
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I_{CC}	Supply current	vs V_{CC} vs Temperature	32 33
SR	Slew rate	vs R_L vs Temperature	34, 35 36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	40 41
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	42 43 44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal Large-signal	45 46, 47

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE

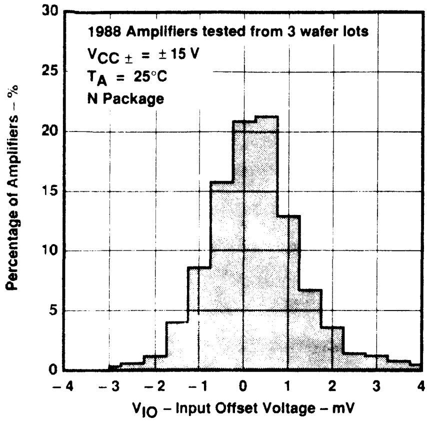


FIGURE 6

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

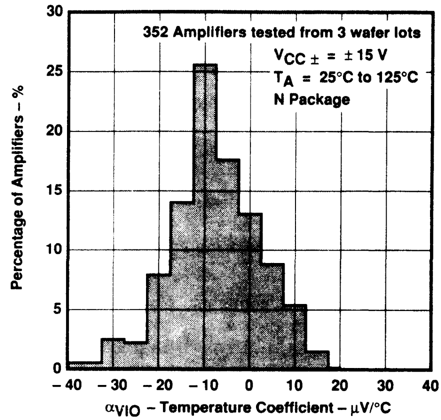


FIGURE 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

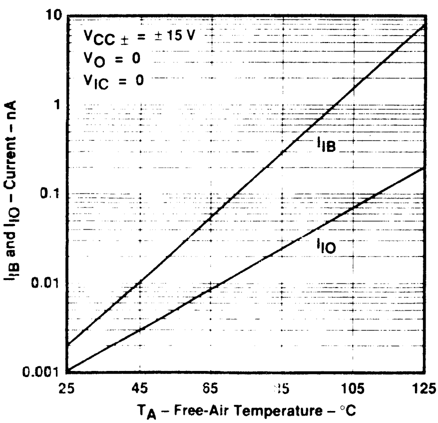


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

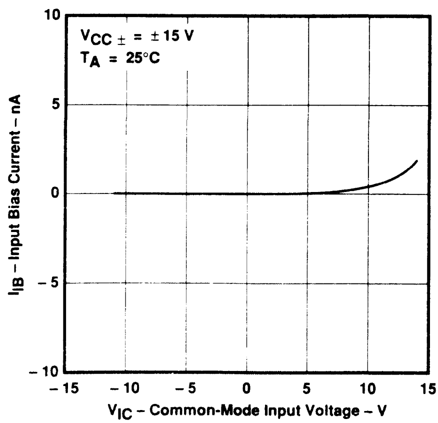


FIGURE 9

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

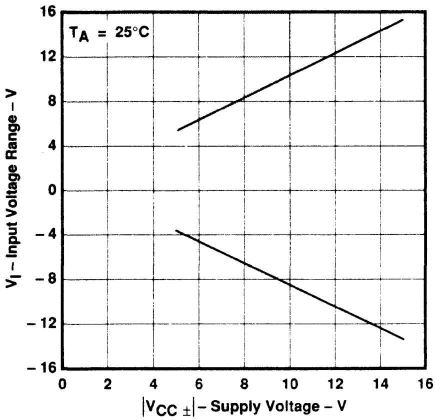


FIGURE 10

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

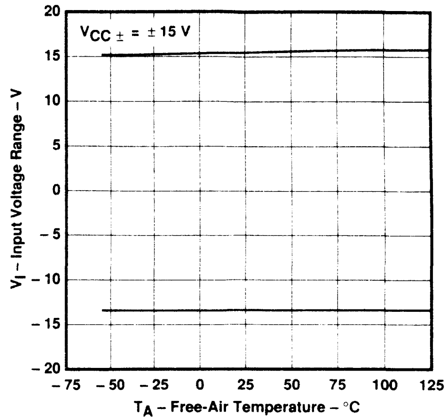


FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

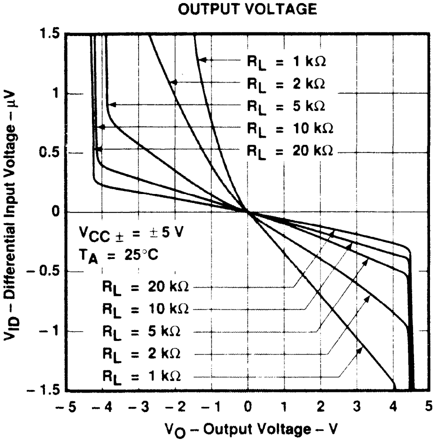


FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

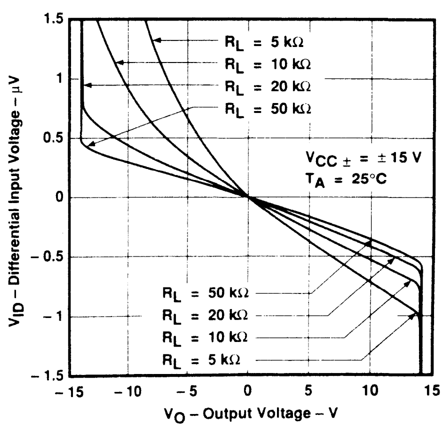


FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

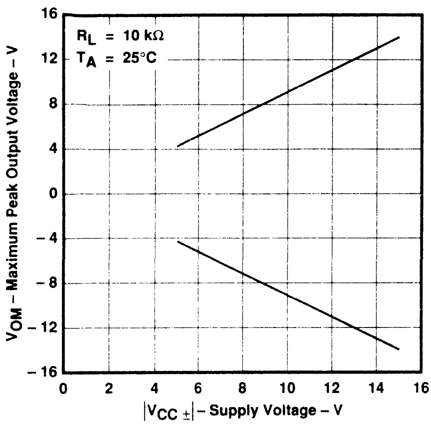


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

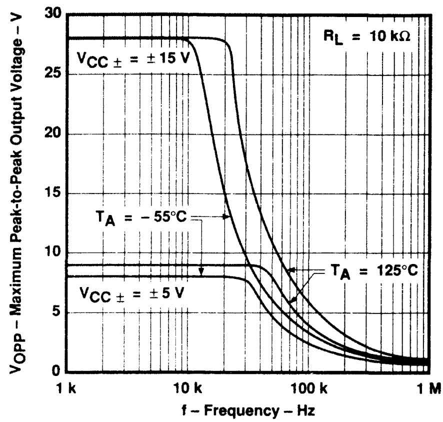


FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

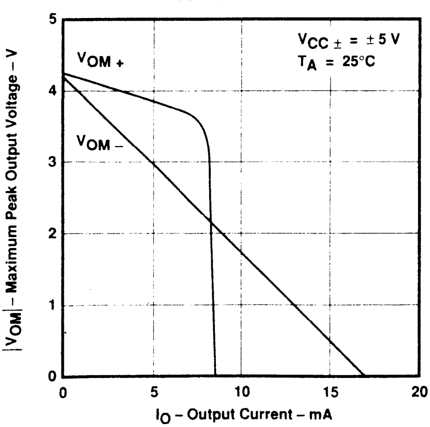


FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

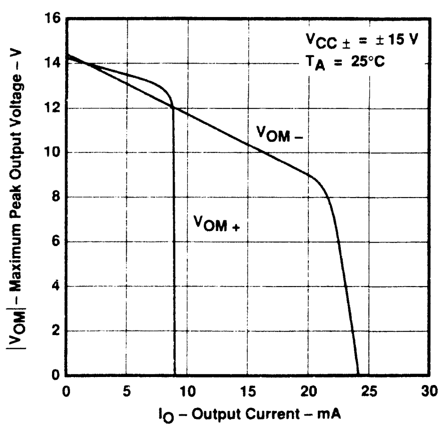


FIGURE 17

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

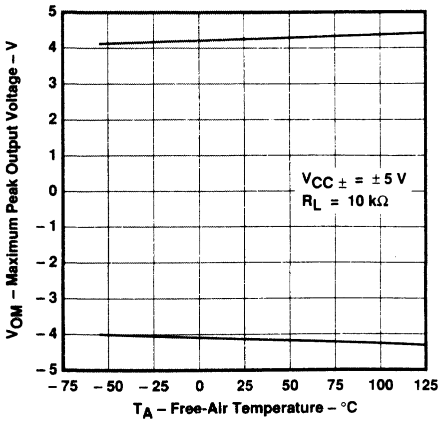


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

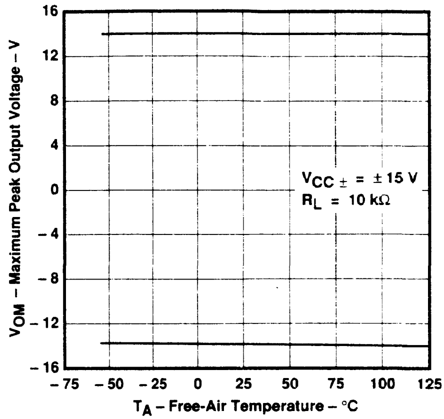


FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

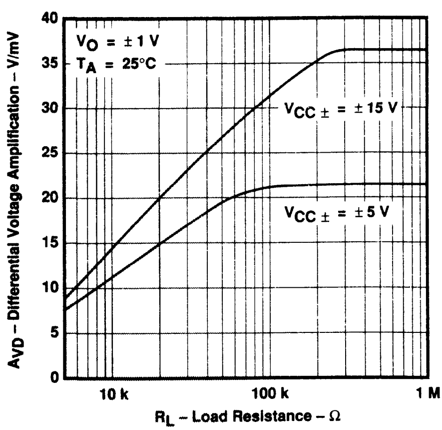


FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

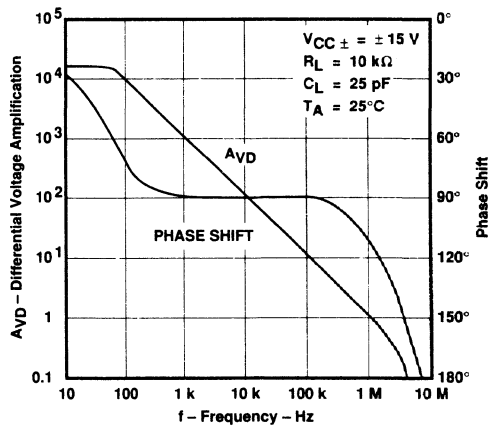


FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

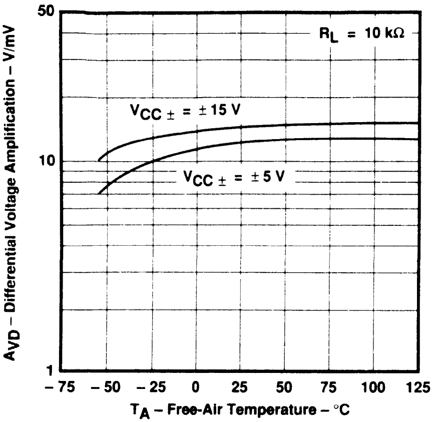


FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

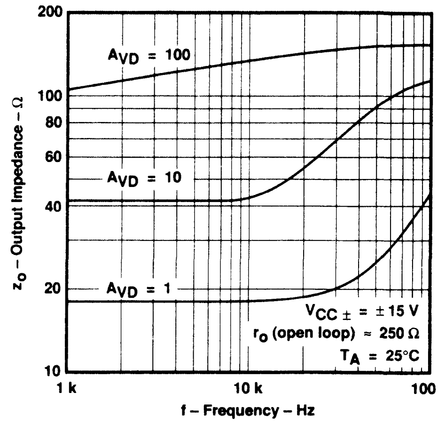


FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

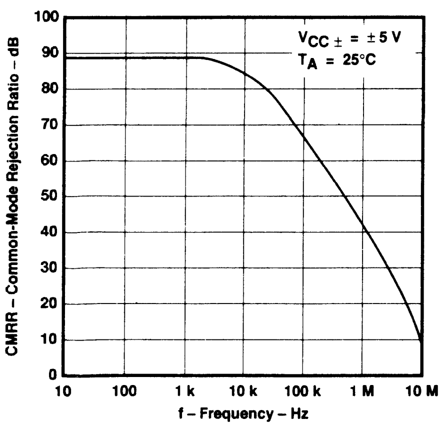


FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

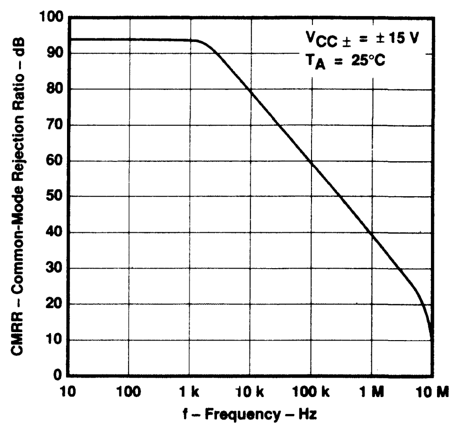


FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

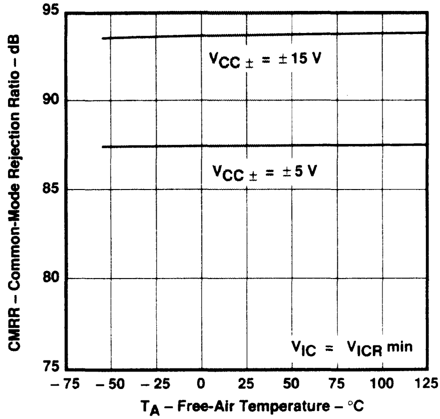


FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

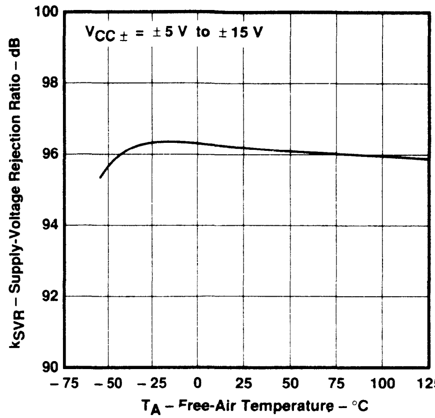


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

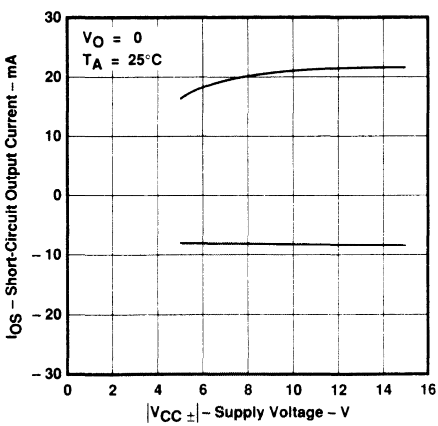


FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

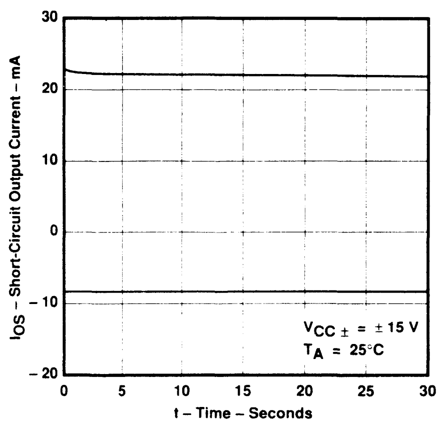


FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

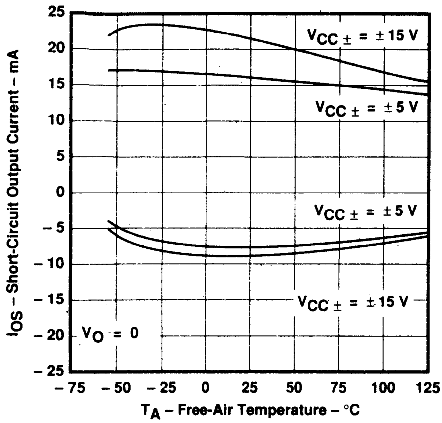


FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

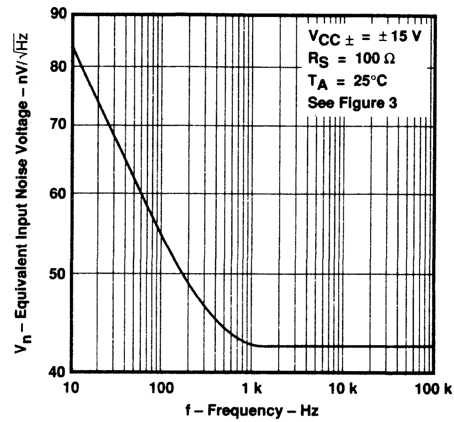


FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

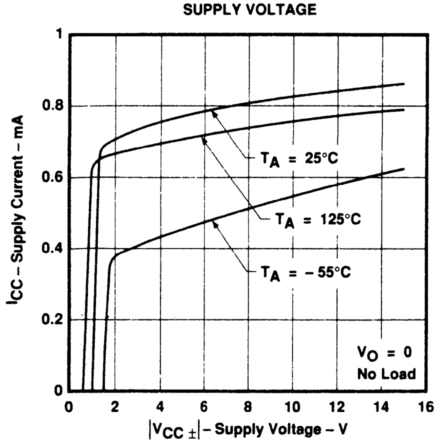


FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

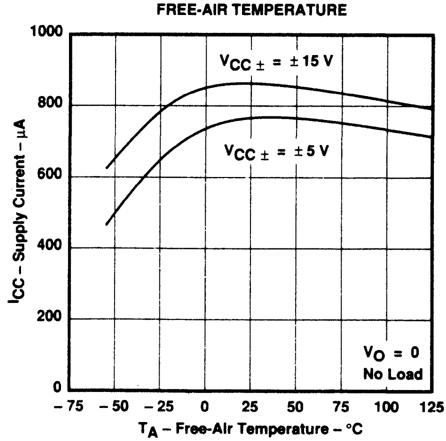


FIGURE 33

TYPICAL CHARACTERISTICS

SLEW RATE vs LOAD RESISTANCE

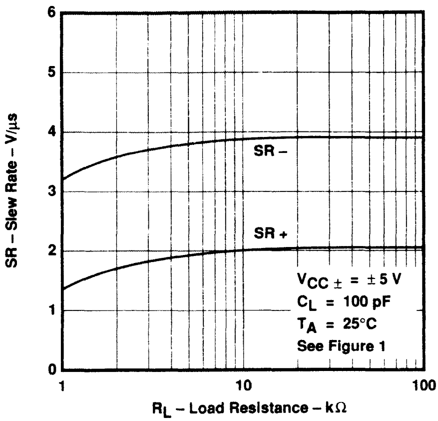


FIGURE 34

SLEW RATE vs LOAD RESISTANCE

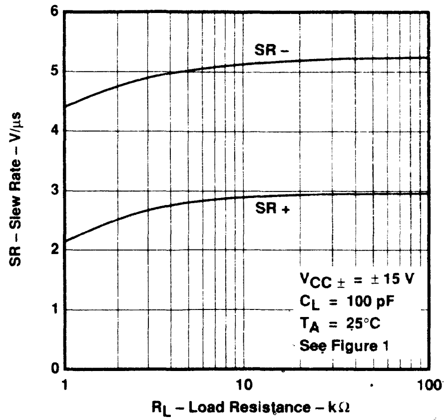


FIGURE 35

SLEW RATE vs FREE-AIR TEMPERATURE

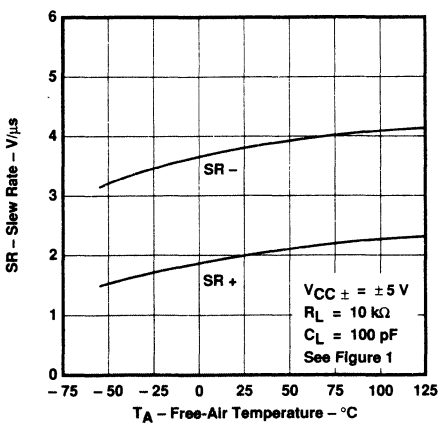


FIGURE 36

SLEW RATE vs FREE-AIR TEMPERATURE

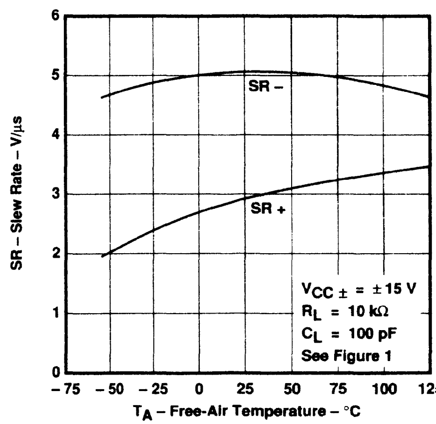


FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR vs LOAD CAPACITANCE

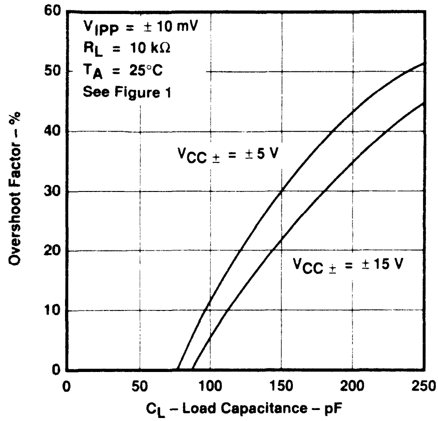


FIGURE 38

TOTAL HARMONIC DISTORTION vs FREQUENCY

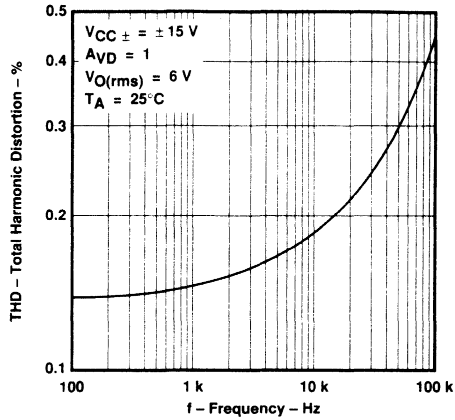


FIGURE 39

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

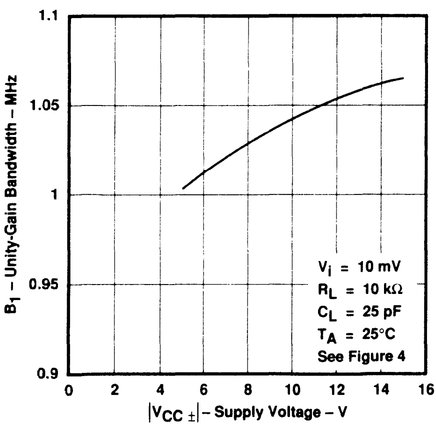


FIGURE 40

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

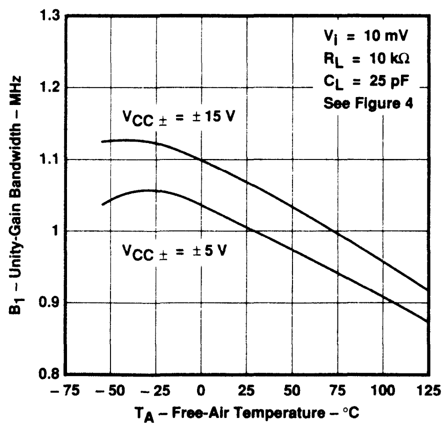


FIGURE 41

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

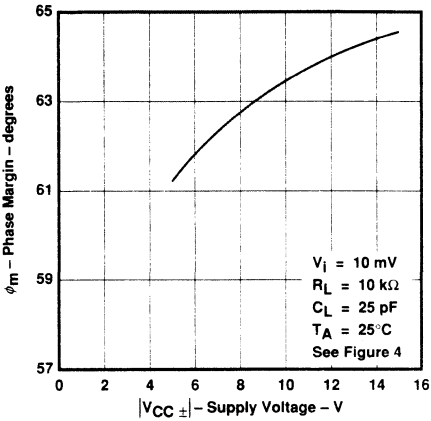


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

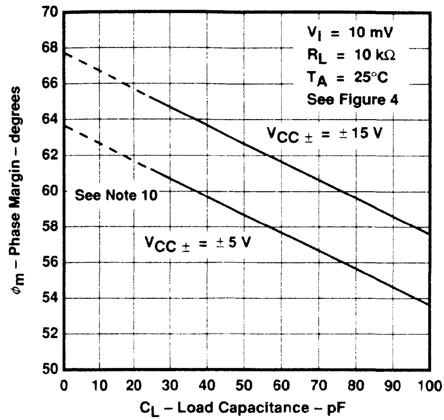


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

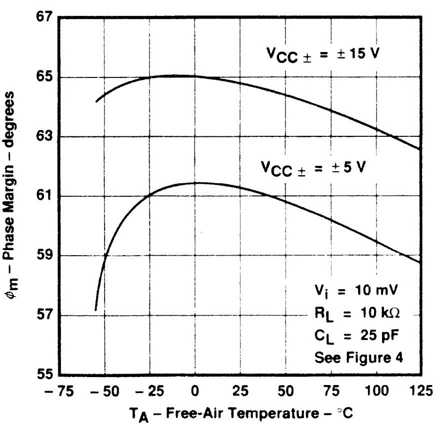


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

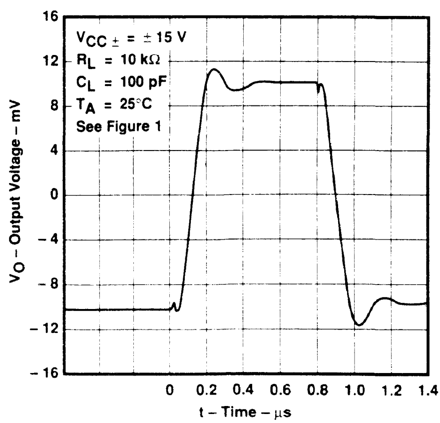


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

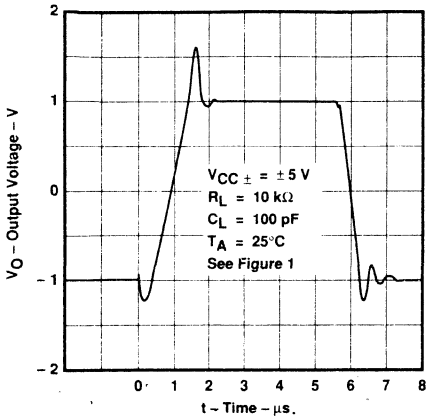


FIGURE 46

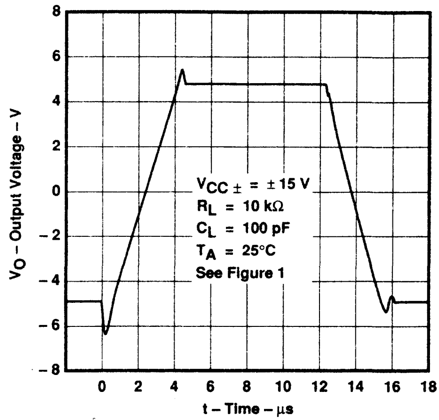


FIGURE 47

TYPICAL APPLICATION DATA

input characteristics

The TL034 and TL034A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL034 and TL034A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage leve' as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

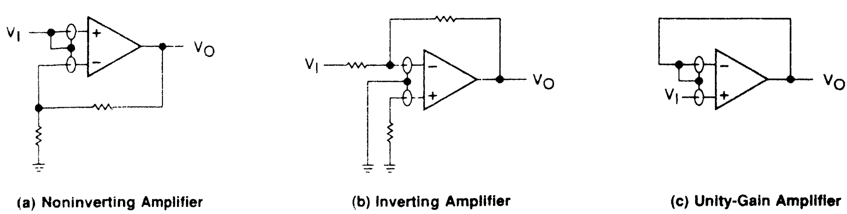
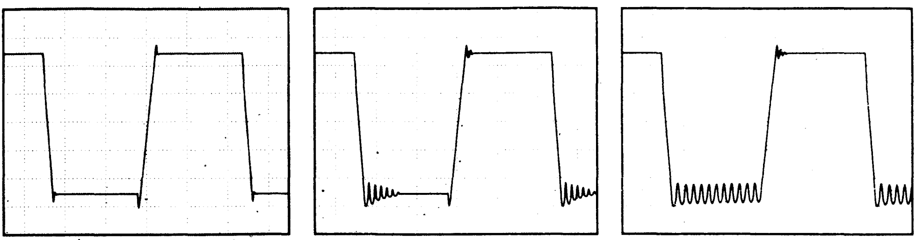


FIGURE 48. USE OF GUARD RINGS

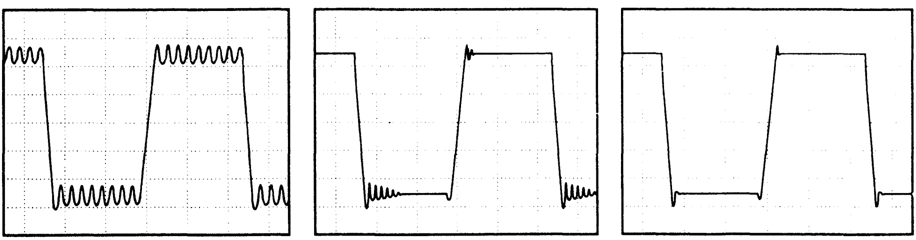
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL034 and TL034A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).

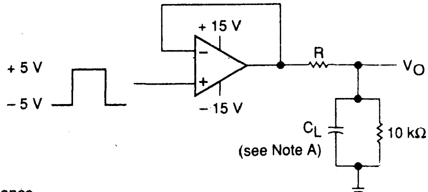


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



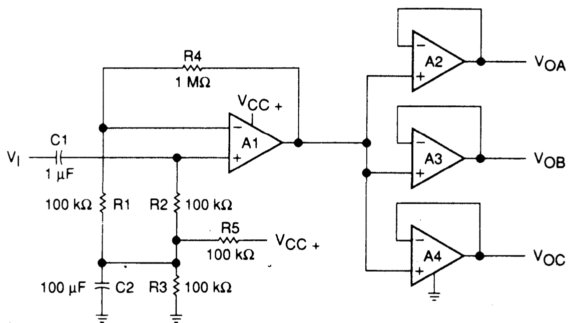
NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

audio distribution amplifier

This audio distribution amplifier feeds the input signal to three separate output channels. A1 amplifies the input signal with a gain of 10 while A2, A3, and A4 serve as buffers to the output channels. The gain response of this circuit is very flat from 20 Hz to 20 kHz. The TL034 allows quick response to the input signal while maintaining low power consumption.



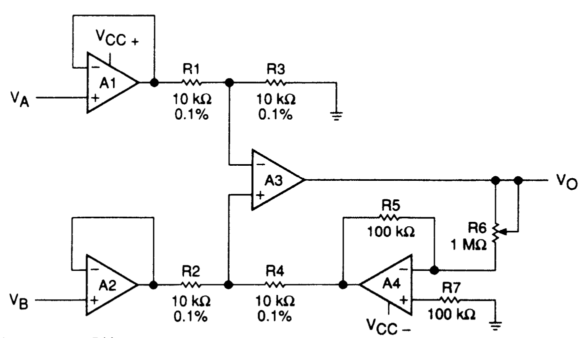
NOTE : A1 through A4 = TL034; V_{CC+} = 5 V.

instrumentation amplifier with linear gain adjust

The TL034 low-offset voltage and low-power consumption provides an accurate but inexpensive instrumentation amplifier. This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R6}{R5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 should always be greater or equal to the value of R5 in order to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors should be 0.1% tolerance resistors.



NOTE : A1 through A4 = TL034; $V_{CC\pm}$ = ± 15 V.

TYPES TL044M, TL044C
QUAD LOW-POWER OPERATIONAL AMPLIFIERS

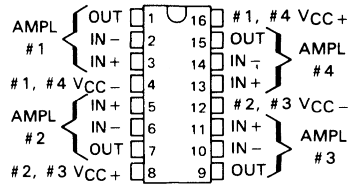
D1662, SEPTEMBER 1973—REVISED AUGUST 1983

NOT RECOMMENDED FOR NEW DESIGN

For new design, see TL064

- **Very Low Power Consumption**
- **Typical Power Dissipation with ±2-V Supplies . . . 340 μW**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Input Offset Voltage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Power Applied in Pairs**

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE
(TOP VIEW)



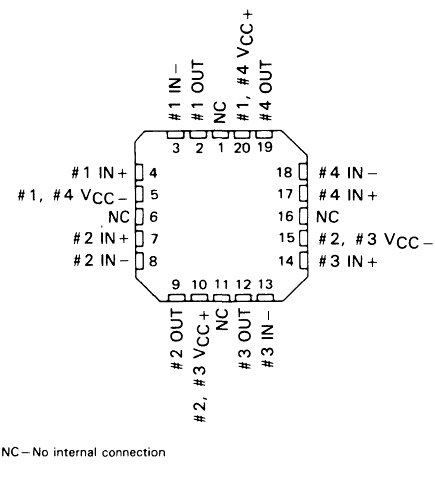
Pins 4 and 12 are internally connected together in the N package only.

description

The TL044 is a quad low-power operational amplifier designed to replace higher-power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use. Power may be applied separately to Section A (amplifiers 1 and 4) or Section B (amplifiers 2 and 3) while the other pair remains unpowered.

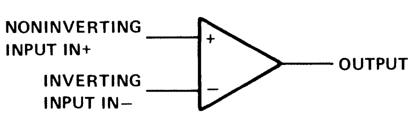
The TL044M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL044C is characterized for operation from 0°C to 70°C.

TL044M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL044M	TL044C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature range (see Note 5)	Each amplifier	500	500	mW
	Total package	680	680	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, J, or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL044M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 85°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the J package, TL044M chips are alloy-mounted; TL044C chips are glass-mounted.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		TL044M MIN	TL044M TYP	TL044M MAX	TL044C MIN	TL044C TYP	TL044C MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current	$V_O = 0$	25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current	$V_O = 0$	25°C		50	100		100	250	nA
			Full range			250			400	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10\ k\Omega$	25°C	20	26		20	26		V
		$R_L \geq 10\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 10\ k\Omega$, $V_O = \pm 10$ V	25°C	72	86		60	80		dB
			Full range	72			60			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C		30	150		30	200	μV/V
			Full range			150			200	
V_n	Equivalent input noise voltage	$A_{VD} = 20$ dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/$\sqrt{Hz}$
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$	25°C		250	400		250	500	μA
			Full range			400			500	
P_D	Total dissipation (four amplifiers)	No load, $V_O = 0$	25°C		7.5	12		7.5	15	mW
			Full range			12			15	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for TL044M is −55°C to 125°C and for TL044C is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL044M MIN	TL044M TYP	TL044M MAX	TL044C MIN	TL044C TYP	TL044C MAX	UNIT
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10\ k\Omega$,		0.3			0.3		μs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10\ k\Omega$, See Figure 1		0.5			0.5		V/μs

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Operational Amplifiers

JUNE 1988

- **Maximum Offset Voltage . . . 800 μV**
- **High Slew Rate . . . 19.8 V/μs Typ**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 18 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

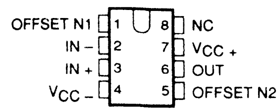
description

The TL051 and TL051A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

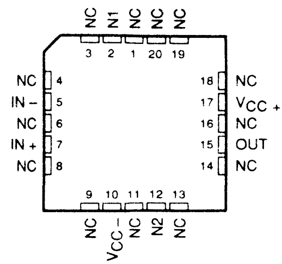
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL051 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL051 has been designed to be functionally compatible as well as pin compatible with the TL071 and TL081.

Two offset voltage grades are available:
TL051 (1.5 mV max) and TL051A (800 μV max).

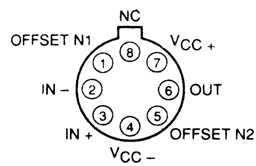
D, JG, or P PACKAGE (TOP VIEW)



FK PACKAGE (TOP VIEW)



L PACKAGE (TOP VIEW)



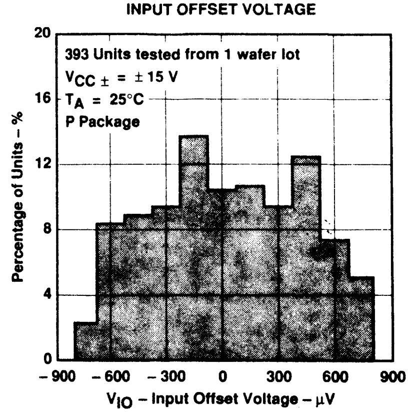
Pin 4 (L Package) is in electrical contact with the case
NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)	Metal Can (L)
0°C to 70°C	800 μV	TL051ACD	TL051ACP	TL051ACJG	—	TL051ACL
	1500 μV	TL051CD	TL051CP	TL051CJG	—	TL051CL
− 40°C to 85°C	800 μV	TL051AID	TL051AIP	TL051AIJG	—	TL051AIL
	1500 μV	TL051ID	TL051IP	TL051IJG	—	TL051IL
− 55°C to 125°C	800 μV	—	—	TL051AMJG	TL051AMFK	TL051AML
	1500 μV	—	—	TL051MJG	TL051MFK	TL051ML

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TL051CDR).

DISTRIBUTION OF TL051A INPUT OFFSET VOLTAGE



ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

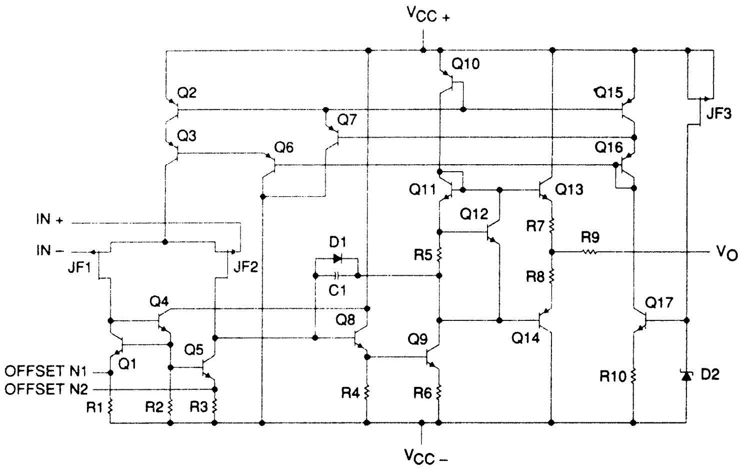
TEXAS INSTRUMENTS

description (continued)

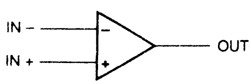
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic



symbol



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 2) .... 18 V
Supply voltage, V_{CC-} (see Note 2) .... – 18 V
Differential input voltage (see Note 3) .... ± 30 V
Input voltage range, V_I (any input, see Notes 2 and 4) .... ± 15 V
Input current, I_I (each input) .... ± 1 mA
Output current, I_O (each output) .... ± 80 mA
Total current into V_{CC+} terminal .... 160 mA
Total current out of V_{CC-} terminal .... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 5) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... – 55°C to 125°C
I-suffix .... – 40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... – 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package .... 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
5. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	
L	650 mW	5.1 mW/°C	421 mW	344 mW	140 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	V
Input voltage, V_I	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

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Operational Amplifiers

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051C	25°C		0.75	3.5		0.59	1.5	mV
				Full range			4.5			2.5	
			TL051AC	25°C		0.55	2.8		0.35	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL051C	25°C to 70°C		8			8		µV/°C
			TL051AC	25°C to 70°C		8			8	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				0°C	3	4.1		13	13.9		
				70°C	3	4.3		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				0°C	2.5	3.8		11.5	12.7		
				70°C	2.5	3.9		11.5	12.8		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				0°C	−2.5	−3.3		−12	−13.1		
				70°C	−2.5	−3.6		−12	−13.4		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				0°C	−2.3	−3.1		−11	−11.9		
				70°C	−2.3	−3.3		−11	−12.1		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 7		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				0°C		2.7	3.2		2.8	3.2	
				70°C		2.6	3.2		2.7	3.2	

NOTES: 6. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		18.2		15	23.7		V/μs
				0°C		19.5		13	24.1		
				70°C		16.4		13	22.6		
SR −	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				0°C		16.8		13	19.9		
				70°C		16		13	19.3		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 10		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				0°C		3.2			3.3		
				70°C		2.7			2.8		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				0°C		58°			62°		
				70°C		59°			62°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.
10. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS			$V_{CC\pm} = \pm5$ V			$V_{CC\pm} = \pm15$ V			UNIT
				T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051I	25°C		0.75	3.5		0.59	1.5	mV
				Full range			5.3			3.3	
			TL051AI	25°C		0.55	2.8		0.35	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL051I	25°C to 85°C		7			8		µV/°C
			TL051AI	25°C to 85°C		8			8	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				−40°C	3	4		13	13.8		
				85°C	3	4.3		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				−40°C	2.5	3.7		11.5	12.6		
				85°C	2.5	3.9		11.5	12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				−40°C	−2.5	−3.2		−12	−12.9		
				85°C	−2.5	−3.8		−12	−13.5		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				−40°C	−2.3	−2.9		−11	−11.8		
				85°C	−2.3	−3.4		−11	−12		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 7		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				−40°C		2.4	3.2		2.6	3.2	
				85°C		2.5	3.2		2.6	3.2	

NOTES: 6. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1, See Note 8		25°C		18.2		15	23.7		V/μs
				– 40°C		20.1		13	23		
				85°C		16.1		13	21.9		
SR –	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				– 40°C		16.6		13	19.4		
				85°C		15.7		13	19.1		
t_r	Rise time	$V_{IPP} = \pm 10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				– 40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	$R_S = 100$ Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz, See Note 10		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		3			3.1		MHz
				– 40°C		3.5			3.6		
				85°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		59°			62°		
				– 40°C		58°			61°		
				85°C		59°			62°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

10. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL051M	25°C		0.75	3.5		0.59	1.5	mV
				Full range			6.5			4.5	
			TL051AM	25°C		0.55	2.8		0.35	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL051M	25°C to 125°C		8			8		µV/°C
			TL051AM	25°C to 125°C		8			8		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				−55°C	3	4		13	13.8		
				125°C	3	4.4		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				−55°C	2.5	3.6		11.5	12.5		
				125°C	2.5	3.9		11.5	12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				−55°C	−2.5	−3.1		−12	−12.9		
				125°C	−2.5	−3.9		−12	−13.6		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				−55°C	−2.3	−2.8		−11	−11.7		
				125°C	−2.3	−3.5		−11	−12		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current	No load, $V_O = 0$		25°C		2.6	3.2		2.7	3.2	mA
				−55°C		2.3	3.2		2.4	3.2	
				125°C		2.4	3.2		2.5	3.2	

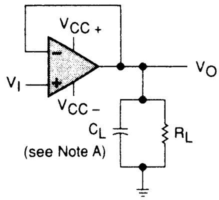
NOTE 6: At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1, See Note 8		25°C		18.2		15	23.7		V/μs
				−55°C		17.5			20		
				125°C		15			21.2		
SR −	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				−55°C		15.1			17		
				125°C		14.8			18.2		
t_r	Rise time	$V_{IPP} = \pm10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				−55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				−55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				−55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz, See Note 10		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		3			3.1		MHz
				−55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		59°			62°		
				−55°C		57°			61°		
				125°C		59°			62°		

NOTES: 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.
10. For $V_{CC\pm} = \pm5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(rms)} = 6$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

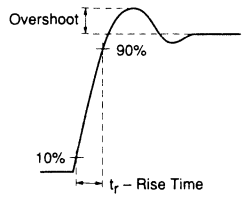


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

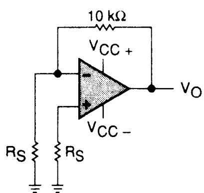
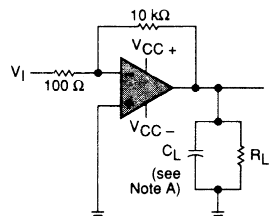


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

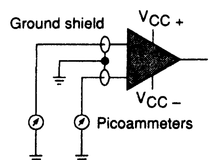


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp bias current level typical of the TL051 and TL051A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test is performed which measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet your application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

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α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC} vs Temperature	9 8
V_I	Input voltage range	vs V_{CC} vs Temperature	10 11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC} vs Output current vs Frequency vs Temperature	14 18, 19 15, 16, 17 20, 21
A_{VD}	Differential voltage amplification	vs R_L vs Frequency vs Temperature	22 23 24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	26, 27 28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC} vs Time vs Temperature	31 32 33
I_{CC}	Supply current	vs V_{CC} vs Temperature	34 35
SR	Slew rate	vs R_L vs Temperature	36, 37 38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC} vs Temperature	43 44
ϕ_m	Phase margin	vs V_{CC} vs C_L vs Temperature	45 46 47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal Large-signal	48 49

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE

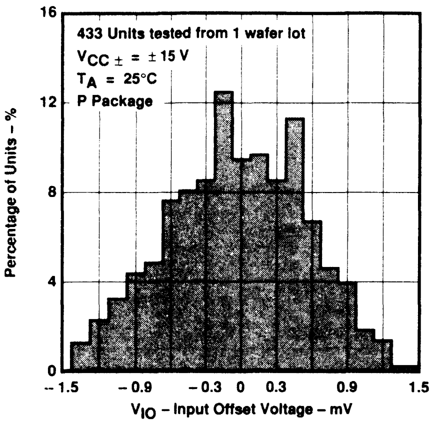


FIGURE 6

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

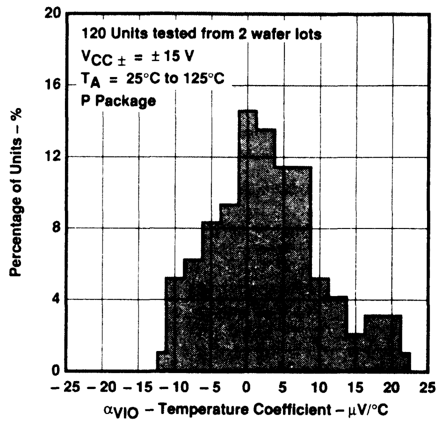


FIGURE 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

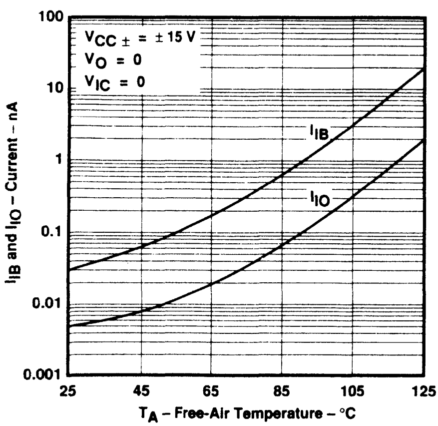


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

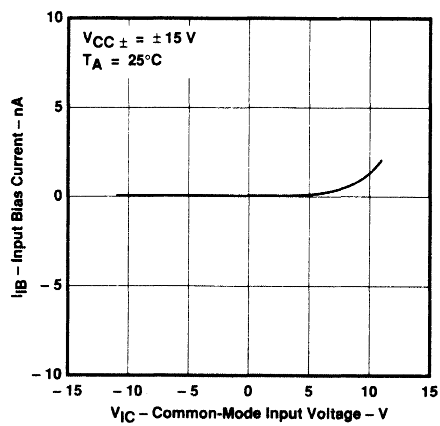


FIGURE 9

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

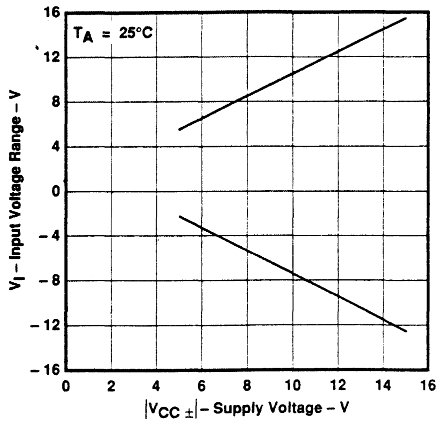


FIGURE 10

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

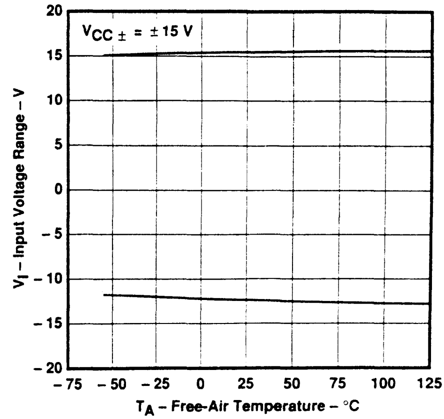


FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

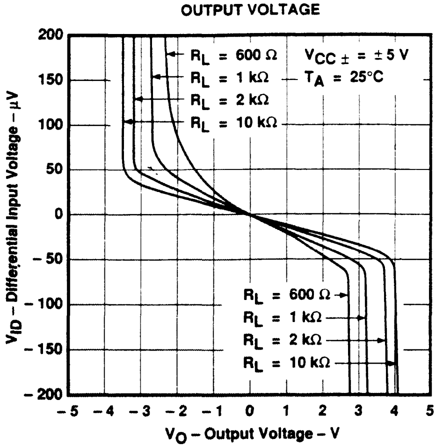


FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

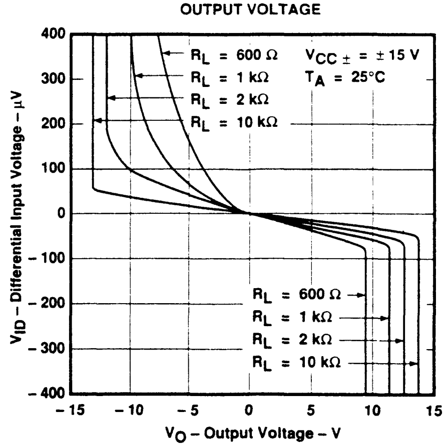


FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

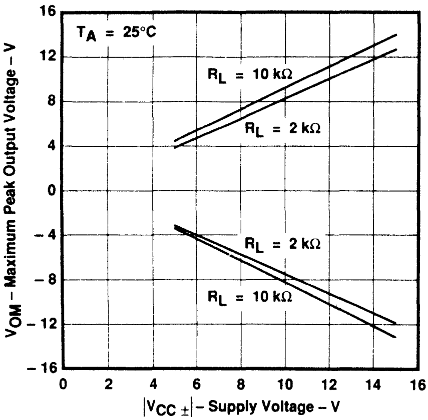


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

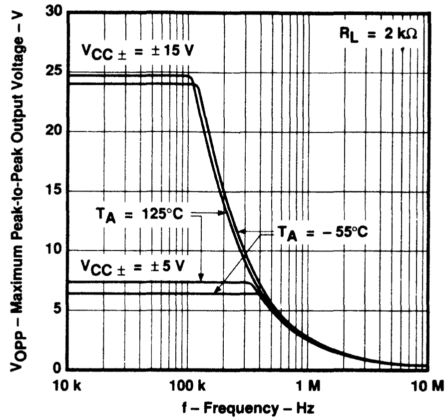


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

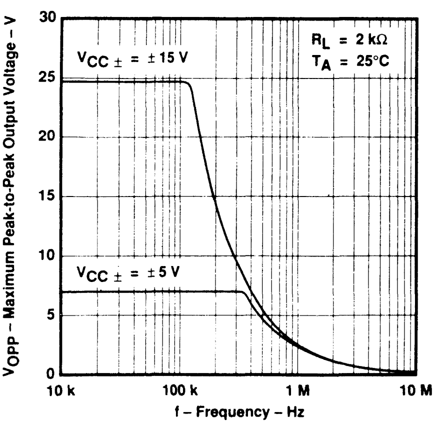


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

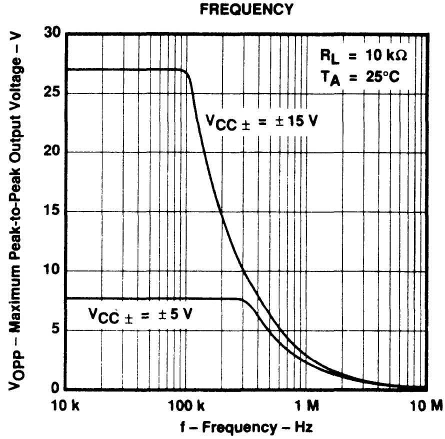


FIGURE 17

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

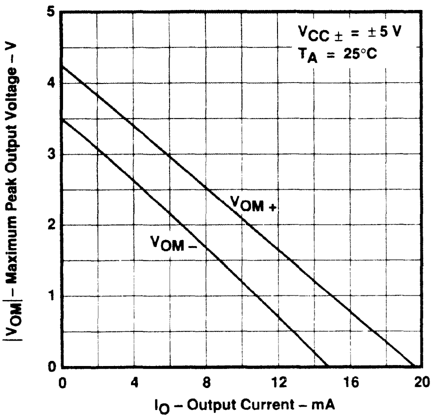


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

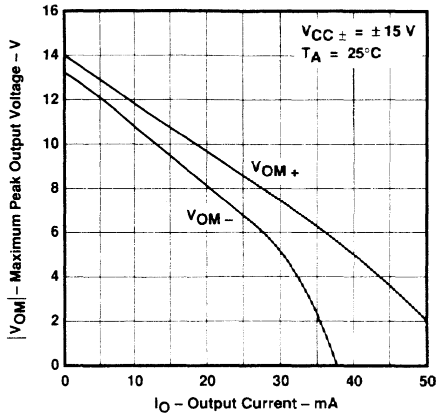


FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

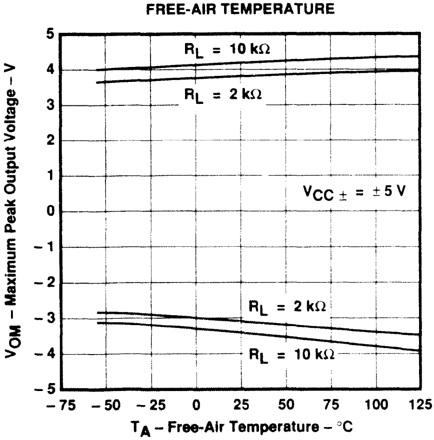


FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

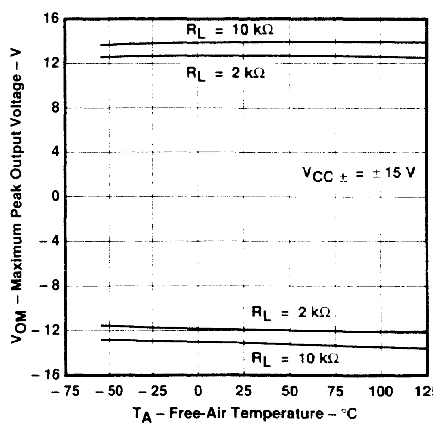


FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

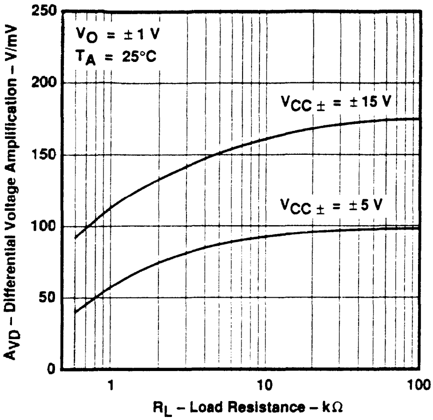


FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

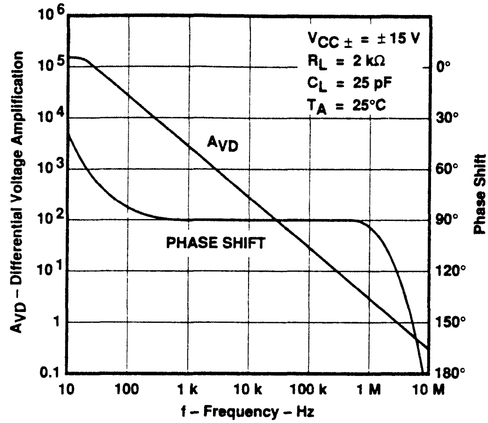


FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

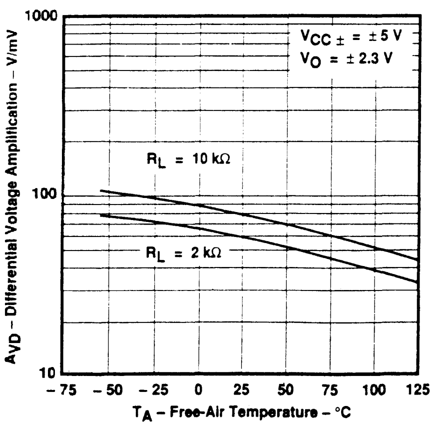


FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

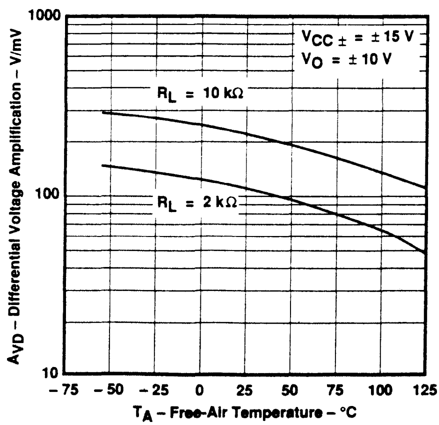


FIGURE 25

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

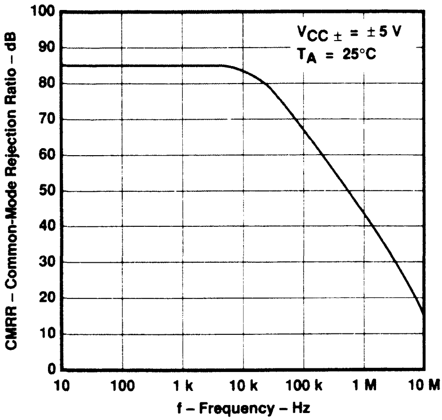


FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

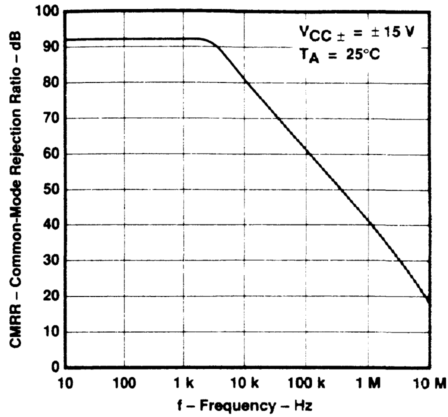


FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

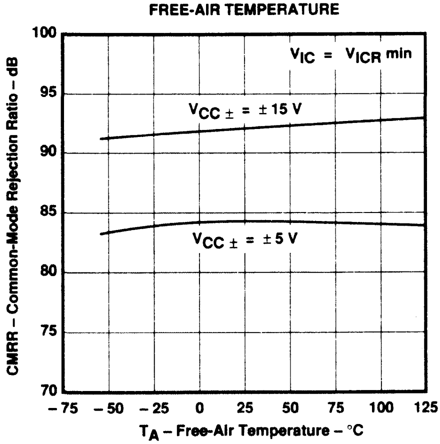


FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

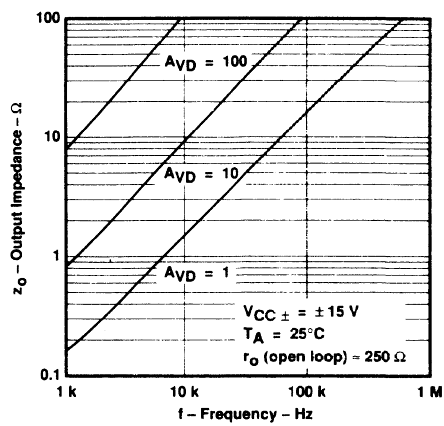


FIGURE 29

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

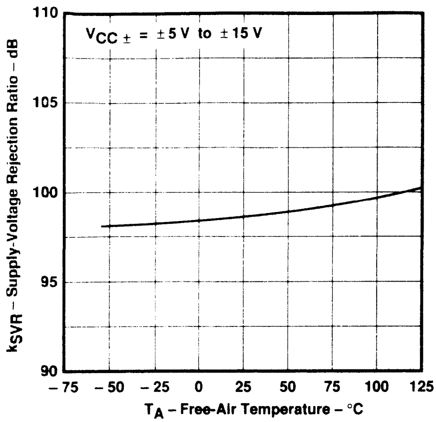


FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

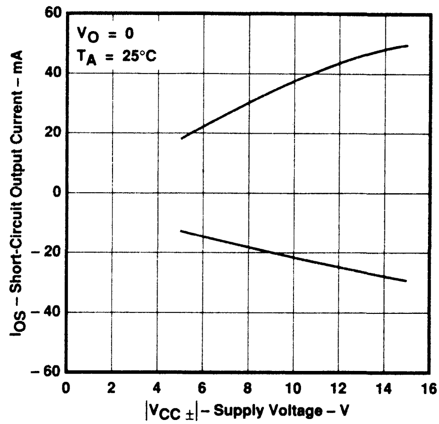


FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

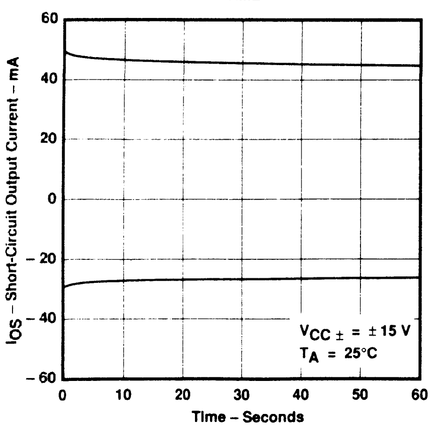


FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

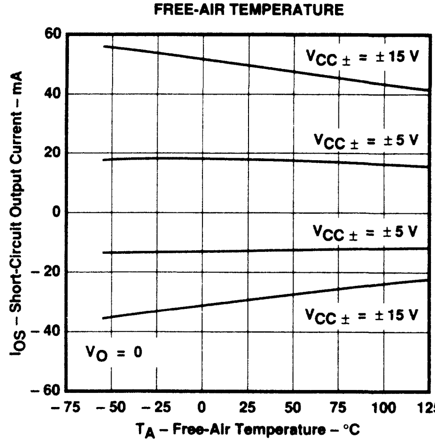


FIGURE 33

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

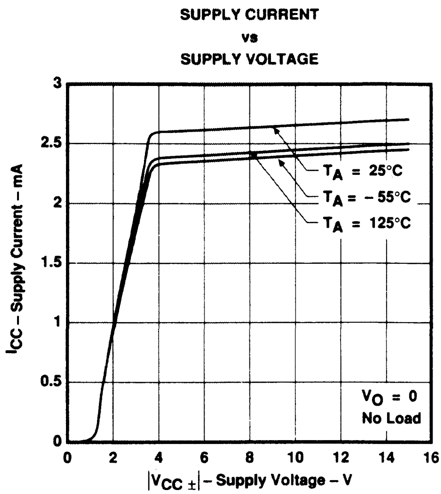


FIGURE 34

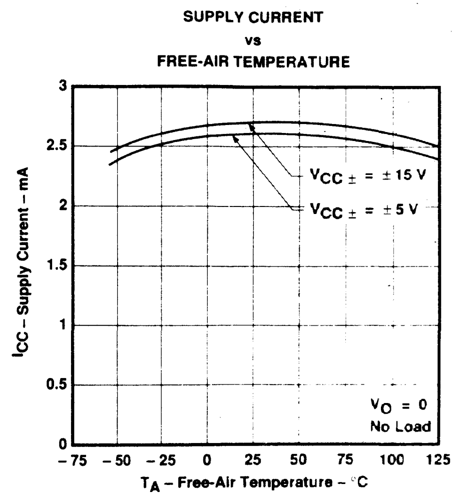


FIGURE 35

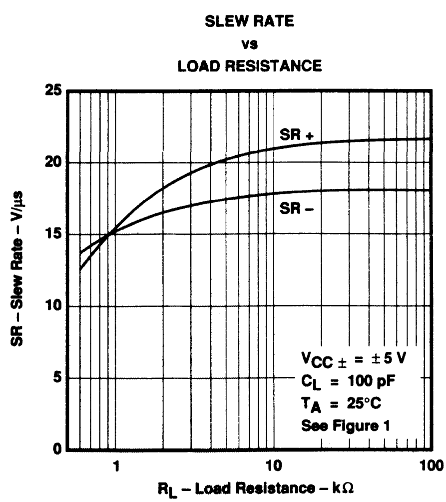


FIGURE 36

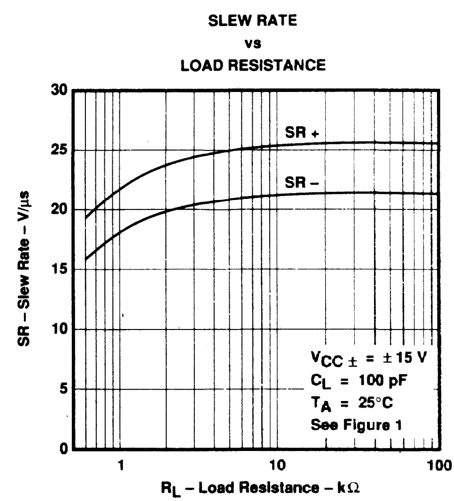


FIGURE 37

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

SLEW RATE
vs
FREE-AIR TEMPERATURE

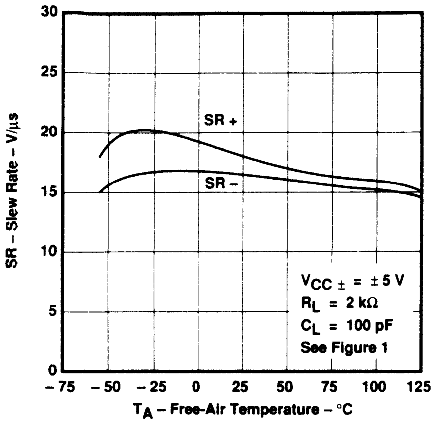


FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

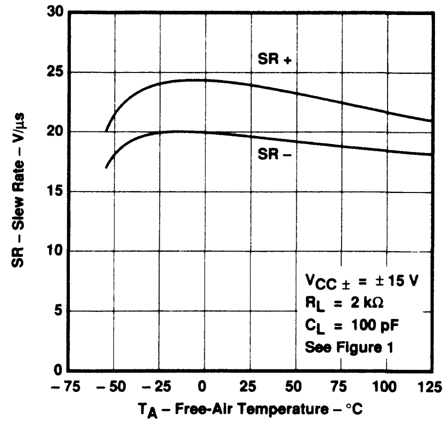


FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

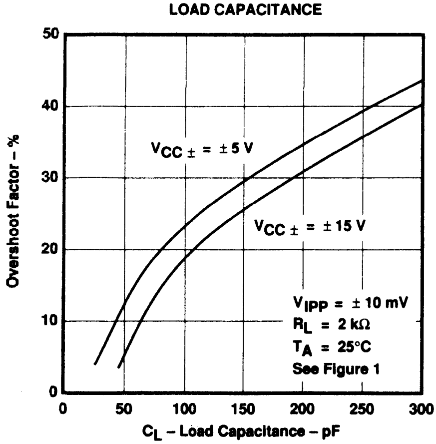


FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

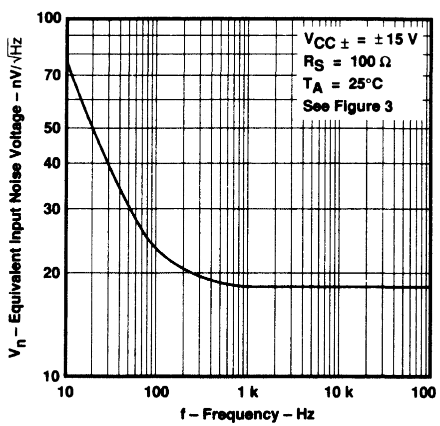


FIGURE 41

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs FREQUENCY

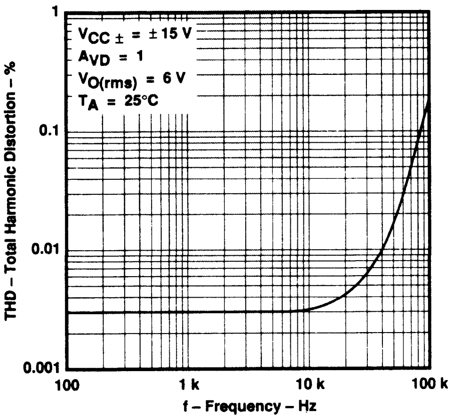


FIGURE 42

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

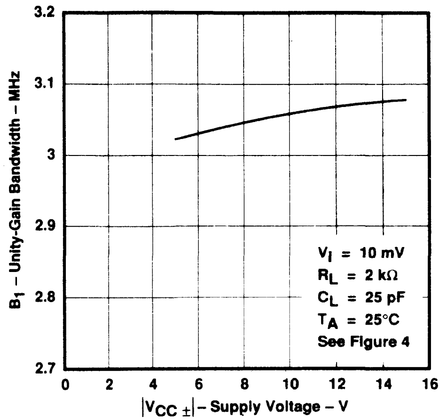


FIGURE 43

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

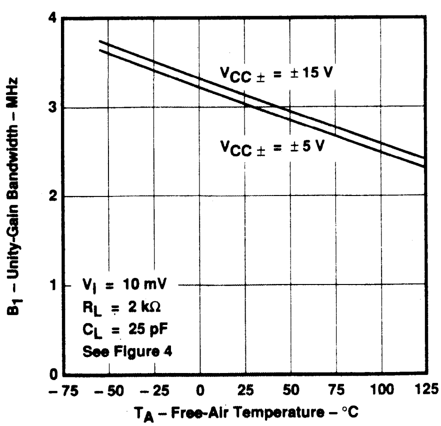


FIGURE 44

PHASE MARGIN vs SUPPLY VOLTAGE

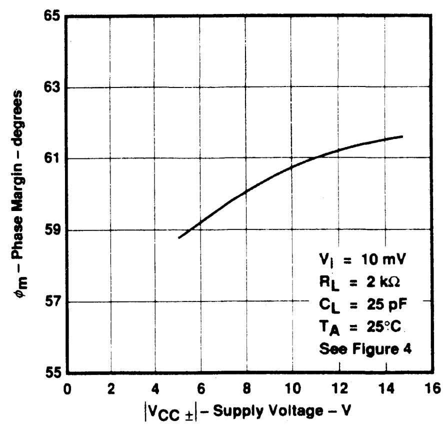


FIGURE 45

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

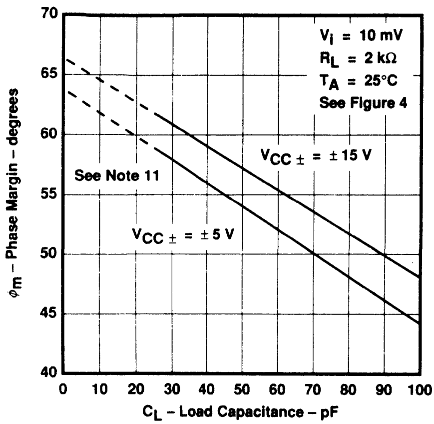


FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

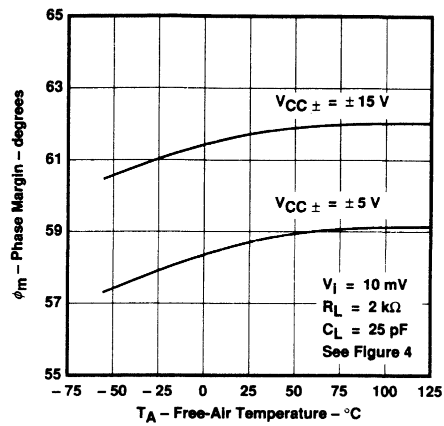


FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

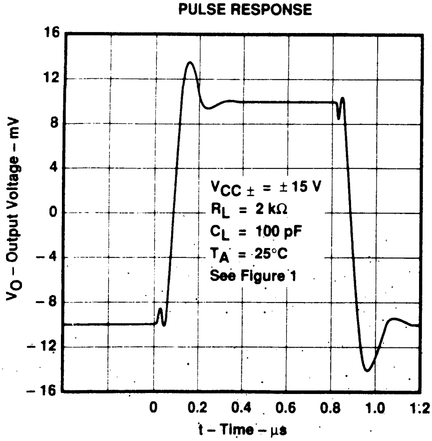


FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

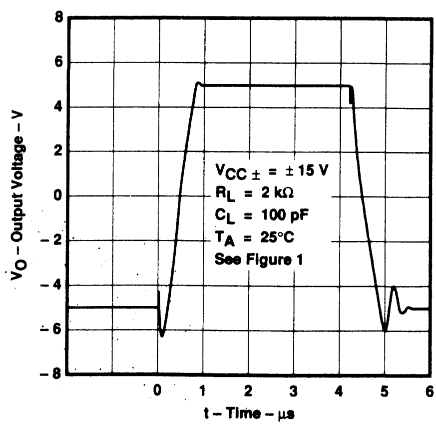


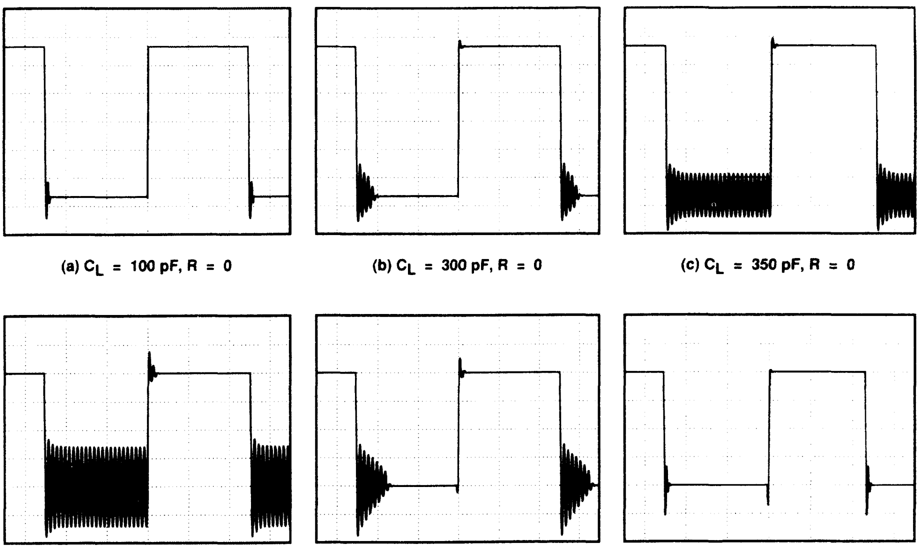
FIGURE 49

NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL APPLICATION DATA

output characteristics

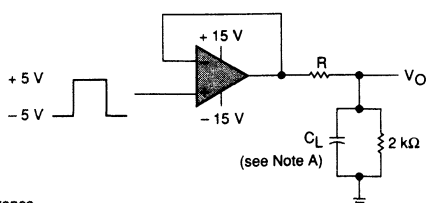
All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL051 and TL051A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

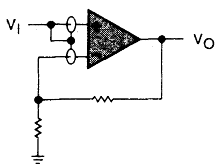
FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

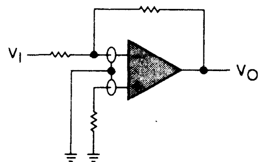
input characteristics

The TL051 and TL051A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

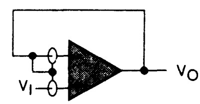
Because of the extremely high input impedance and resulting low bias current requirements, the TL051 and TL051A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity-Gain Amplifier

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL051 and TL051A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

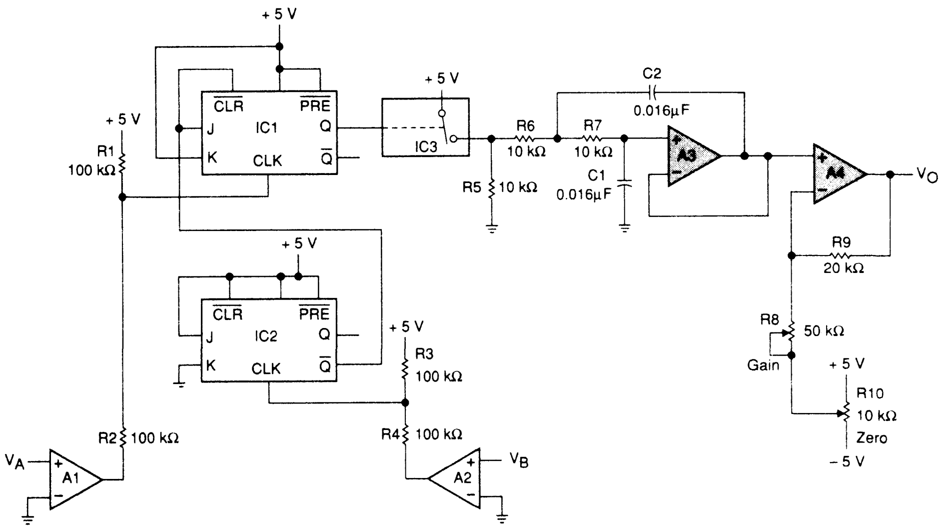
phase meter

This phase meter produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparator converts these two input sine waves into ± 5 V square waves. Then R2 and R4 provide level shifting prior to the 74HC109 dual J-K flip flops.

Flip-flop IC2 is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop IC1 also produces a square wave at half the input frequency. The pulse width of IC1 varies from zero to half the period where zero corresponds to zero phase delay between V_A and V_B and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from IC1 causes the TLC4066 switch to charge the TL051 integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of IC1 approximates a square wave and A3 has an output of almost 2.5 V. A4 acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0 to 2.5 V integrator output to a 0 to 3.6 V output range.

R8 and R10 provide output gain and zero level calibration. This circuit operates over a 100 Hz to 10 kHz frequency range.



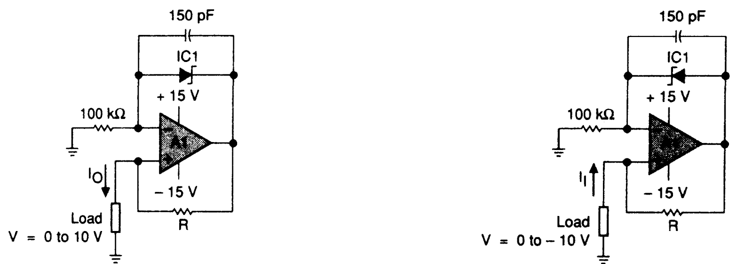
NOTES: IC1 and IC2 = 74HC109.
IC3 = TLC4066.
A1, A2 = TLC3702: $V_{CC\pm}$ = ±5 V.
A3,A4 = TL051; $V_{CC\pm}$ = ±5 V.

TYPICAL APPLICATION DATA

precision constant current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low current shunt regulator maintains 2.5 V between the inverting input and the output of the TL051. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



(a) Source current load (b) Sink current load

NOTES: IC1 = LM385, LT1004, or LT1009 voltage reference.
A1 = TL051.
$I = \frac{2.5\ V}{R}$, R = Low temperature coefficient metal film resistor.

JUNE 1988

- **Maximum Offset Voltage . . . 800 μV**
- **High Slew Rate . . . 17.8 V/μs Typ**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

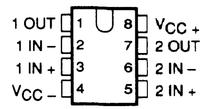
description

The TL052 and TL052A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

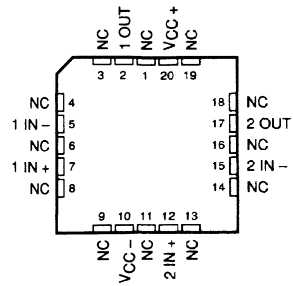
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL052 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL052 has been designed to be functionally compatible as well as pin compatible with the TL072 and TL082.

Two offset voltage grades are available: TL052 (1.5 mV max) and TL052A (800 μV max).

D, JG, or P PACKAGE (TOP VIEW)

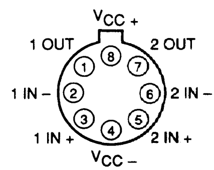


FK PACKAGE (TOP VIEW)



NC – No internal connection

L PACKAGE (TOP VIEW)



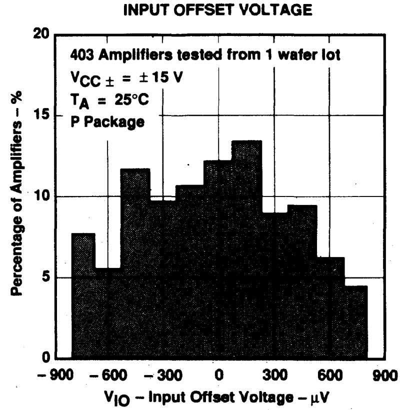
Pin 4 is in electrical contact with the case

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE				
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)	Metal Can (L)
0°C to 70°C	800 μV	TL052ACD	TL052ACP	TL052ACJG	—	TL052ACL
	1500 μV	TL052CD	TL052CP	TL052CJG	—	TL052CL
− 40°C to 85°C	800 μV	TL052AID	TL052AIP	TL052AIJG	—	TL052AIL
	1500 μV	TL052ID	TL052IP	TL052IJG	—	TL052IL
− 55°C to 125°C	800 μV	—	—	TL052AMJG	TL052AMFK	TL052AML
	1500 μV	—	—	TL052MJG	TL052MFK	TL052ML

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TL052CDR).

DISTRIBUTION OF TL052A INPUT OFFSET VOLTAGE



ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

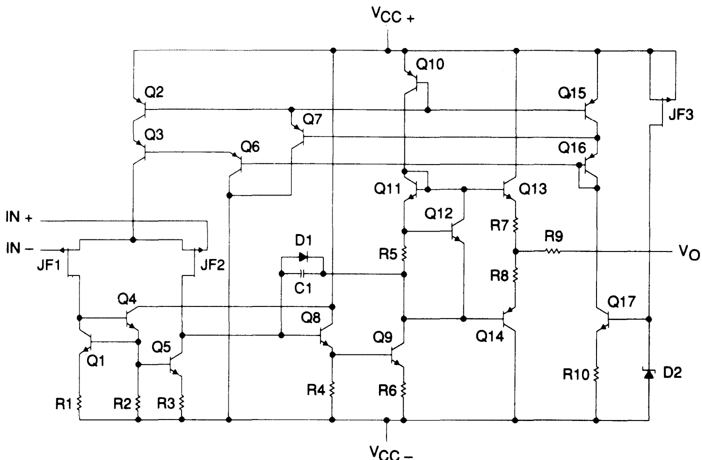
TEXAS INSTRUMENTS

description (continued)

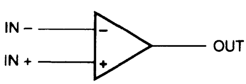
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 2) . . . . 18 V
Supply voltage, V_{CC-} (see Note 2) . . . . – 18 V
Differential input voltage (see Note 3) . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 2 and 4) . . . . ± 15 V
Input current, I_I (each input) . . . . ± 1 mA
Output current, I_O (each output) . . . . ± 80 mA
Total current into V_{CC+} terminal . . . . 160 mA
Total current out of V_{CC-} terminal . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 5) . . . . Unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . – 55°C to 125°C
I-suffix . . . . – 40°C to 85°C
C-suffix . . . . 0°C to 70°C
Storage temperature range . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
5. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	
L	650 mW	5.1 mW/°C	421 mW	344 mW	140 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	V
Input voltage, V_I	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS			$V_{CC\pm} = \pm 5$ V			$V_{CC\pm} = \pm 15$ V			UNIT
				T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052C	25°C		0.73	3.5		0.65	1.5	mV
				Full range			4.5			2.5	
			TL052AC	25°C		0.51	2.8		0.4	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL052C	25°C to 70°C		8			8		µV/°C
			TL052AC	25°C to 70°C		8			6	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				0°C	3	4.1		13	13.9		
				70°C	3	4.3		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				0°C	2.5	3.8		11.5	12.7		
				70°C	2.5	3.9		11.5	12.8		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				0°C	−2.5	−3.3		−12	−13.1		
				70°C	−2.5	−3.6		−12	−13.4		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				0°C	−2.3	−3.1		−11	−11.9		
				70°C	−2.3	−3.3		−11	−12.1		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 7		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				0°C		4.7	6.4		4.8	6.4	
				70°C		4.4	6.4		4.6	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTES: 6. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		17.8		13	20.7		V/µs
				0°C		18.5		11	20.9		
				70°C		16.5		11	20.8		
SR −	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				0°C		15.7		11	18.5		
				70°C		14.7		11	16.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 10		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				0°C		3.2			3.2		
				70°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				0°C		59°			63°		
				70°C		60°			63°		

NOTES: 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.

9. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

10. For $V_{CC\pm} = \pm5$ V, $V_{O(rms)}$ = 1 V; for $V_{CC\pm} = \pm15$ V, $V_{O(rms)}$ = 6 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052I	25°C		0.73	3.5		0.65	1.5	mV
				Full range			5.3			3.3	
			TL052AI	25°C		0.51	2.8		0.4	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 6)		TL052I	25°C to 85°C		7			6		µV/°C
			TL052AI	25°C to 85°C		6			6	25	
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				−40°C	3	4		13	13.8		
				85°C	3	4.3		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				−40°C	2.5	3.7		11.5	12.6		
				85°C	2.5	3.9		11.5	12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				−40°C	−2.5	−3.2		−12	−12.9		
				85°C	−2.5	−3.8		−12	−13.5		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				−40°C	−2.3	−2.9		−11	−11.8		
				85°C	−2.3	−3.4		−11	−12		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 7		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				−40°C		4.5	6.4		4.7	6.4	
				85°C		4.4	6.4		4.6	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTES: 6. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

7. At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1, See Note 8		25°C		17.8		13	20.7		V/μs
				– 40°C		18.8		11	20.6		
				85°C		16		11	20.7		
SR –	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				– 40°C		16		11	17.8		
				85°C		14.5		11	17.2		
t_r	Rise time	$V_{IPP} = \pm 10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				– 40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	$R_S = 100$ Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz, See Note 10		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		3			3		MHz
				– 40°C		3.5			3.6		
				85°C		2.5			2.6		
ϕ_m	Phase margin at unity gain	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		60°			63°		
				– 40°C		58°			61°		
				85°C		60°			63°		

NOTES: 8. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.
10. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL052M	25°C		0.73	3.5		0.65	1.5	mV
				Full range			6.5			4.5	
			TL052AM	25°C		0.51	2.8		0.4	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL052M	25°C to 125°C		10			9		µV/°C
			TL052AM	25°C to 125°C		9			8		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				−55°C	3	4		13	13.8		
				125°C	3	4.4		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				−55°C	2.5	3.6		11.5	12.5		
				125°C	2.5	3.9		11.5	12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				−55°C	−2.5	−3.1		−12	−12.9		
				125°C	−2.5	−3.9		−12	−13.6		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				−55°C	−2.3	−2.8		−11	−11.7		
				125°C	−2.3	−3.5		−11	−12		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (two amplifiers)	No load, $V_O = 0$		25°C		4.6	5.6		4.8	5.6	mA
				−55°C		4.4	6.4		4.5	6.4	
				125°C		4.2	6.4		4.4	6.4	
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

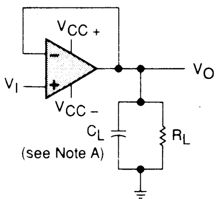
NOTE 6: At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1, See Note 8		25°C		17.8		13	20.7		V/µs
				– 55°C		18.8			20.3		
				125°C		14.5			20.2		
SR –	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				– 55°C		15.7			17.6		
				125°C		13.8			16.5		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				– 55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				– 55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 10		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				– 55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				– 55°C		57°			61°		
				125°C		60°			63°		

NOTES: 8. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.
10. For $V_{CC\pm} = \pm5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(rms)} = 6$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

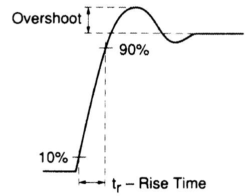


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

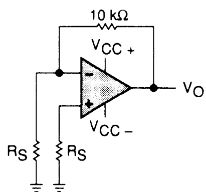
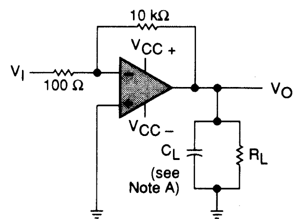


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

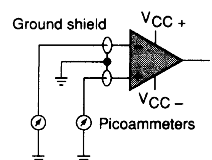


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

At the picoamp bias current level typical of the TL052 and TL052A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test is performed which measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet your application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE

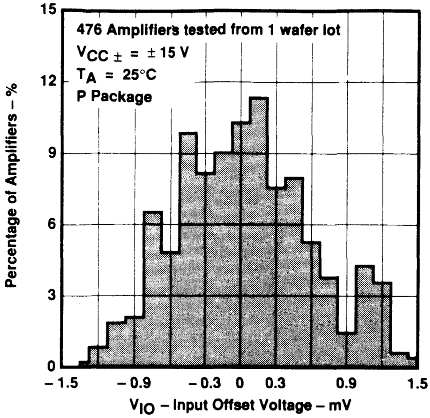


FIGURE 6

DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

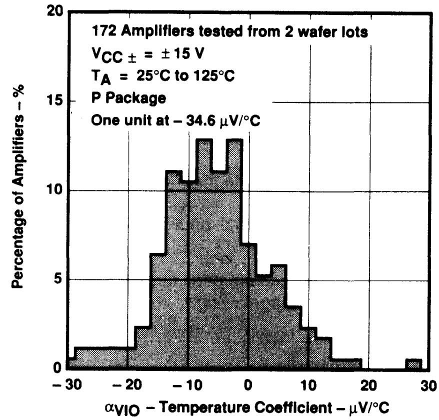


FIGURE 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

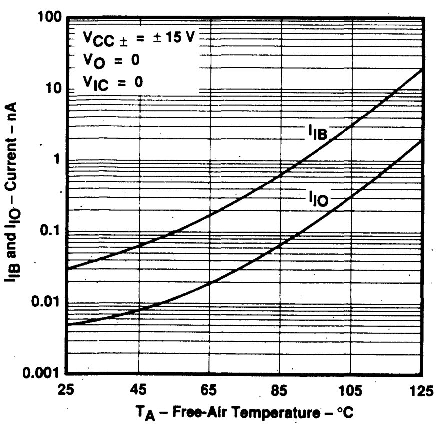


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

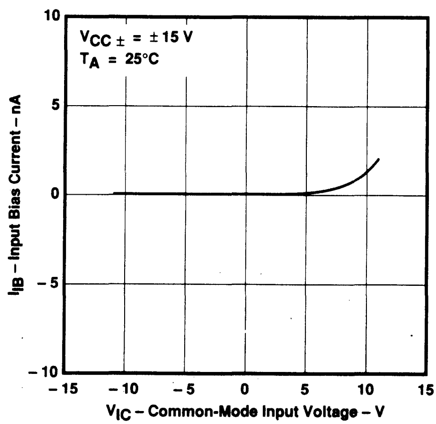


FIGURE 9

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

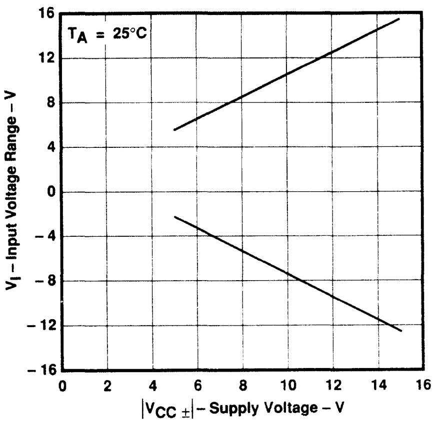


FIGURE 10

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

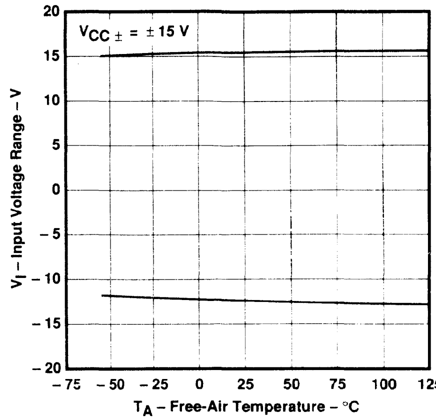


FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

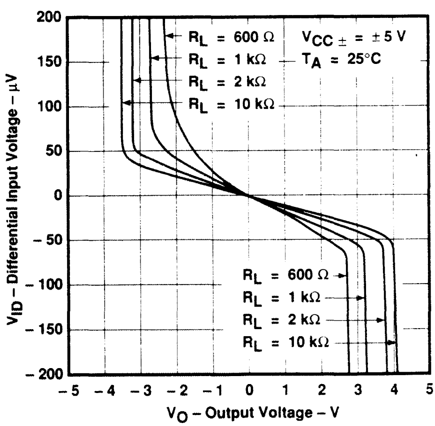


FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

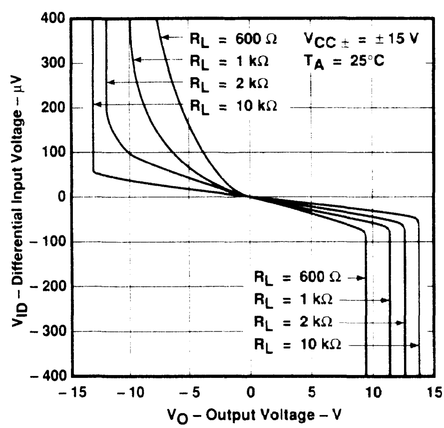


FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

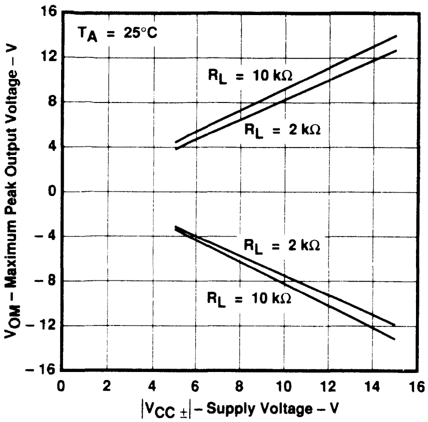


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

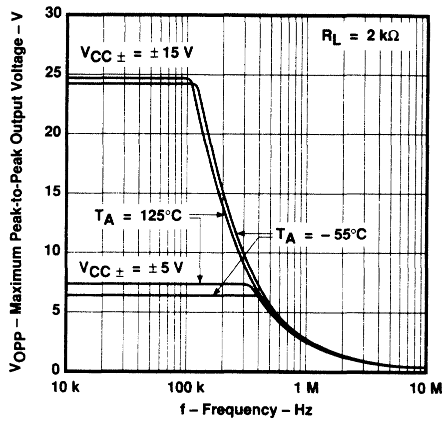


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

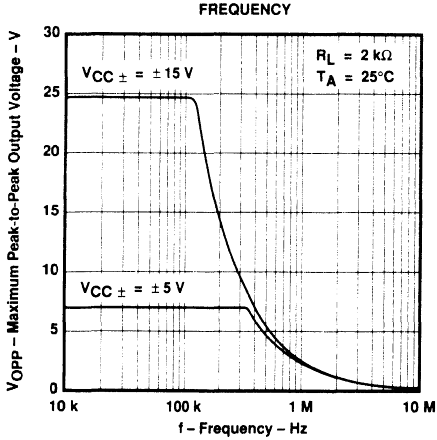


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

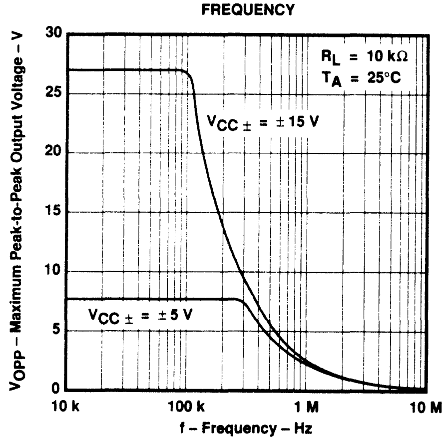


FIGURE 17

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

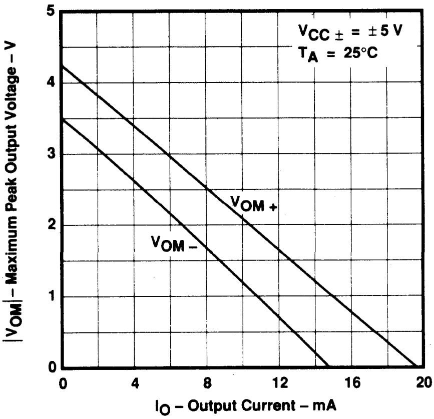


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

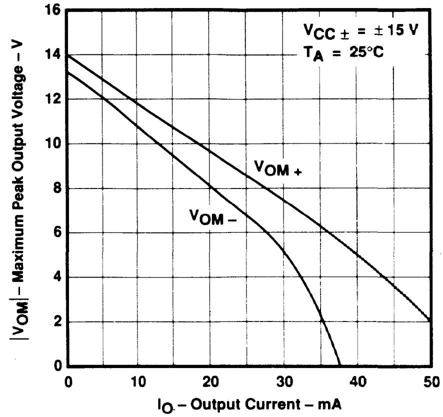


FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

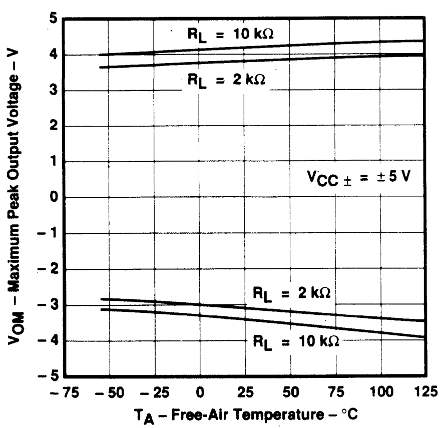


FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

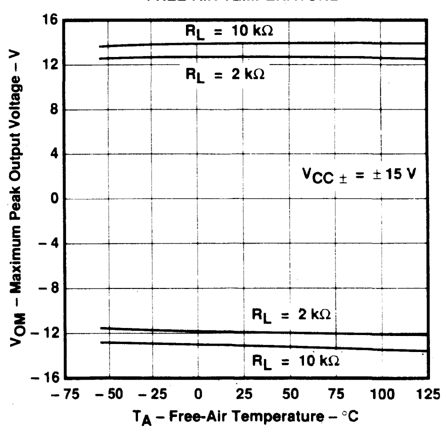


FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

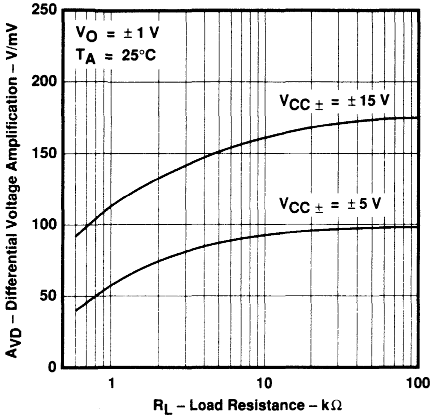


FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

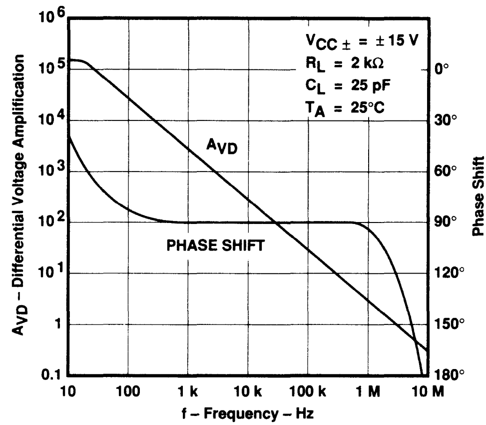


FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

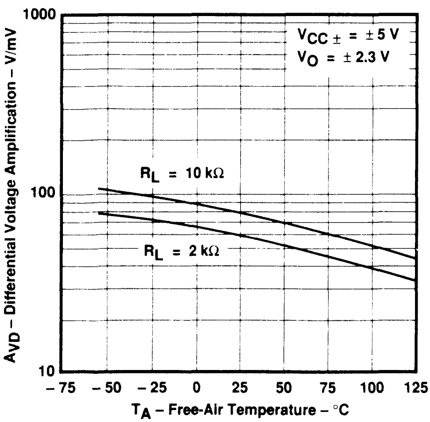


FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

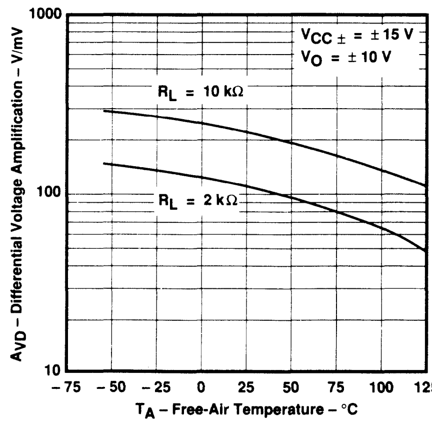


FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

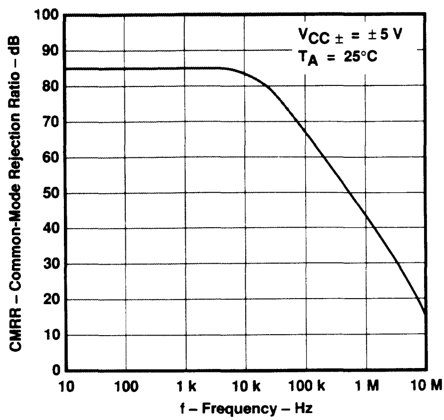


FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

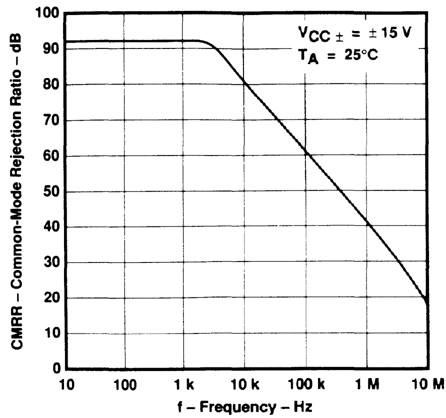


FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

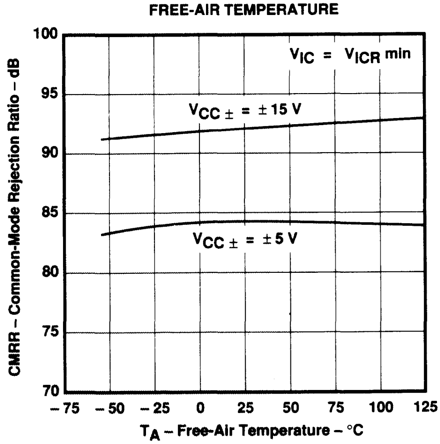


FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

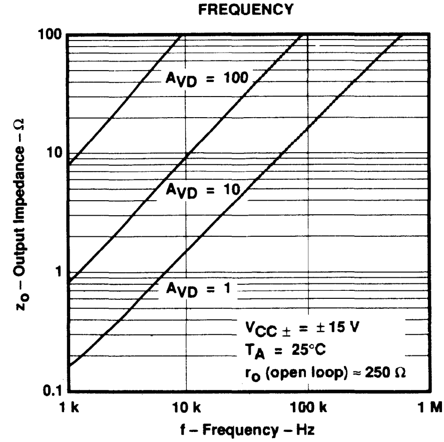


FIGURE 29

3

Operational Amplifiers

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

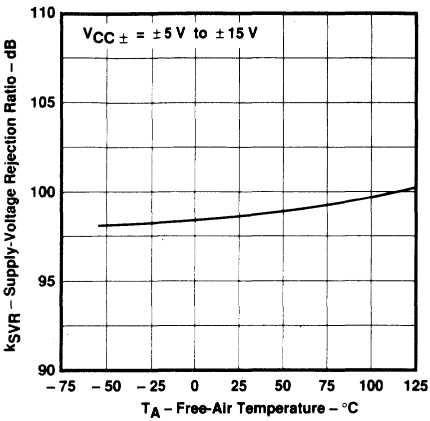


FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

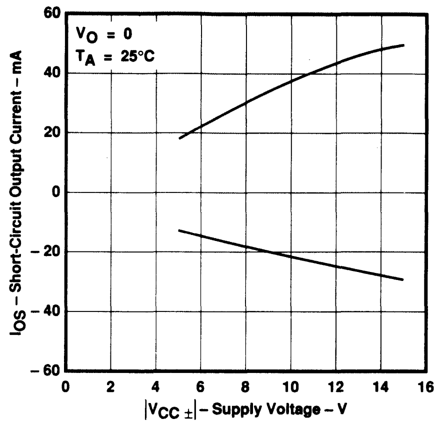


FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

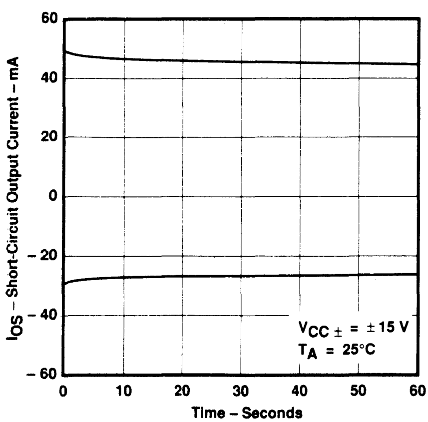


FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

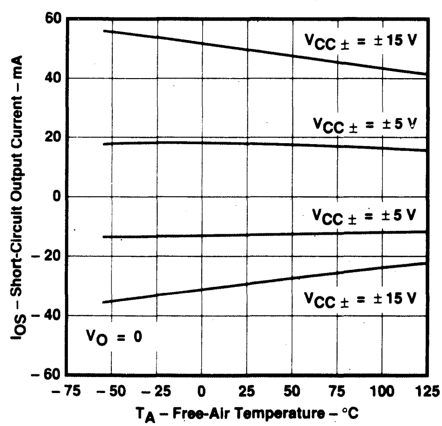


FIGURE 33

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

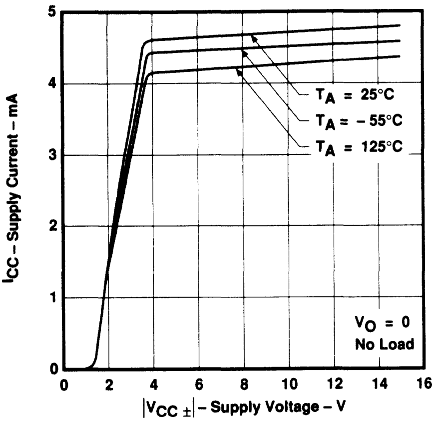


FIGURE 34

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

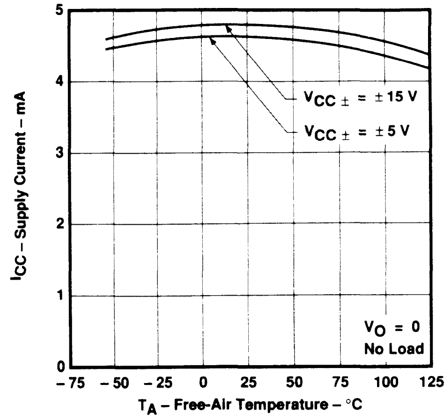


FIGURE 35

SLEW RATE vs LOAD RESISTANCE

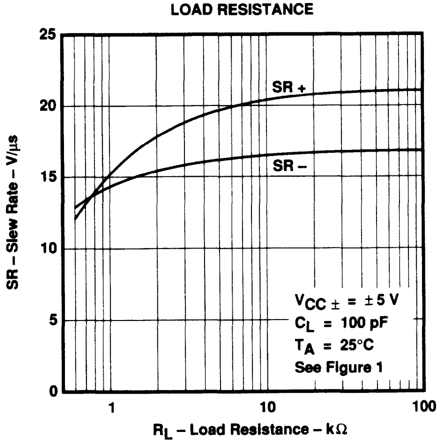


FIGURE 36

SLEW RATE vs LOAD RESISTANCE

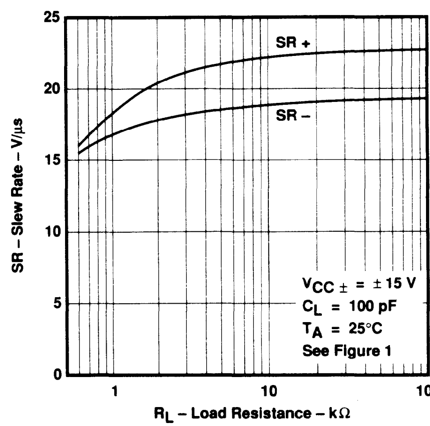


FIGURE 37

TYPICAL CHARACTERISTICS

SLEW RATE
vs
FREE-AIR TEMPERATURE

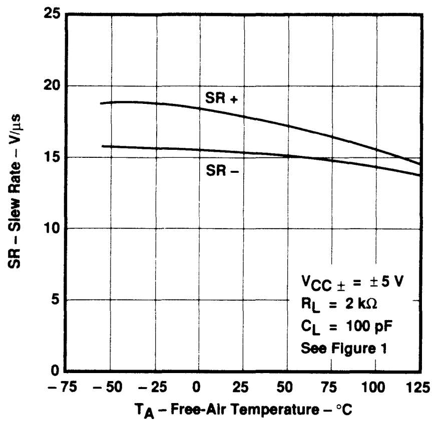


FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

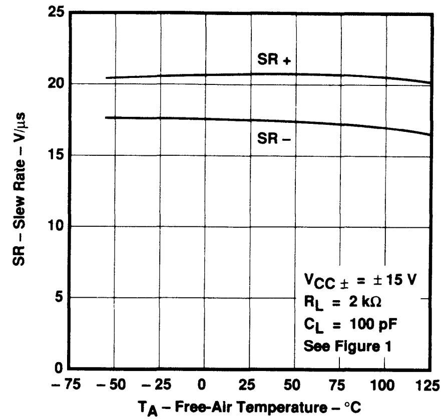


FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

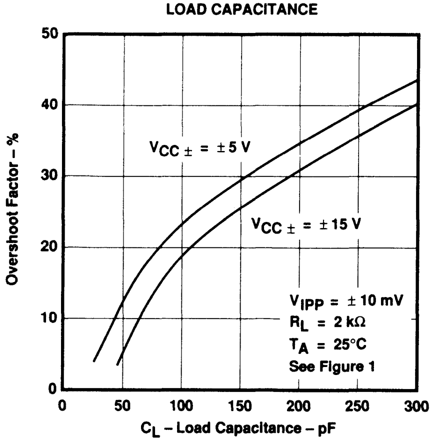


FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

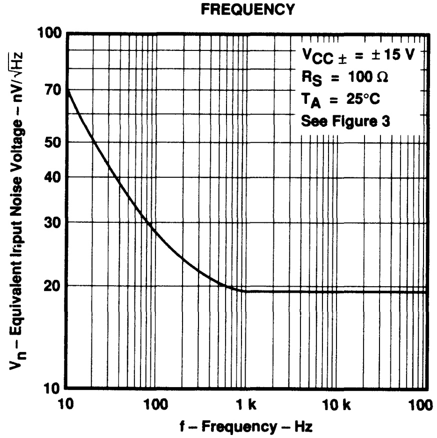


FIGURE 41

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

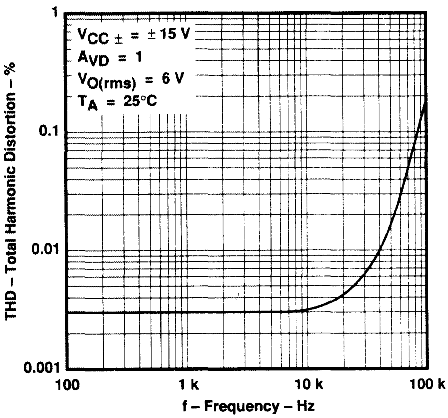


FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

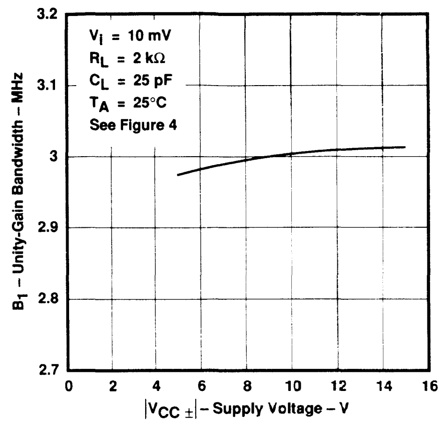


FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

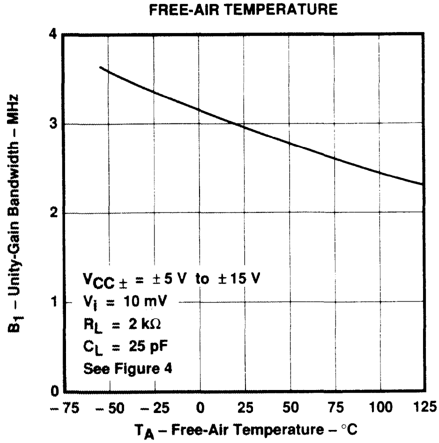


FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

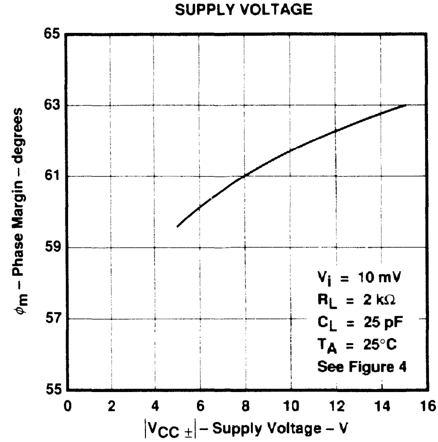


FIGURE 45

3
Operational Amplifiers

TYPICAL CHARACTERISTICS

**PHASE MARGIN
vs
LOAD CAPACITANCE**

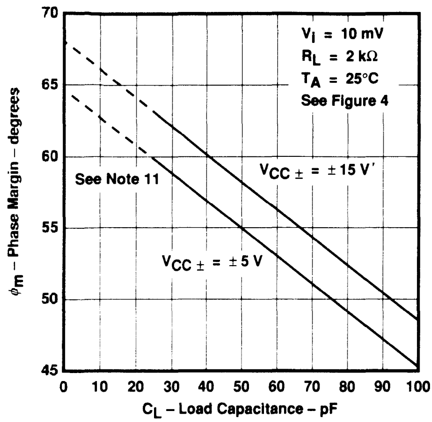


FIGURE 46

**PHASE MARGIN
vs
FREE-AIR TEMPERATURE**

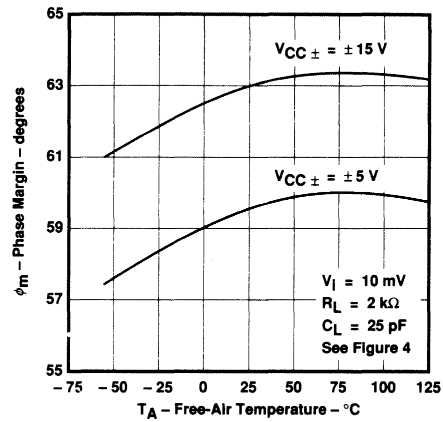


FIGURE 47

**VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE**

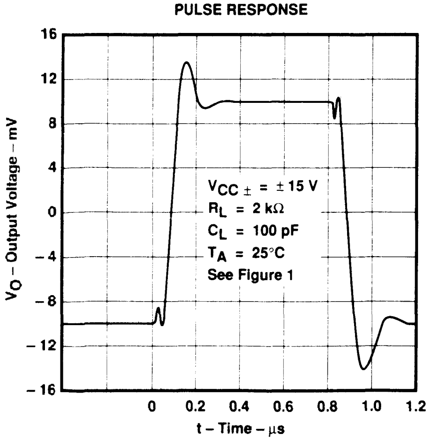


FIGURE 48

**VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE**

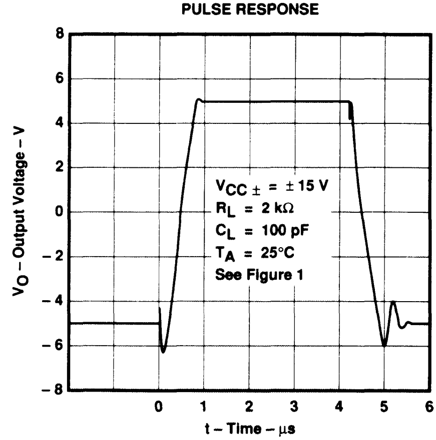


FIGURE 49

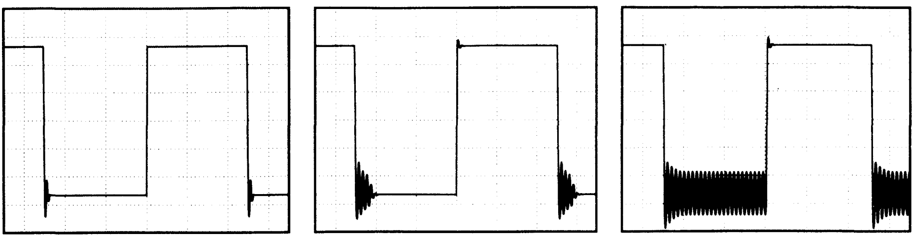
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

3 Operational Amplifiers

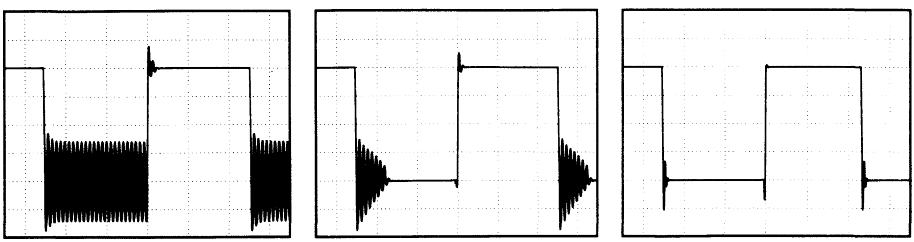
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL052 and TL052A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).

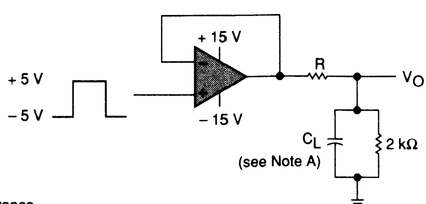


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

input characteristics

The TL052 and TL052A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL052 and TL052A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

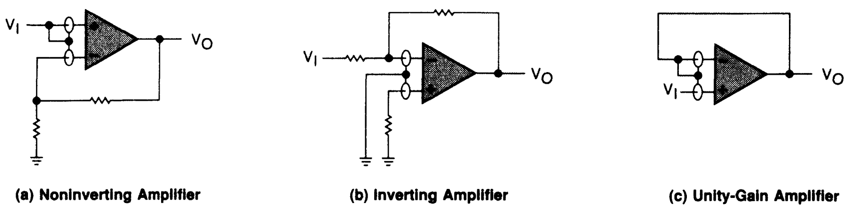


FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL052 and TL052A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

instrumentation amplifier with adjustable gain/null

This instrumentation amplifier benefits greatly from the high input impedance and stable input offset voltage of the TL052A. Amplifiers A1, A2, and A3 form the actual instrumentation amplifier while A4 provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100 while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

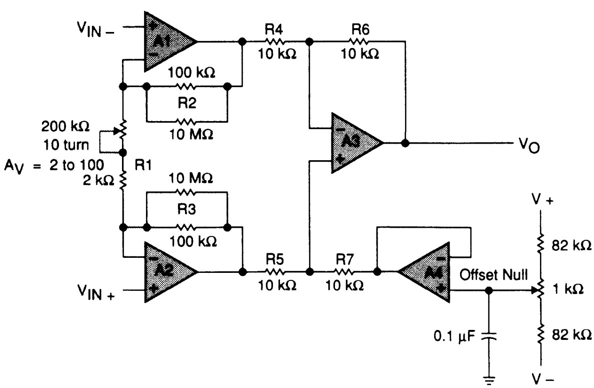
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if A4 is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL052A will minimize the DC error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 will control the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This DC error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature will also create an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs will minimize the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE: A1 thru A4 = TL052A; $V_{CC\pm}$ = ± 15 V.

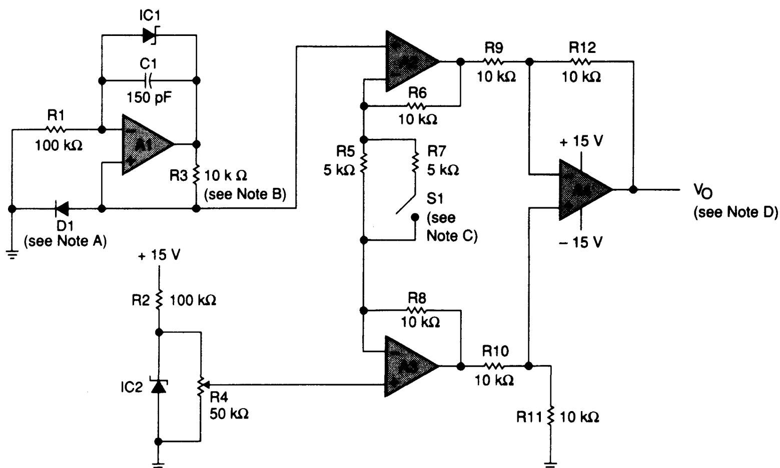
TYPICAL APPLICATION DATA

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built. Amplifier A1 and IC1 establish a constant current through the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL052 must use split supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature sensitive voltage from the diode is compared to a temperature stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer will remain constant.

Amplifiers A2, A3, and A4 form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A1 thru A4 = TL052.
IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.
A. Temperature sensing diode ≈ (– 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. $V_O \propto$ Temp; 10 mV/°C or 10 mV/°F.

TYPICAL APPLICATION DATA

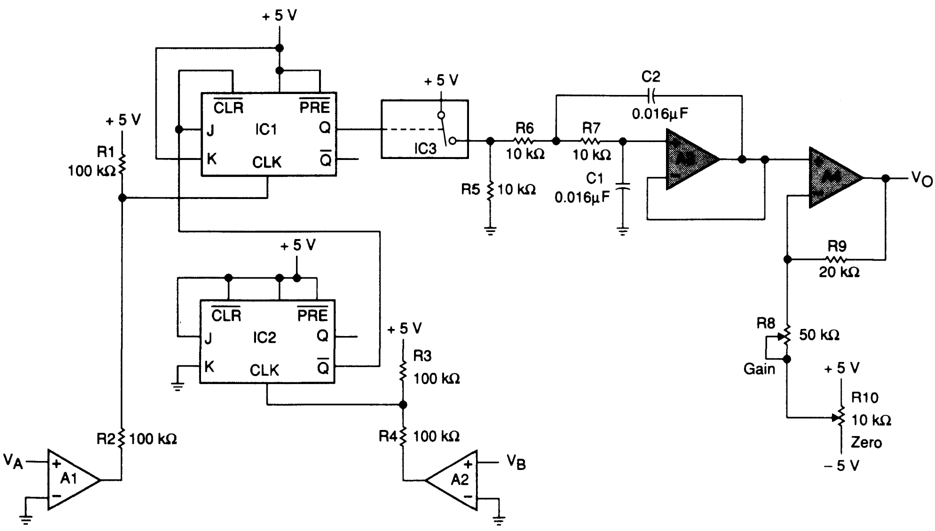
phase meter

This phase meter produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparator converts these two input sine waves into ± 5 V square waves. Then R2 and R4 provide level shifting prior to the 74HC109 dual J-K flip flops.

Flip-flop IC2 is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop IC1 also produces a square wave at half the input frequency. The pulse width of IC1 varies from zero to half the period where zero corresponds to zero phase delay between V_A andV_B and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from IC1 causes the TLC4066 switch to charge the TL052 integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of IC1 approximates a square wave and A3 has an output of almost 2.5 V. A4 acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0 to 2.5 V integrator output to a 0 to 3.6 V output range.

R8 and R10 provide output gain and zero level calibration. This circuit operates over a 100 Hz to 10 kHz frequency range.



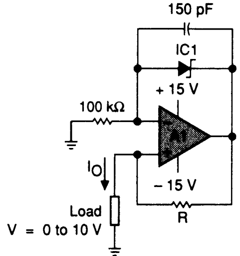
NOTES: IC1 and IC2 = 74HC109.
IC3 = TLC4066.
A1, A2 = TLC3702; $V_{CC\pm}$ = ±5 V.
A3,A4 = TL052; $V_{CC\pm}$ = ±5 V.

TYPICAL APPLICATION DATA

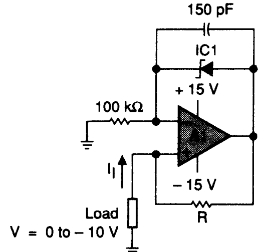
precision constant current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low current shunt regulator maintains 2.5 V between the inverting input and the output of the TL052. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



(a) Source current load



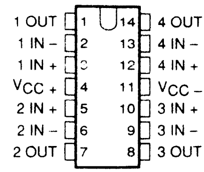
(b) Sink current load

NOTES: IC1 = LM385, LT1004, or LT1009 voltage reference.
A1 = TL052.
$I = \frac{2.5\ V}{R}$, R = Low temperature coefficient metal film resistor.

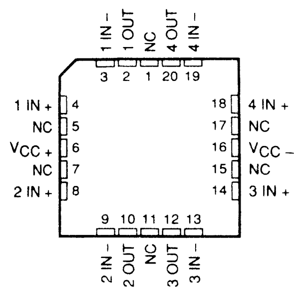
JUNE 1988

- **Maximum Offset Voltage . . . 1.5 mV**
- **High Slew Rate . . . 15.9 V/μs Typ**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 21 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**
- **Monolithic Construction**

D, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

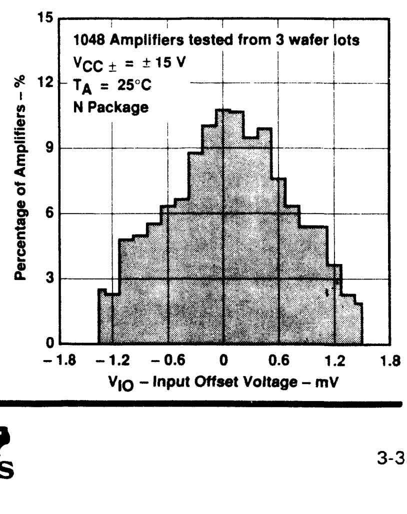
description

The TL054 and TL054A quad operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL054 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL054 has been designed to be functionally compatible as well as pin compatible with the TL074 and TL084.

Two offset voltage grades are available:
TL054 (4 mV max) and TL054A (1.5 mV max).

DISTRIBUTION OF TL054A
INPUT OFFSET VOLTAGE



AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	1.5 mV	TL054ACD	TL054ACN	TL054ACJ	—
	4 mV	TL054CD	TL054CN	TL054CJ	—
– 40°C to 85°C	1.5 mV	TL054AID	TL054AIN	TL054AIJ	—
	4 mV	TL054ID	TL054IN	TL054IJ	—
– 55°C to 125°C	1.5 mV	—	—	TL054AMJ	TL054AMFK
	4 mV	—	—	TL054MJ	TL054MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TL054CDR).

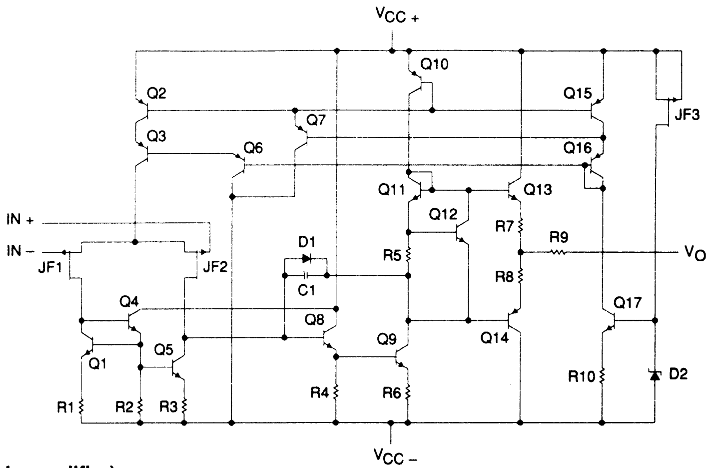
TEXAS INSTRUMENTS

description (continued)

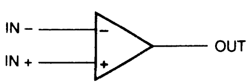
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The M- suffix devices are characterized for operation over the full military temperature range of − 55°C to 125°C. The I- suffix devices are characterized for operation from − 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 2)	18 V
Supply voltage, V_{CC-} (see Note 2)	− 18 V
Differential input voltage (see Note 3)	± 30 V
Input voltage range, V_I (any input, see Notes 2 and 4)	± 15 V
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output)	± 80 mA
Total current into V_{CC+} terminal	160 mA
Total current out of V_{CC-} terminal	160 mA
Duration of short-circuit current at (or below) 25°C (see Note 5)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix	− 55°C to 125°C
I-suffix	− 40°C to 85°C
C-suffix	0°C to 70°C
Storage temperature range	− 65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
5. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	− 1		4	− 1		4	− 1		4	V
	$V_{CC\pm} = \pm 15$ V	− 11		11	− 11		11	− 11		11	V
Input voltage, V_I	$V_{CC\pm} = \pm 5$ V	− 1		4	− 1		4	− 1		4	V
	$V_{CC\pm} = \pm 15$ V	− 11		11	− 11		11	− 11		11	V
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054C	25°C		0.64	5.5		0.56	4	mV
				Full range			7.7			6.2	
			TL054AC	25°C		0.57	3.5		0.5	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage		TL054C	25°C to 70°C		25			23		µV/°C
			TL054AC	25°C to 70°C		24			23		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				0°C	3	4.1		13	13.9		
				70°C	3	4.3		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				0°C	2.5	3.8		11.5	12.7		
				70°C	2 5	3.9		11.5	12.8		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				0°C	−2.5	−3.3		−12	−13.1		
				70°C	−2.5	−3.6		−12	−13.4		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				0°C	−2.3	−3.1		−11	−11.9		
				70°C	−2.3	−3.3		−11	−12.1		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				0°C	30	88		60	173		
				70°C	20	57		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				0°C	65	84		75	92		
				70°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				0°C	75	99		75	99		
				70°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				0°C		8.2	12.8		8.5	12.8	
				70°C		7.9	11.2		8.2	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTE 6: At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1, See Note 7		25°C		15.4		10	17.8		V/μs
				0°C		15.7		8	17.9		
				70°C		14.4		8	17.5		
SR –	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				0°C		14.3		8	16.1		
				70°C		13.3		8	15.5		
t_r	Rise time	$V_{IPP} = \pm 10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 8)	$R_S = 100$ Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz, See Note 9		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		2.7			2.7		MHz
				0°C		3			3		
				70°C		2.4			2.4		
ϕ_m	Phase margin at unity gain	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		61°			64°		
				0°C		60°			64°		
				70°C		61°			63°		

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

9. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)} = 6$ V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054I	25°C		0.64	5.5		0.56	4	mV
				Full range			8.8			7.3	
			TL054AI	25°C		0.57	3.5		0.5	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL054I	25°C to 85°C		25			24		µV/°C
			TL054AI	25°C to 85°C		25			23		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				−40°C	3	4		13	13.8		
				85°C	3	4.3		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				−40°C	2.5	3.7		11.5	12.6		
				85°C	2.5	3.9		11.5	12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				−40°C	−2.5	−3.2		−12	−12.9		
				85°C	−2.5	−3.8		−12	−13.5		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				−40°C	−2.3	−2.9		−11	−11.8		
				85°C	−2.3	−3.4		−11	−12		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				−40°C	30	101		60	212		
				85°C	20	50		30	70		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				−40°C	65	83		75	92		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm5$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				−40°C		7.9	12.8		8.2	12.8	
				85°C		7.6	11.2		7.9	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

NOTE 6: At $V_{CC\pm} = \pm5$ V, $V_O = \pm2.3$ V; at $V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
SR +	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		15.4		10	17.8		V/μs
				−40°C		16.4		8	18		
				85°C		14		8	17.3		
SR −	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				−40°C		14.7		8	16.1		
				85°C		13		8	15.3		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				−40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				−40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				−40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 8)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 9		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				−40°C		3.3			3.3		
				85°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				−40°C		59°			62°		
				85°C		61°			64°		

NOTES: 7. For $V_{CC\pm} = \pm 5$ V, $V_{IPP} = \pm 1$ V; for $V_{CC\pm} = \pm 15$ V, $V_{IPP} = \pm 5$ V.

8. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

9. For $V_{CC\pm} = \pm 5$ V, $V_{O(rms)}$ = 1 V; for $V_{CC\pm} = \pm 15$ V, $V_{O(rms)}$ = 6 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm 5$ V MIN	$V_{CC\pm} = \pm 5$ V TYP	$V_{CC\pm} = \pm 5$ V MAX	$V_{CC\pm} = \pm 15$ V MIN	$V_{CC\pm} = \pm 15$ V TYP	$V_{CC\pm} = \pm 15$ V MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	TL054M	25°C		0.64	5.5		0.56	4	mV
				Full range			10.5			9	
			TL054AM	25°C		0.57	3.5		0.5	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL054M	25°C to 125°C		21			20		µV/°C
			TL054AM	25°C to 125°C		21			20		
I_{IO}	Input offset current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	$V_O = 0$, $V_{IC} = 0$, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$		25°C	3	4.2		13	13.9		V
				−55°C	3	4		13	13.8		
				125°C	3	4.4		13	14		
		$R_L = 2\ k\Omega$		25°C	2.5	3.8		11.5	12.7		
				−55°C	2.5	3.6		11.5	12.5		
				125°C	2.5	3.9		11.5	12.7		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$		25°C	−2.5	−3.5		−12	−13.2		V
				−55°C	−2.5	−3.1		−12	−12.9		
				125°C	−2.5	−3.9		−12	−13.6		
		$R_L = 2\ k\Omega$		25°C	−2.3	−3.2		−11	−12		
				−55°C	−2.3	−2.8		−11	−11.7		
				125°C	−2.3	−3.5		−11	−12		
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$, See Note 6		25°C	25	72		50	133		V/mV
				−55°C	30	99		60	209		
				125°C	10	35		15	35		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$		25°C	65	84		75	92		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, $V_O = 0$		25°C		8.1	11.2		8.4	11.2	mA
				−55°C		7.8	12.8		8.1	12.8	
				125°C		7.1	11.2		7.5	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$		25°C		120			120		dB

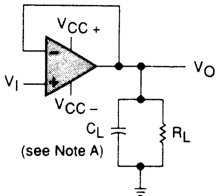
NOTE 6: At $V_{CC\pm} = \pm 5$ V, $V_O = \pm 2.3$ V; at $V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A	$V_{CC\pm} = \pm5$ V MIN	$V_{CC\pm} = \pm5$ V TYP	$V_{CC\pm} = \pm5$ V MAX	$V_{CC\pm} = \pm15$ V MIN	$V_{CC\pm} = \pm15$ V TYP	$V_{CC\pm} = \pm15$ V MAX	UNIT
SR+	Positive slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1, See Note 7		25°C		15.4		10	17.8		V/µs
				−55°C		16.7			18.3		
				125°C		12.9			16.7		
SR−	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				−55°C		14.7			16.3		
				125°C		12.2			14.5		
t_r	Rise time	$V_{IPP} = \pm10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figures 1 and 2		25°C		55			56		ns
				−55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				−55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				−55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		µV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$R_S = 1$ kΩ, $R_L = 2$ kΩ, f = 1 kHz, See Note 9		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		2.7			2.7		MHz
				−55°C		3.4			3.4		
				125°C		2.1			2.1		
ϕ_m	Phase margin at unity gain	$V_i = 10$ mV, $R_L = 2$ kΩ, $C_L = 25$ pF, See Figure 4		25°C		61°			64°		
				−55°C		58°			62°		
				125°C		60°			64°		

NOTES: 7. For $V_{CC\pm} = \pm5$ V, $V_{IPP} = \pm1$ V; for $V_{CC\pm} = \pm15$ V, $V_{IPP} = \pm5$ V.
9. For $V_{CC\pm} = \pm5$ V, $V_{O(rms)} = 1$ V; for $V_{CC\pm} = \pm15$ V, $V_{O(rms)} = 6$ V.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

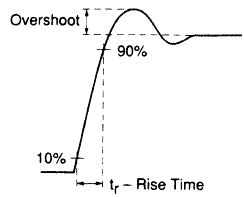


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

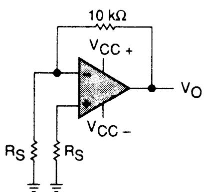
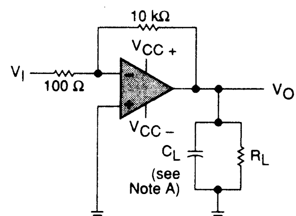


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

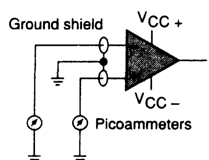


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

At the picoamp bias current level typical of the TL054 and TL054A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test is performed which measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet your application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of contents for graphs

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TL054
INPUT OFFSET VOLTAGE**

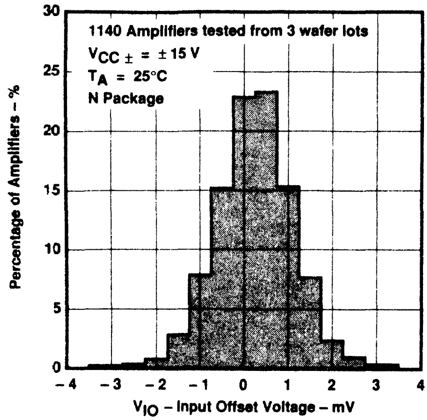


FIGURE 6

**DISTRIBUTION OF TL054
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

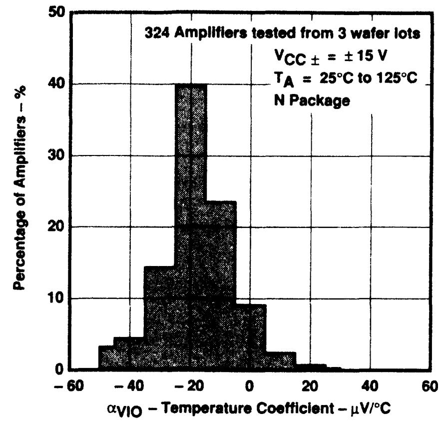


FIGURE 7

**INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

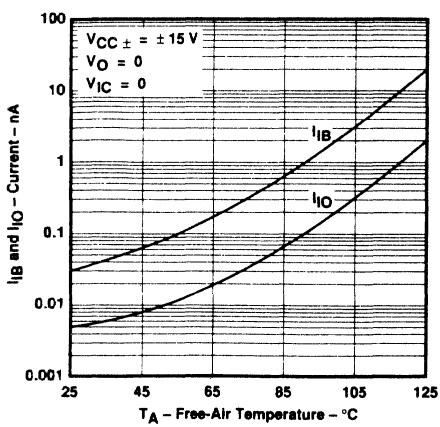


FIGURE 8

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

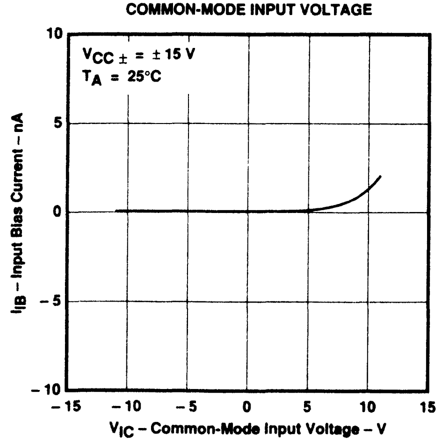


FIGURE 9

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

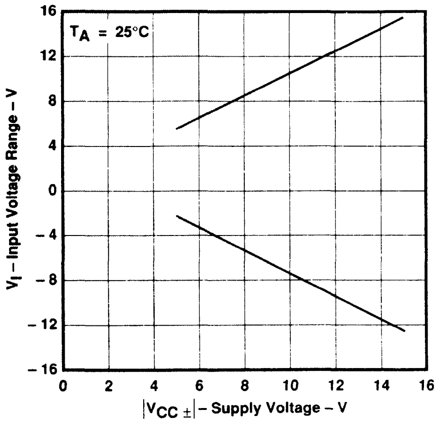


FIGURE 10

INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

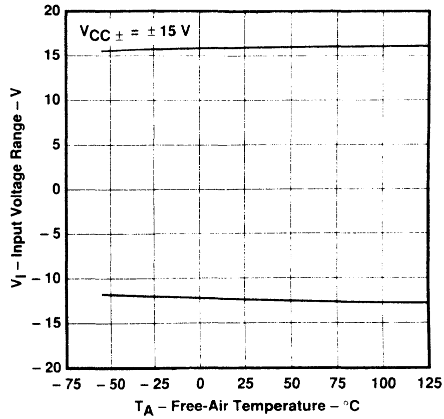


FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

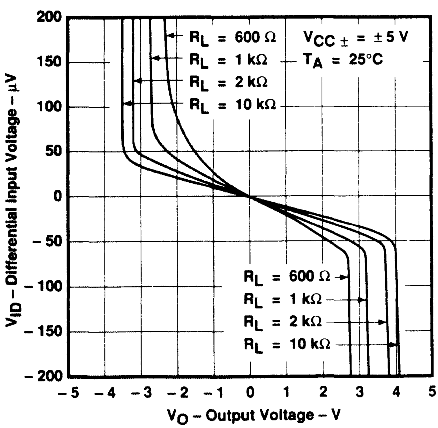


FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

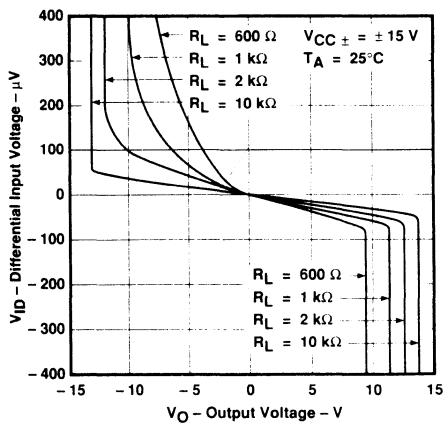


FIGURE 13

3
Operational Amplifiers

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

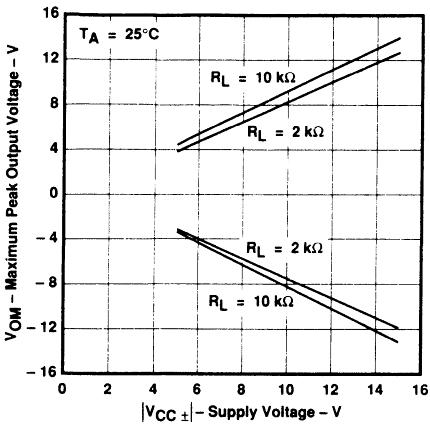


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

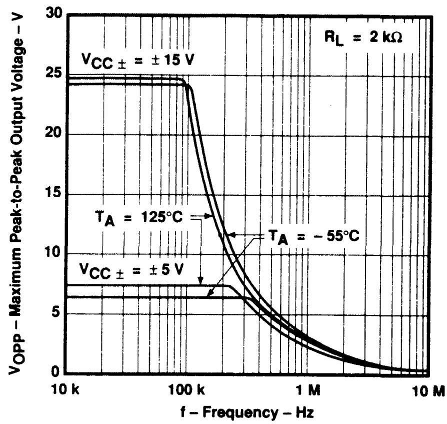


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

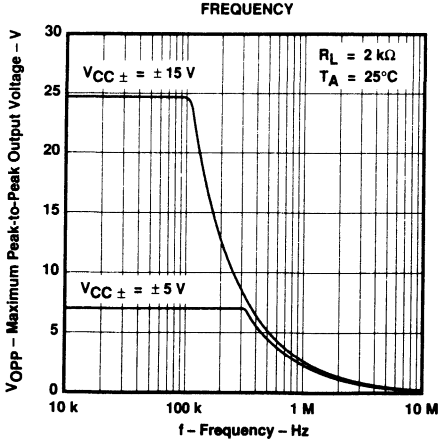


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

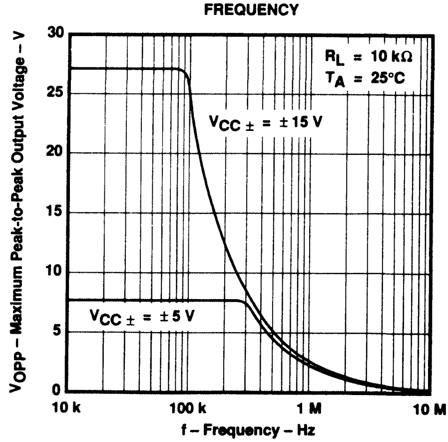


FIGURE 17

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

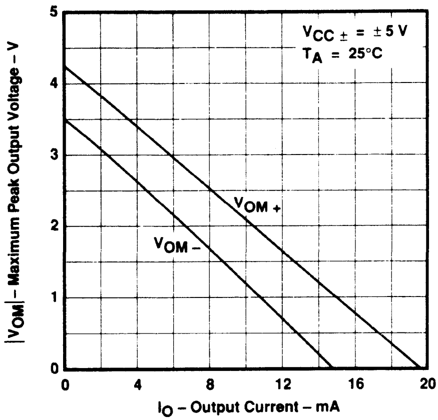


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

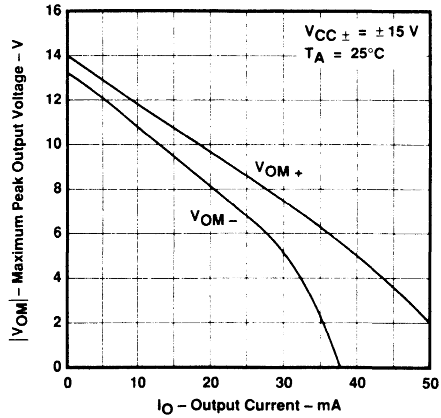


FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

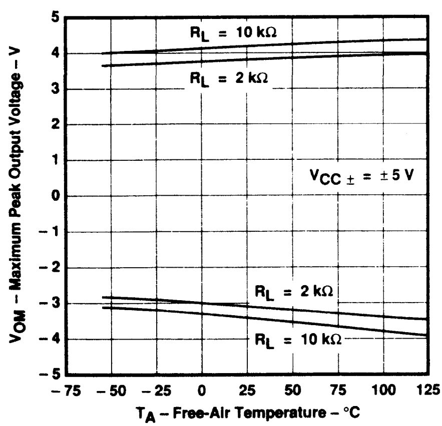


FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

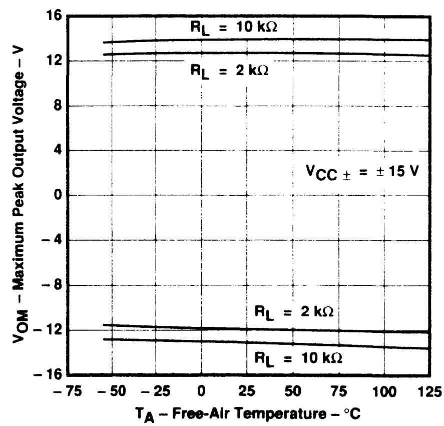


FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

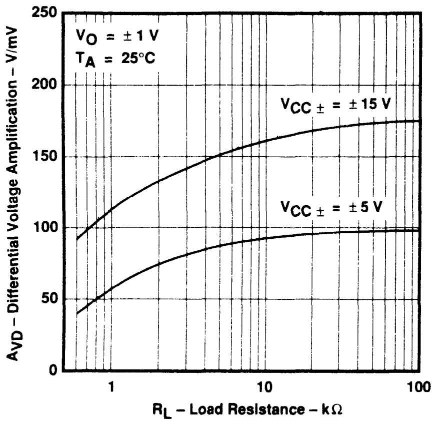


FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

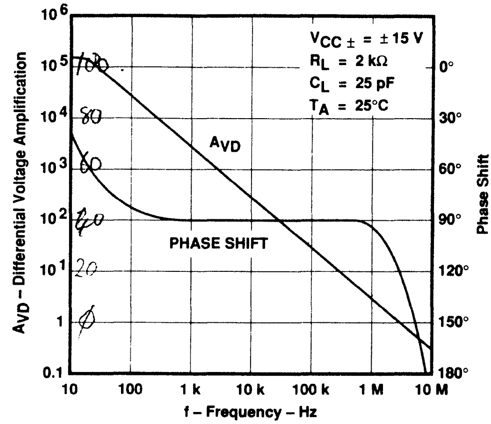


FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

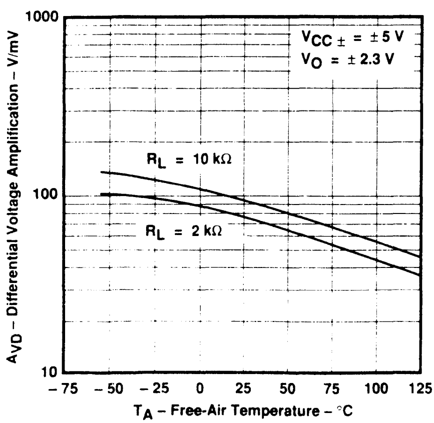


FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

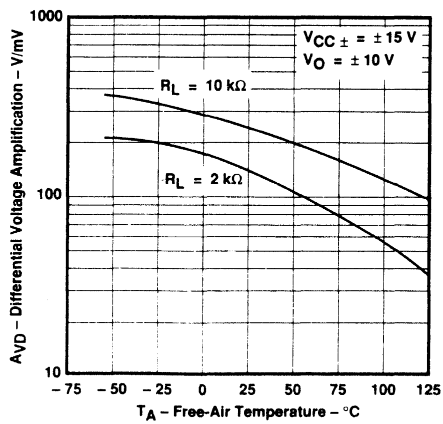


FIGURE 25

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

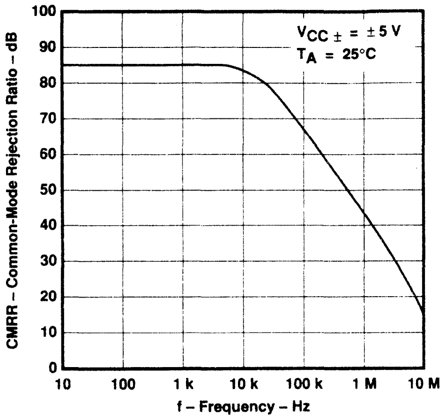


FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

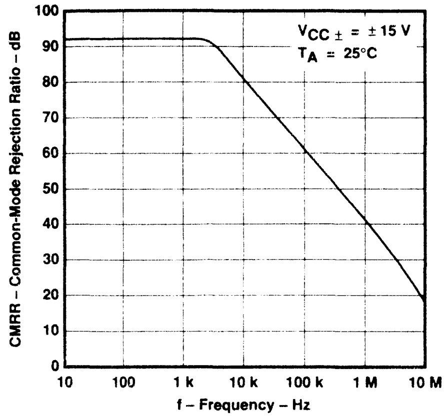


FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

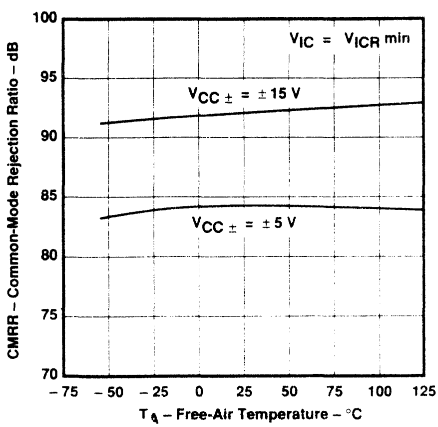


FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

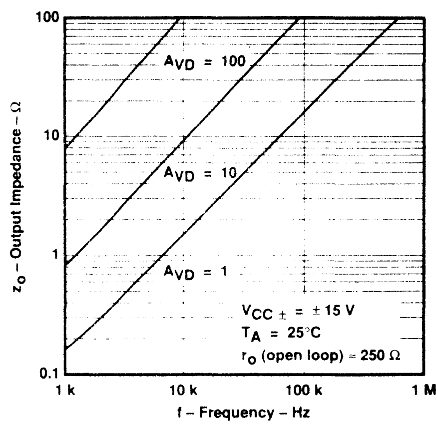


FIGURE 29

Operational Amplifiers 3

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

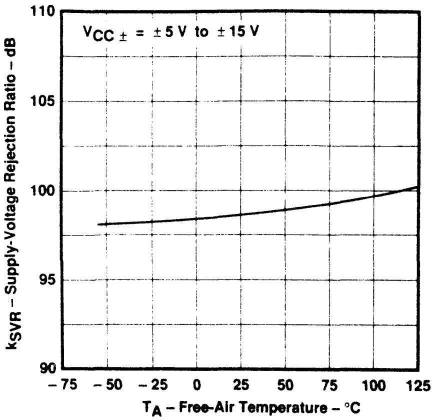


FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

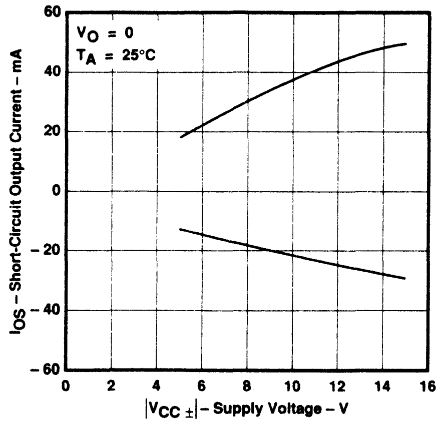


FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

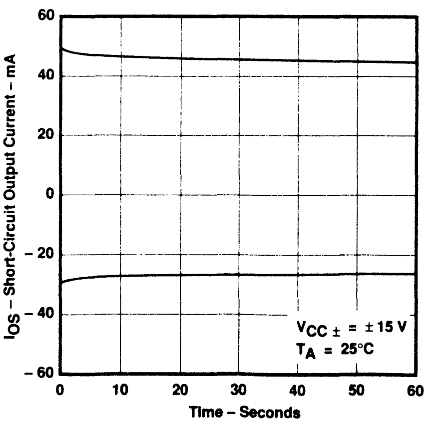


FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

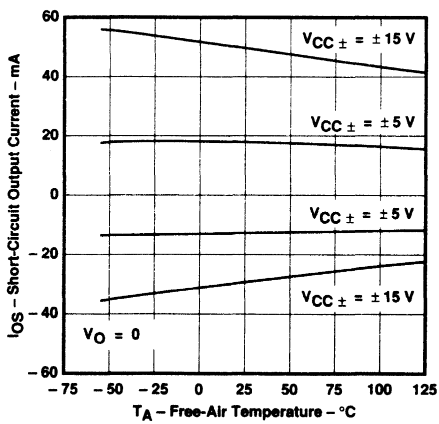


FIGURE 33

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

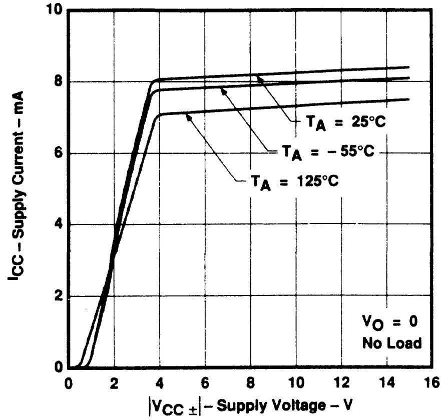


FIGURE 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

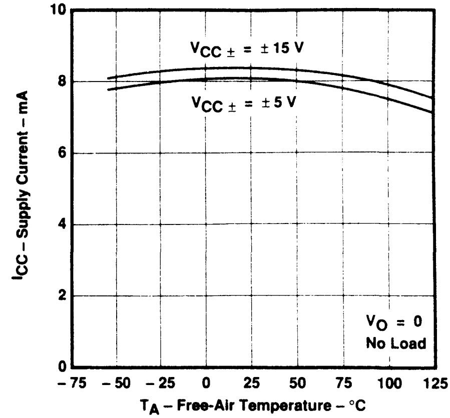


FIGURE 35

SLEW RATE
vs
LOAD RESISTANCE

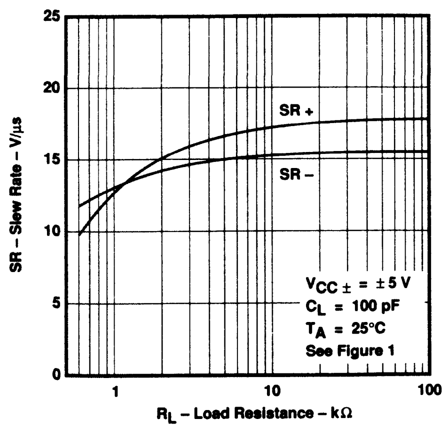


FIGURE 36

SLEW RATE
vs
LOAD RESISTANCE

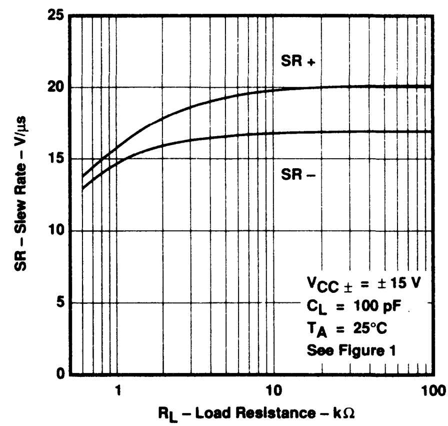


FIGURE 37

TYPICAL CHARACTERISTICS

SLEW RATE
vs
FREE-AIR TEMPERATURE

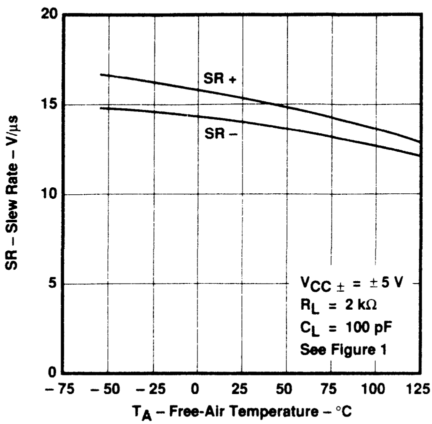


FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

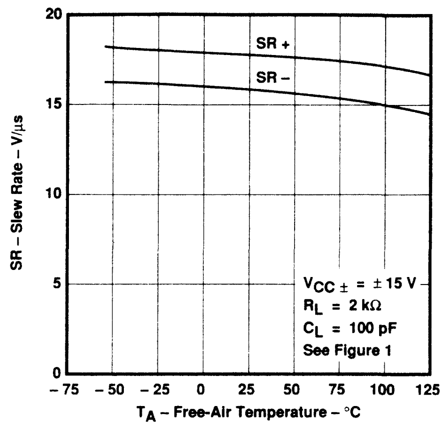


FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

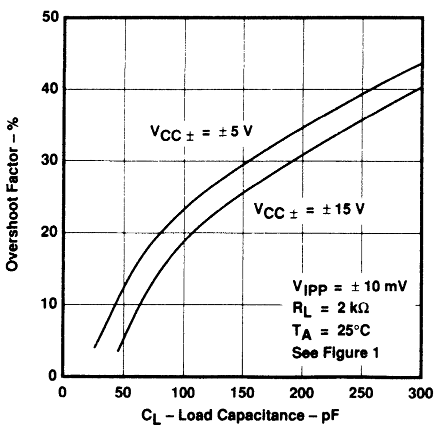


FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

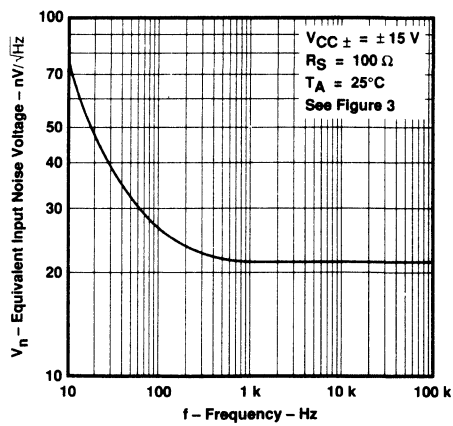


FIGURE 41

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

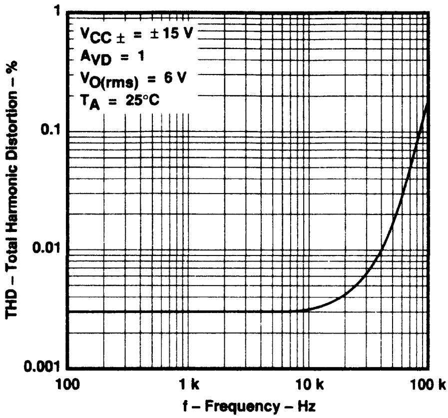


FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

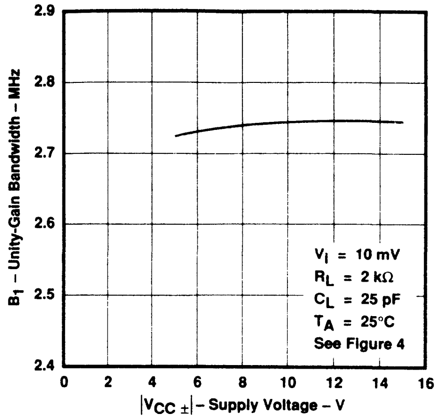


FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

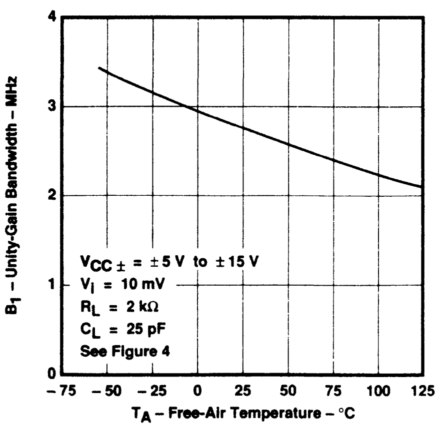


FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

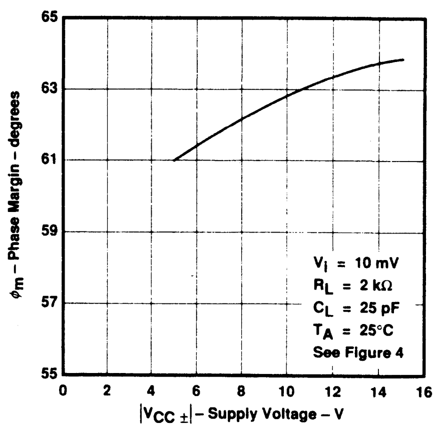


FIGURE 45

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

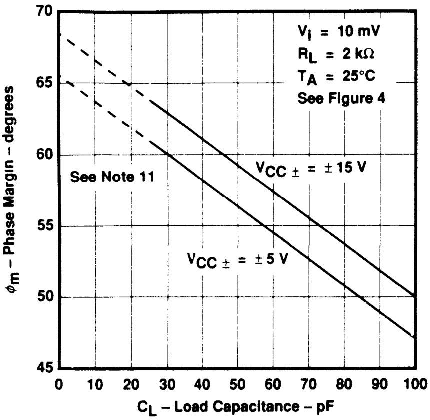


FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

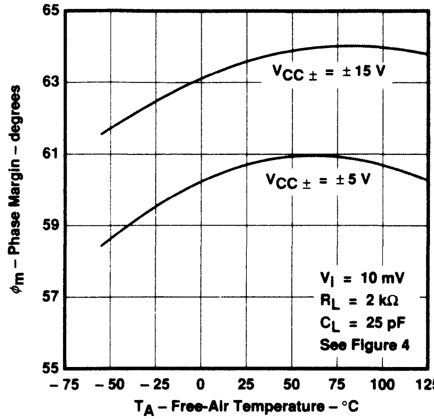


FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

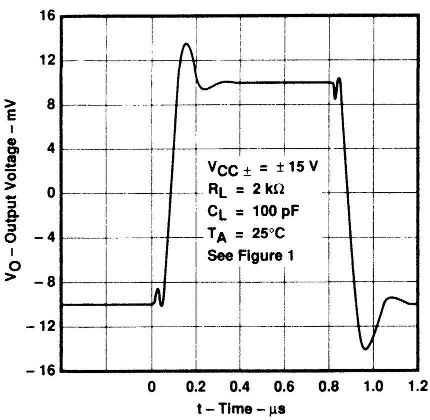


FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

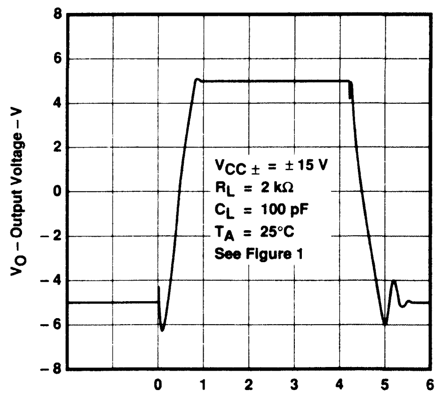


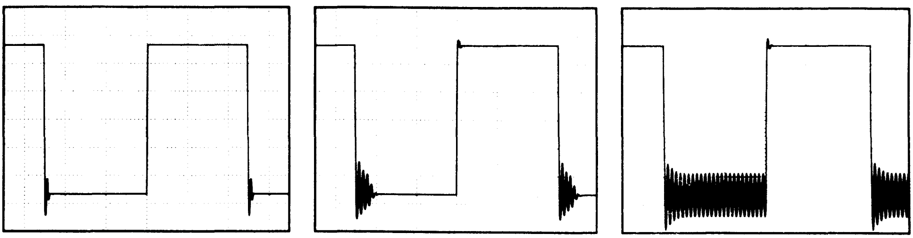
FIGURE 49

NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

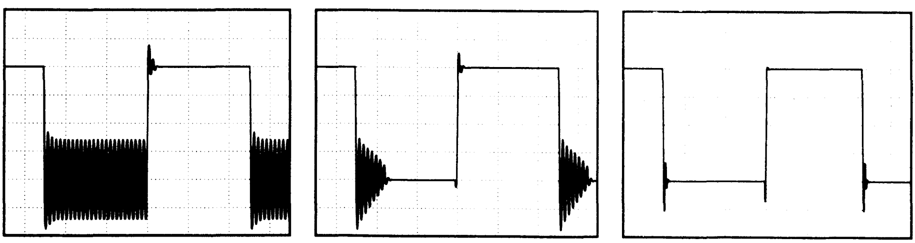
TYPICAL APPLICATION DATA

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL054 and TL054A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).

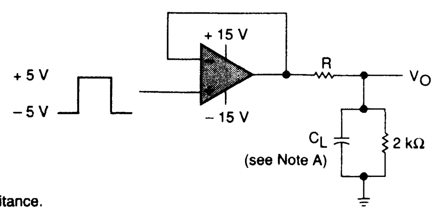


(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0



(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

3 Operational Amplifiers

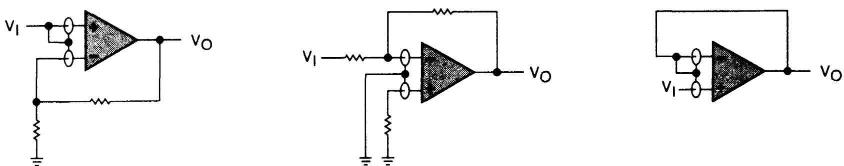
TYPICAL APPLICATION DATA

input characteristics

The TL054 and TL054A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL054 and TL054A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL054 and TL054A result in very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

instrumentation amplifier with adjustable gain/null

This instrumentation amplifier benefits greatly from the high input impedance and stable input offset voltage of the TL054A. Amplifiers A1, A2, and A3 form the actual instrumentation amplifier while A4 provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100 while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

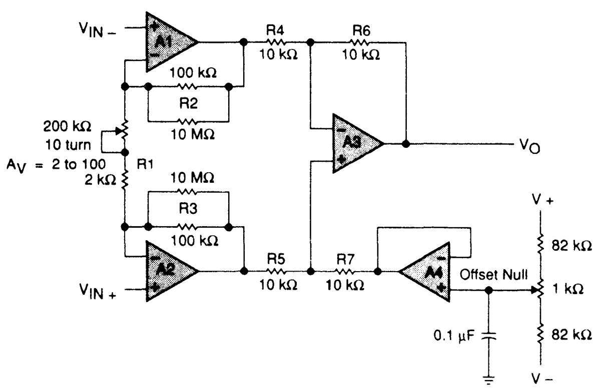
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if A4 is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL054A will minimize the DC error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 will control the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This DC error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature will also create an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs will minimize the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE: A1 thru A4 = TL054A; $V_{CC\pm} = \pm 15$ V.

TYPICAL APPLICATION DATA

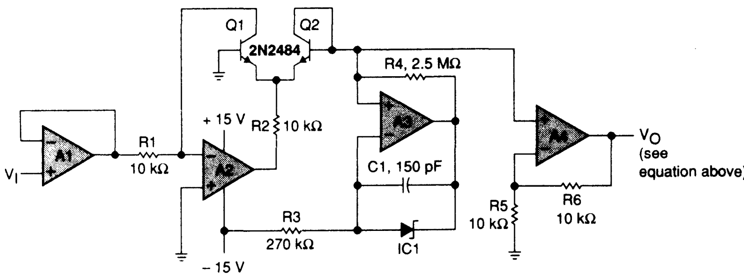
high input impedance log amplifier

The low input offset voltage and high input impedance of the TL054A create a precision log amplifier. IC1 is a 2.5 V precision low-current, shunt regulator. Transistors Q1 and Q2 must be a closely matched NPN pair. For best performance over temperature, R4 should be a metal film resistor with a low temperature coefficient.

In this circuit A1 serves as a high impedance unity-gain buffer. Amplifier A2 converts the input voltage to a current through R1 and Q1. Amplifier A3, IC1, and R4 form a one microamp temperature stable current source which sets the base-emitter voltage of Q2. Amplifier A4 then amplifies the difference between the base-emitter voltage of Q1 and Q2. The output voltage is given by the following equation:

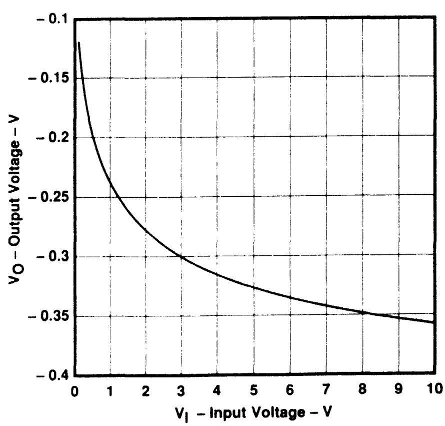
$$V_O = -\left[1 + \frac{R6}{R5}\right]\frac{kT}{q}\left[\ln\frac{V_I}{(R1 \times 1 \times 10^{-6})}\right]$$

where $k = 1.38 \times 10^{-23}$, $q = 1.602 \times 10^{-19}$, and T is in degrees Kelvin.



NOTES: A1 thru A4 = TL054A.
IC1 = LM385, LT1004, or LT1009 voltage reference.

OUTPUT VOLTAGE
vs
INPUT VOLTAGE



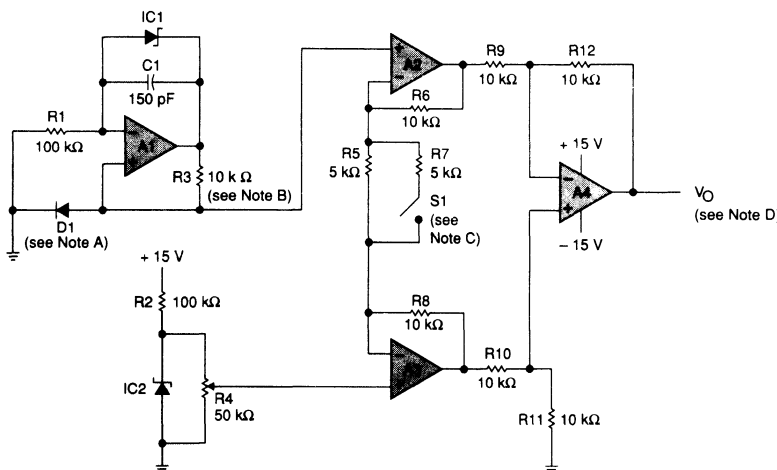
TYPICAL APPLICATION DATA

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built. Amplifier A1 and IC1 establish a constant current through the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL054 must use split supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature sensitive voltage from the diode is compared to a temperature stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer will remain constant.

Amplifiers A2, A3, and A4 form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A1 thru A4 = TL054.
IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.
A. Temperature sensing diode ≈ (− 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. $V_O \propto$ Temp; 10 mV/°C or 10 mV/°F.

3

Operational Amplifiers

TYPICAL APPLICATION DATA

voltage ratio to dB converter

This application measures the amplitude ratio of two signals and then converts the ratio to decibels. The output voltage provides a resolution of 100 mV/dB. The two inputs can be either DC or sinusoidal AC signals. When using AC signals, both signals should be the same frequency or output glitches will occur. For measuring two input signals of different frequencies, extra filtering should be added after the rectifiers.

The circuit contains three low-offset TL054A devices. Two of these devices provide the rectification and logarithmic conversion of the inputs. The third TL054A forms an instrumentation amplifier. The stage performing the logarithmic conversion also requires two well-matched NPN transistors.

The input signal first passes through a high impedance unity-gain buffer A1 (A5). Then A2 (A6) rectifies the input signal at a gain of 0.5, and A3 (A7) provides a non-inverting gain of 2 so that the system gain is still one. A4 (A8), R6 (R13), and Q1 (Q2) perform the logarithmic conversion of the rectified input signal. The instrumentation amplifier formed by A9, A10, A12 scales the difference of the two logarithmic voltages by a gain of 33.6. As a result, the output voltage equals 100 mV/dB. The 1 kΩ potentiometer on the input of A11 calibrates the zero dB reference level.

$$X\,dB = 20\log\left[\frac{V_A}{V_B}\right] = 20\left[\frac{\ln(V_A) - \ln(V_B)}{\ln(10)}\right]$$

$$X\,dB = 8.686\left[\ln(V_A) - \ln(V_B)\right]$$

$$V_{BE(Q1)} = \frac{kT}{q}\ln\left[\frac{V_A}{R \times I_S}\right] \qquad V_{BE(Q2)} = \frac{kT}{q}\ln\left[\frac{V_B}{R \times I_S}\right]$$

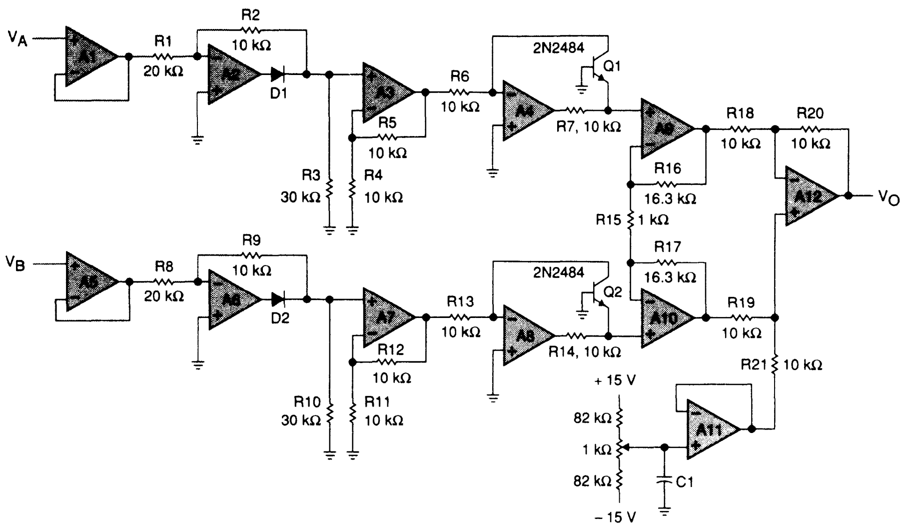
$$\Delta V_{BE} = V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q}\left[\ln(V_A) - \ln(V_B)\right]$$

$$X\,dB = \frac{8.686}{kT/q}\left[V_{BE(Q1)} - V_{BE(Q2)}\right] = 336\left[V_{BE(Q1)} - V_{BE(Q2)}\right] \text{ at } 25°C.$$

where $k = 1.38 \times 10^{-23}$, $q = 1.602 \times 10^{-19}$, and T is in degrees Kelvin.

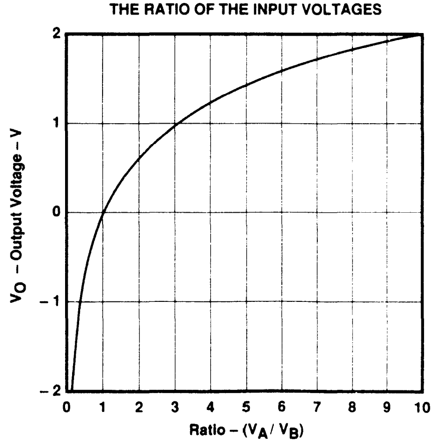
This would give a resolution of 1 V/dB. Therefore, the gain of the instrumentation amplifier is set at 33.6 to obtain 100 mV/dB.

TYPICAL APPLICATION DATA



NOTES: A1 thru A12 = TL054A, $V_{CC\pm}$ = ± 15 V.
D1 and D2 = 1N914.

OUTPUT VOLTAGE
vs
THE RATIO OF THE INPUT VOLTAGES



TYPES TL060, TL060A, TL060B, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

D2392, NOVEMBER 1978—REVISED AUGUST 1983

20 DEVICES COVER MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

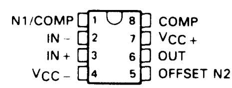
- Very Low Power Consumption
- Typical Supply Current . . . 200 μA (per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common mode input voltage range includes Vcc+
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL060)
- Latch-Up Free Operation
- High Slew Rate . . . . 3.5 V/μs Typ

description

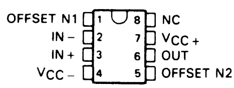
The JFET-input operational amplifiers of the TL061 series are designed as low-power versions of the TL081 series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL061 series features the same terminal assignments as the TL071 and TL081 series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55 °C to 125 °C, those with an "I" suffix are characterized for operation from −25 °C to 85 °C, and those with a "C" suffix are characterized for operation from 0 °C to 70 °C.

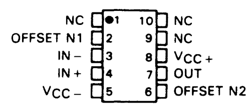
TL060, TL060A, TL060B
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



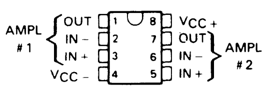
TL061, TL061A, TL061B
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



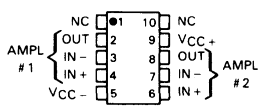
TL061
U FLAT PACKAGE
(TOP VIEW)



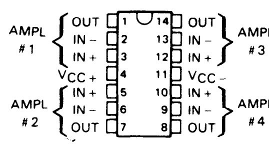
TL062, TL062A, TL062B
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



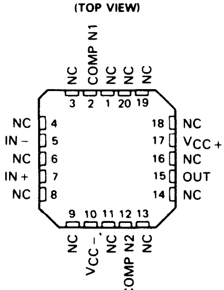
TL062
U FLAT PACKAGE
(TOP VIEW)



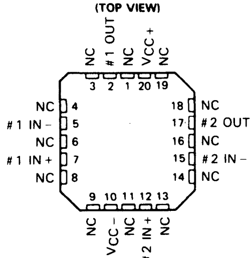
TL064 . . . D, J, N, OR W PACKAGE
TL064A, TL064B . . . D, J, OR N PACKAGE
(TOP VIEW)



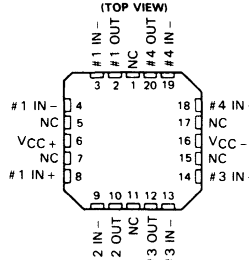
TL061
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



TL062
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



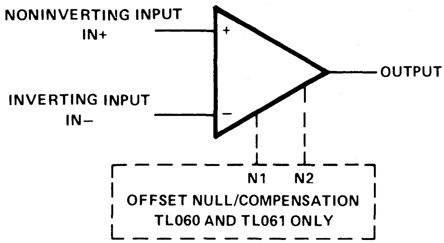
TL064
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



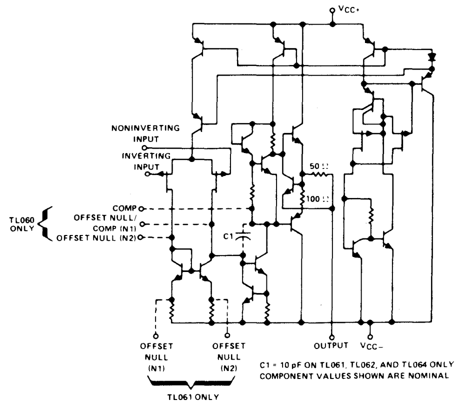
NC—No internal connection

TYPES TL060, TL060A, TL060B, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL06_M	TL06_I	TL06_C TL06_AC TL06_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	D package		680	680	mW
	FK package	680			mW
	J, JG, N, P, or W package	680	680	680	mW
	U package	675			mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, FK, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG packages, TL06_M chips are alloy-mounted; TL06_I, TL06_C, TL06_AC, and TL06_BC chips are glass-mounted.

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL060	TL061	TL062	TL064
TL06_M	JG	FK, JG, U	FK, JG, U	FK, J, W
TL06_I	D, JG, P	D, JG, P	D, JG, P	D, J, N
TL06_C	D, JG, P	D, JG, P	D, JG, P	D, J, N
TL06_AC	D, JG, P	D, JG, P	D, JG, P	D, J, N
TL06_BC	D, JG, P	D, JG, P	D, JG, P	D, J, N

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL060M TL061M TL062M MIN	TYP	MAX	TL064M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	9	mV
			T_A = −55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55°C to 125°C			10			10		μV/°C
I_{IO}	Input offset * current‡	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = −55°C to 125°C			20			20	nA
I_{IB}	Input bias current*	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = −55°C to 125°C			50			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	+15 −12		±11.5	+15 −12		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ, T_A = 25°C		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ, T_A = −55°C to 125°C		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L ≥ 10 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = −55°C to 125°C	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, V_O = 0, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, V_O = 0, T_A = 25°C			200	250		200	250	μA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.
*For M suffix devices these parameters are guaranteed but not tested.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TL060I TL061I TL062I TL064I			TL060C TL061C TL062C TL064C			TL060AC TL061AC TL062AC TL064AC			TL060BC TL061BC TL062BC TL064BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	15		3	6		2	3	mV
			T_A = full range			9			20			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			10			10			10			10		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	200		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	400		30	400		30	400		30	400	pA
			T_A = full range			20			10			7			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11.5	+15 −12		±11	+15 −12		±11.5	+15 −12		±11.5	+15 −12		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$, $T_A = 25°C$		±10	±13.5		±10	±13.5		±10	±13.5		±10	±13.5		V
		$R_L \geq 10\ k\Omega$, T_A = full range		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 10\ k\Omega$	$T_A = 25°C$	4	6		3	6		4	6		4	6		V/mV
			T_A = full range	4			3			4			4			
B_1	Unity-gain bandwidth	$R_L = 10\ k\Omega$, $T_A = 25°C$			1			1			1			1		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	86		70	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio $(\Delta V_{CC\pm}/\Delta V_{IO})$	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	95		70	95		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			6	7.5		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, $V_O = 0$, $T_A = 25°C$			200	250		200	250		200	250		200	250	μA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

†All characteristics are measured under optn-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −25°C to 85°C for TL06_I and 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 10 kΩ,		0.2		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

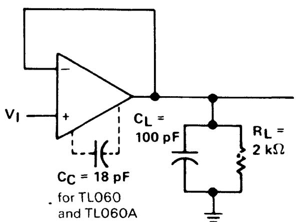


FIGURE 1—UNITY-GAIN AMPLIFIER

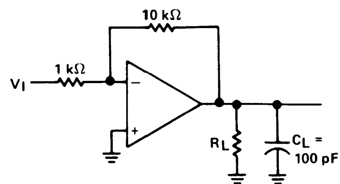


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

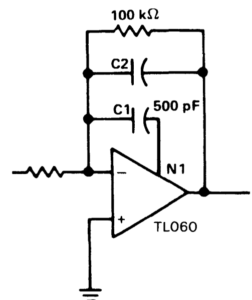
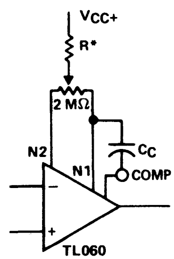


FIGURE 3—FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS



*For best results use R = 20 MΩ for $V_{CC\pm} = \pm 15$ V to R = 5 MΩ for $V_{CC\pm} = \pm 3$ V.

FIGURE 4

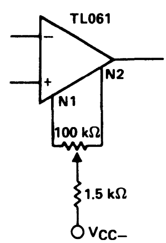


FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

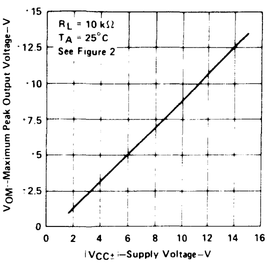


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

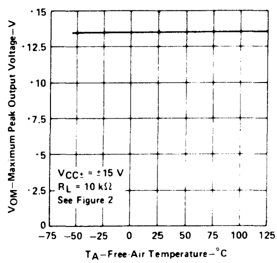


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

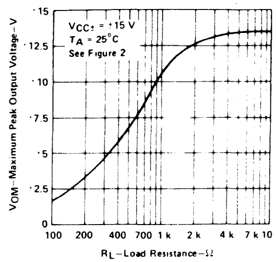


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

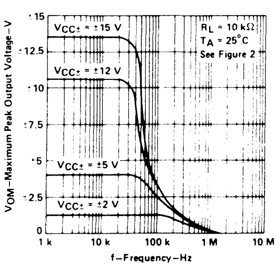


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

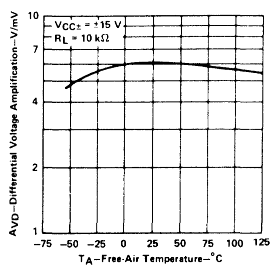


FIGURE 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

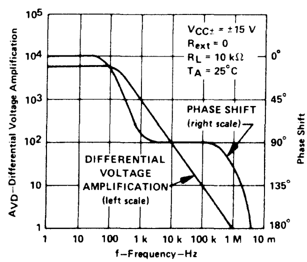


FIGURE 11

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE

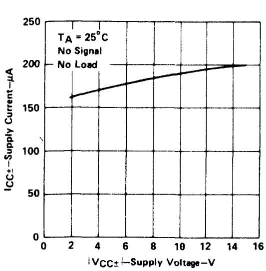


FIGURE 12

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

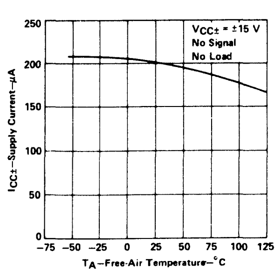


FIGURE 13

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

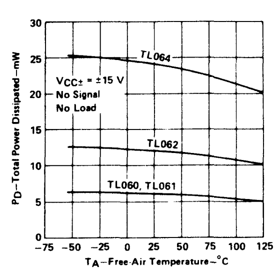


FIGURE 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL CHARACTERISTICS†

ALL EXCEPT TL06_C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

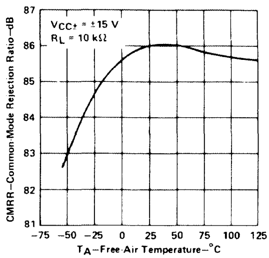


FIGURE 15

NORMALIZED UNITY-GAIN BANDWIDTH,
SLEW RATE, and PHASE SHIFT
vs
FREE-AIR TEMPERATURE

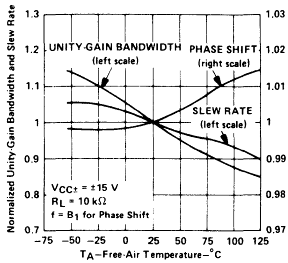


FIGURE 16

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

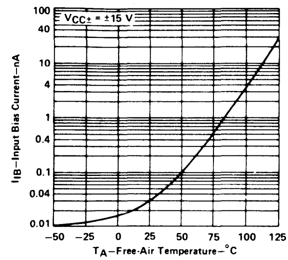


FIGURE 17

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

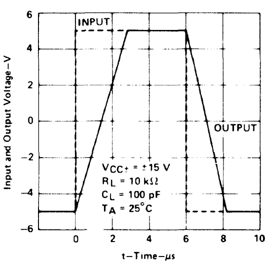


FIGURE 18

OUTPUT VOLTAGE
vs
ELAPSED TIME

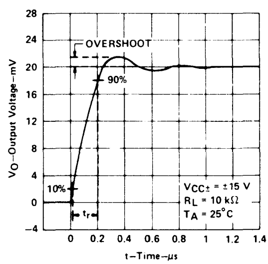


FIGURE 19

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

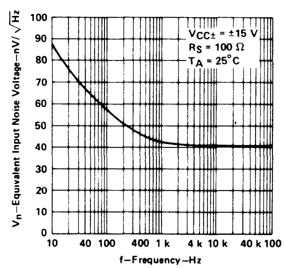


FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL APPLICATION DATA

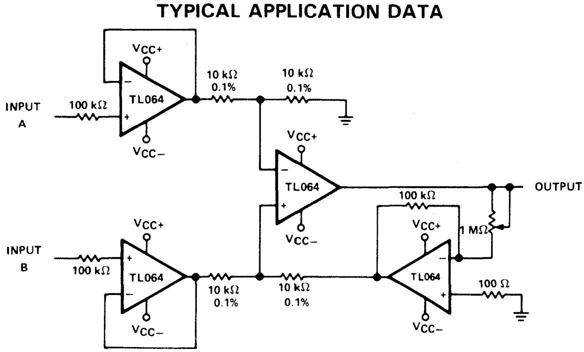


FIGURE 21—INSTRUMENTATION AMPLIFIER

TYPICAL APPLICATION DATA

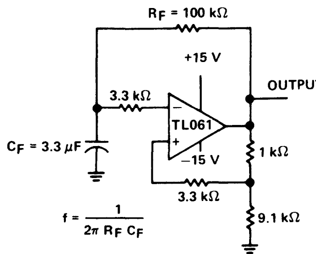


FIGURE 22—0.5-Hz SQUARE-WAVE OSCILLATOR

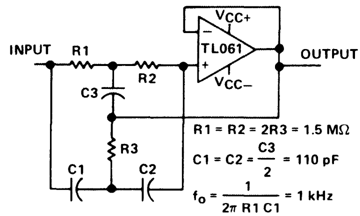


FIGURE 23—HIGH-Q NOTCH FILTER

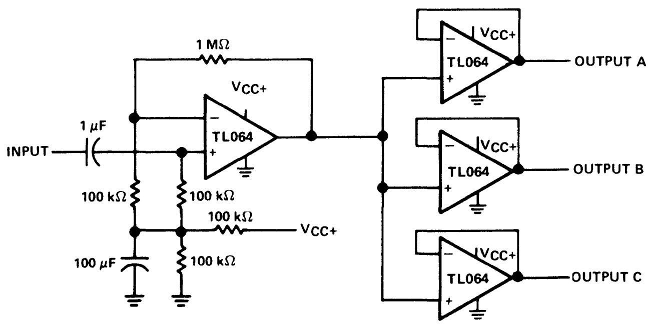


FIGURE 24—AUDIO DISTRIBUTION AMPLIFIER

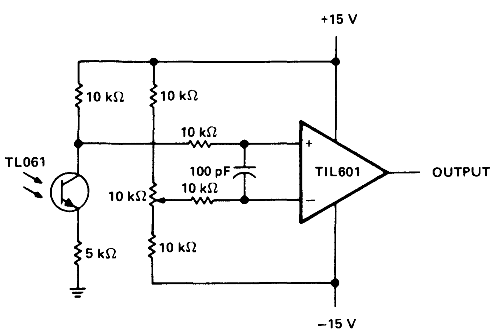


FIGURE 25—LOW-LEVEL LIGHT DETECTOR PREAMPLIFIER

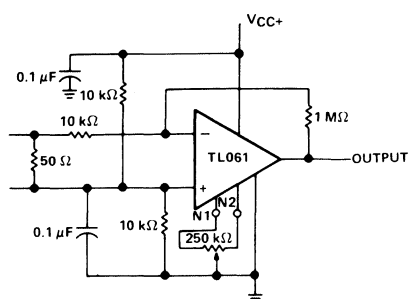


FIGURE 26—AC AMPLIFIER

TYPICAL APPLICATION DATA

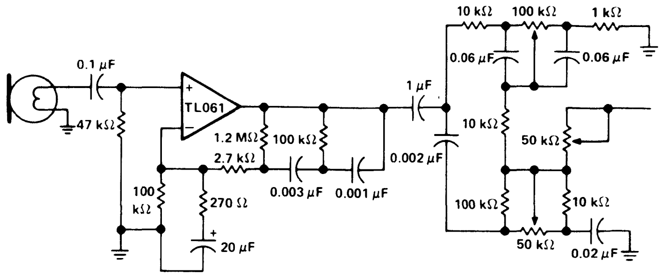


FIGURE 27—MICROPHONE PREAMPLIFIER WITH TONE CONTROL

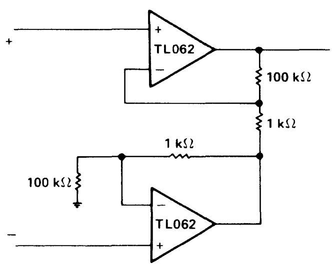


FIGURE 28—INSTRUMENTATION AMPLIFIER

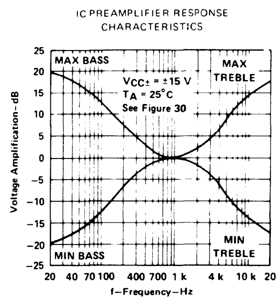


FIGURE 29

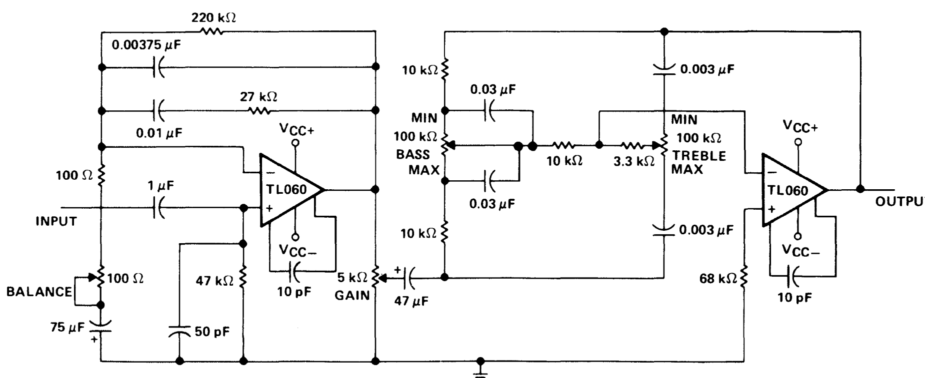


FIGURE 30—IC PREAMPLIFIER

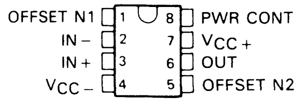
TYPES TL066M, TL066I, TL066C, TL066AC, TL066BC
ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

D2494, FEBRUARY 1979—REVISED AUGUST 1983

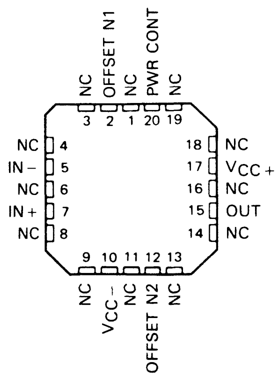
5 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Very Low, Adjustable ("Programmable") Power Consumption
- Adjustable Supply Current . . . 5 μA to 200 μA
- Very Low Input Bias and Offset Currents
- Wide Supply Range . . . ±1.2 V to ±18 V
- Wide Common-Mode and Differential Voltage Range
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Unity-Gain Bandwidth . . . 1 MHz Typ (100 kHz at 25 μW)
- High Slew Rate . . . 3.5 V/μs Typ
- Internal Frequency Compensation
- Latch-Up-Free Operation
- Common mode input voltage range includes Vcc+

TL066M . . . JG PACKAGE
TL066I, TL066C, TL066AC, TL066BC . . . D, JG, OR P PACKAGE
(TOP VIEW)



TL066M . . . FK PACKAGE
(TOP VIEW)

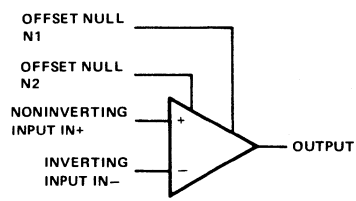


NC—No internal connection

description

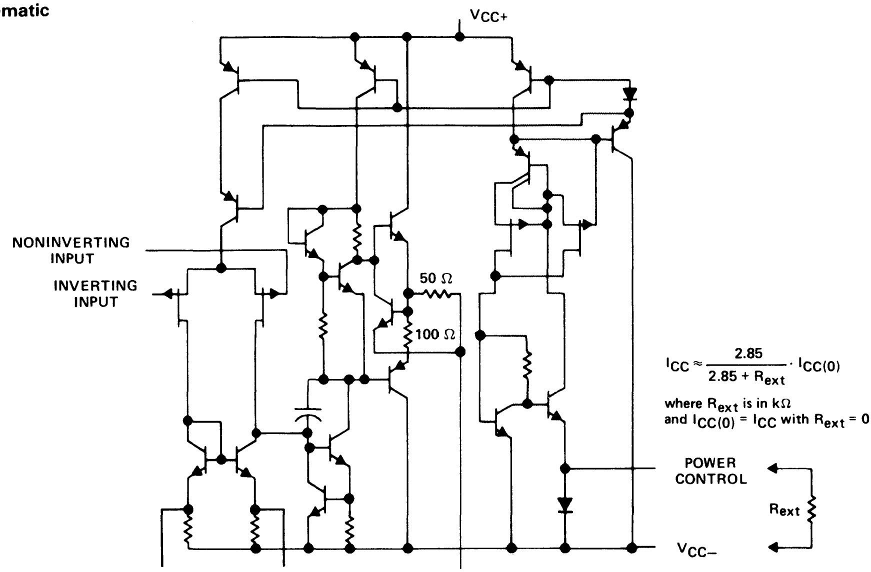
The TL066, TL066A, and TL066B are JFET-input operational amplifiers similar to the TL061 with the additional feature of being power-adjustable. They feature very low input offset and bias currents, high input impedance, wide bandwidth, and high slew rate. The power-control feature permits the amplifiers to be adjusted to require as little as 25 microwatts of power. This type of amplifier, which provides for changing several characteristics by varying one external element, is sometimes referred to as being "programmable." The JFET-input stage combined with the adjustable-low-power feature results in superior bandwidth and slew rate performance compared to low-power bipolar-input devices.

symbol



The TL066M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL066I is characterized for operation from −25°C to 85°C; the TL066C, TL066AC, and TL066BC are characterized for operation from 0°C to 70°C.

schematic



$I_{CC} \approx \frac{2.85}{2.85 + R_{ext}} \cdot I_{CC(0)}$

where R_{ext} is in kΩ
and $I_{CC(0)} = I_{CC}$ with $R_{ext} = 0$

COMPONENT VALUES SHOWN ARE NOMINAL

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

		TL066M	TL066I	TL066C TL066AC TL066BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Voltage between power-control terminal and V_{CC-}		±0.5	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		680	680	680	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, or JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the JG package, the TL066I, TL066C, TL066AC, and TL066BC chips are glass-mounted; the TL066M chips are alloy-mounted.

electrical characteristics, V_{CC} = ±15 V

PARAMETER		TEST CONDITIONS†	TL066M MIN	TL066M TYP	TL066M MAX	TL066I MIN	TL066I TYP	TL066I MAX	TL066C MIN	TL066C TYP	TL066C MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω, T_A = 25°C		3	6		3	6		3	15	mV
		V_O = 0, R_S = 50 Ω, T_A = full range			9			9			20	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = full range		10			10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0, T_A = 25°C		5	100		5	100		5	200	pA
		V_O = 0, T_A = full range			20			10			5	nA
I_{IB}	Input bias current‡	V_O = 0, T_A = 25°C		30	200		30	200		30	400	pA
		V_O = 0, T_A = full range			50			20			10	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C	±11.5	+15 −12		±11.5	+15 −12		±11	+15 −12		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C, $R_L \geq$ 10 kΩ	±10	±13.5		±10	±13.5		±10	±13.5		V
		T_A = full range, $R_L \geq$ 10 kΩ	±10	±13.5		±10	±13.5		±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 10 kΩ, V_O = ±10 V, T_A = 25°C	4	6		4	6		3	6		V/mV
		$R_L \geq$ 10 kΩ, V_O = ±10 V, T_A = full range	4						3			
B_1	Unity-gain bandwidth	T_A = 25°C, R_L = 10 kΩ		1			1			1		MHz
r_i	Imput resistance	T_A = 25°C		10^{12}			10^{12}			10^{12}		Ω
r_o	Output resistance	T_A = 25°C, f = 1 kHz		220			220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C	80	86		80	86		70	76		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω, T_A = 25°C	80	95		80	95		70	95		dB
P_D	Total power dissipation	V_O = 0, No load, T_A = 25°C		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current	V_O = 0, No load, T_A = 25°C		200	250		200	250		200	250	μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of T_A is −55°C to 125°C for TL066M; −25°C to 85°C for TL066I; and 0°C to 70°C for TL066C. The electrical parameters are measured with the power-control terminal (pin 8) connected to V_{CC-}.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

electrical characteristics, $V_{CC} = \pm 15$ V

PARAMETER		TEST CONDITIONS†		TL066AC			TL066BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $T_A = 25°C$	$R_S = 50\ \Omega$,		3	6		2	3	mV
		$V_O = 0$, T_A = full range	$R_S = 50\ \Omega$,			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, T_A = full range	$R_S = 50\ \Omega$,		10			10		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$,	$T_A = 25°C$		5	100		5	100	pA
		$V_O = 0$,	T_A = full range			3			3	nA
I_{IB}	Input bias current‡	$V_O = 0$,	$T_A = 25°C$		30	200		30	200	pA
		$V_O = 0$,	T_A = full range			7			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11.5	+15 −12		±11.5	+15 −12		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$,	$R_L \geq 10\ k\Omega$,	±10	±13.5		±10	±13.5		V
		T_A = full range,	$R_L \geq 10\ k\Omega$	±10	±13.5		±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	$V_O = \pm 10$ V,	4	6		4	6		V/mV
		$R_L \geq 10\ k\Omega$, T_A = full range	$V_O = \pm 10$ V,	4			4			
B_1	Unity-gain bandwidth	$T_A = 25°C$,	$R_L = 10\ k\Omega$		1			1		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
r_o	Output resistance	$T_A = 25°C$,	f = 1 kHz		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio $(\Delta V_{CC\pm}/\Delta V_{IO})$	$V_{CC} = \pm 9$ V to ± 15 V, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	95		80	95		dB
P_D	Total power dissipation	No load, $T_A = 25°C$	$V_O = 0$,		6	7.5		6	7.5	mW
I_{CC}	Supply current	No load, $T_A = 25°C$	$V_O = 0$,		200	250		200	250	μA

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of $T_A = -55°C$ to 125°C for TL066M; −25°C to 85°C for TL066I; and 0°C to 70°C for TL066C, TL066AC, and TL066BC. The electrical parameters are measured with the power-control terminal (pin 8) connected to V_{CC-}.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$, $R_{ext} = 0$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10$ kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10$ kΩ		0.2		μs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω,	f = 1 kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

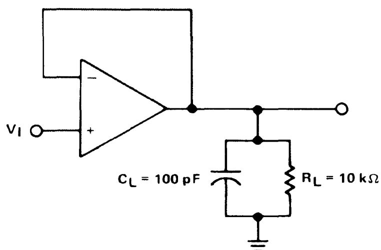


FIGURE 1—UNITY-GAIN AMPLIFIER

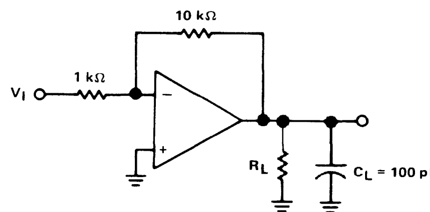


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

INPUT OFFSET VOLTAGE NULL CIRCUIT

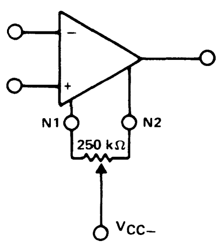


FIGURE 3

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

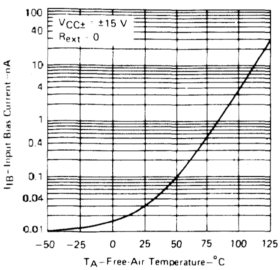


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

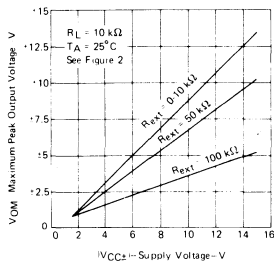


FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
EXTERNAL-CONTROL RESISTANCE

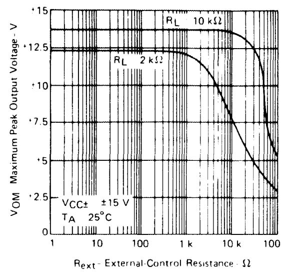


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

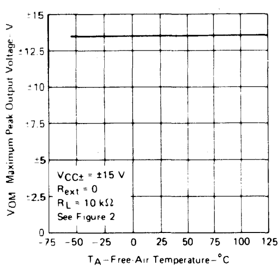


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

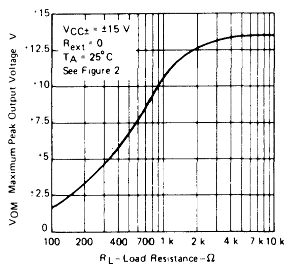


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

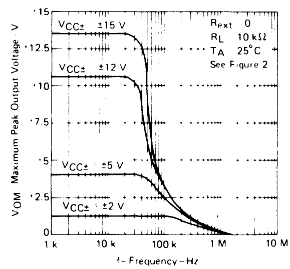


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
EXTERNAL-CONTROL RESISTANCE

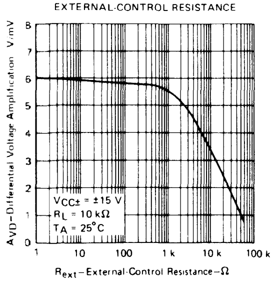


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

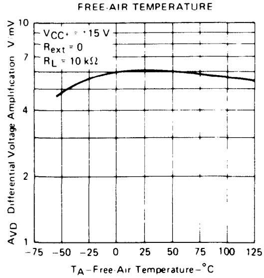


FIGURE 11

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

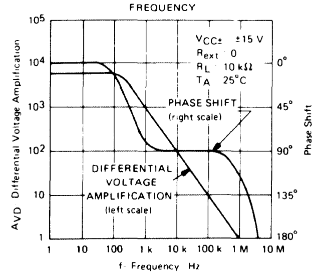


FIGURE 12

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

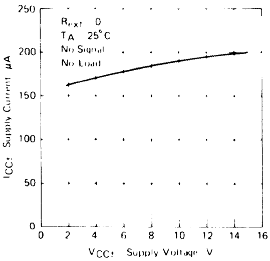


FIGURE 13

SUPPLY CURRENT
vs
EXTERNAL CONTROL RESISTANCE

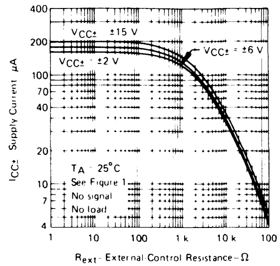


FIGURE 14

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

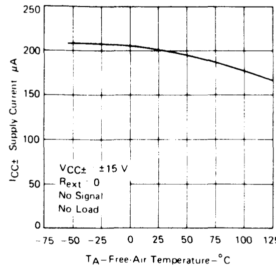


FIGURE 15

TOTAL POWER DISSIPATION
vs
EXTERNAL-CONTROL RESISTANCE

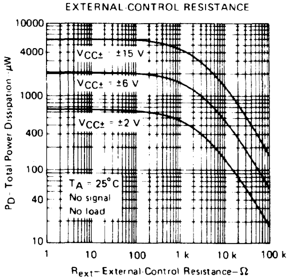


FIGURE 16

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
EXTERNAL-CONTROL RESISTANCE

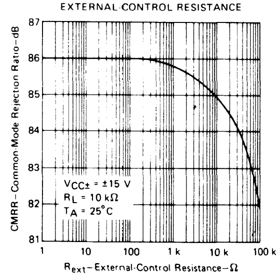


FIGURE 17

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

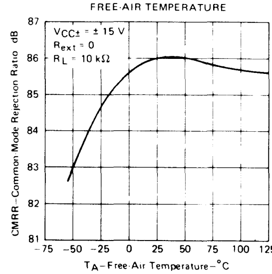


FIGURE 18

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

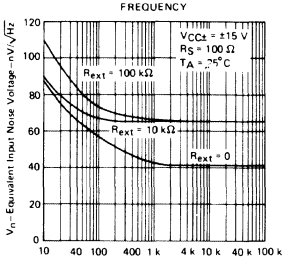


FIGURE 19

EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

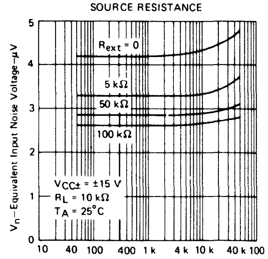


FIGURE 20

UNITY GAIN BANDWIDTH
vs
EXTERNAL-CONTROL RESISTANCE

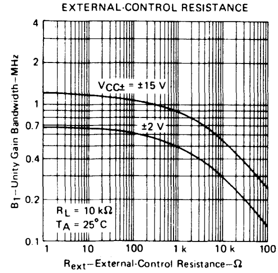


FIGURE 21

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

3

Operational Amplifiers

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
EXTERNAL-CONTROL RESISTANCE

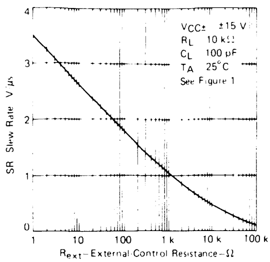


FIGURE 22

NORMALIZED UNITY-GAIN BANDWIDTH,
SLEW RATE, and PHASE SHIFT
vs
FREE-AIR TEMPERATURE

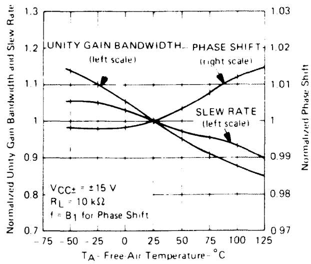


FIGURE 23

VOLTAGE FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

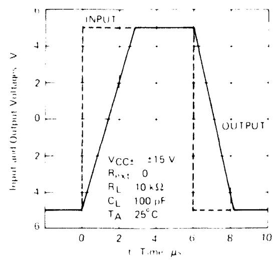


FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

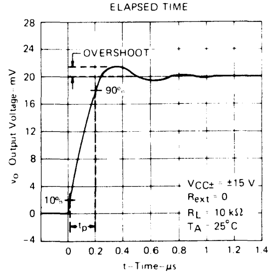


FIGURE 25

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

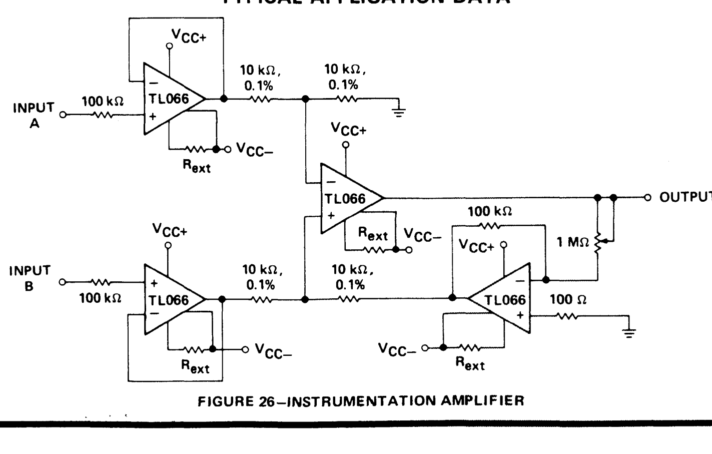


FIGURE 26—INSTRUMENTATION AMPLIFIER

3 Operational Amplifiers

883

TEXAS INSTRUMENTS

TYPICAL APPLICATION DATA

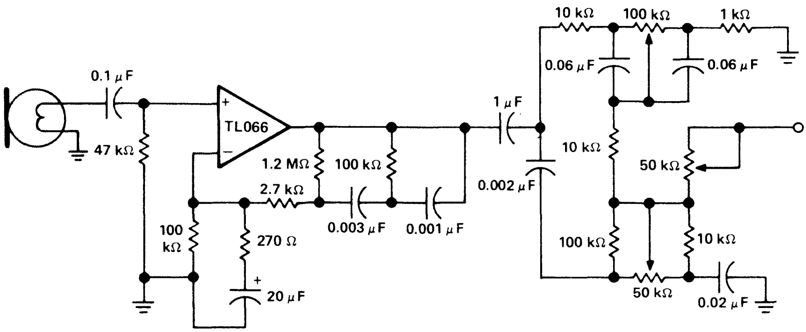


FIGURE 27—MICROPHONE PREAMPLIFIER WITH TONE CONTROL

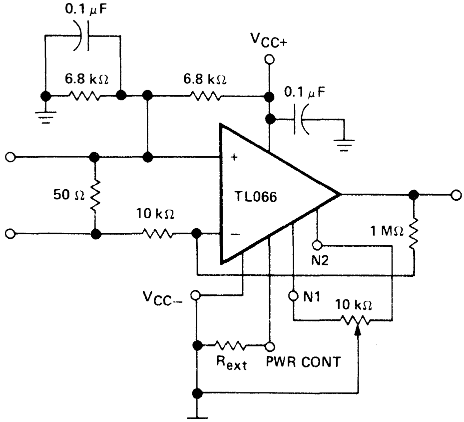


FIGURE 28—AC AMPLIFIER

TYPICAL APPLICATION DATA

IC PREAMPLIFIER RESPONSE CHARACTERISTICS

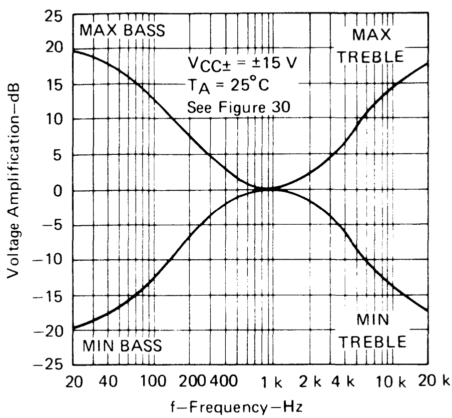


FIGURE 29

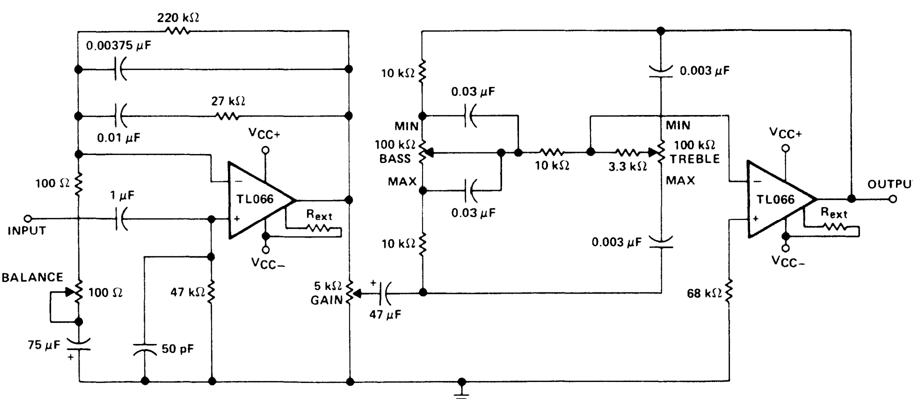


FIGURE 30–IC PREAMPLIFIER

TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075 LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

D2393, SEPTEMBER 1978—REVISED SEPTEMBER 1983

19 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

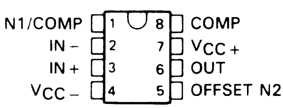
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion 0.003% Typ
- Low Noise . . . Vn = 18 nV/√Hz Typ
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL070, TL070A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- Common mode input voltage range includes Vcc+

description

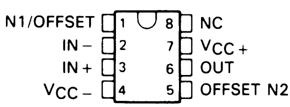
The JFET-input operational amplifiers on the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

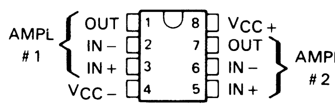
TL070, TL070A
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



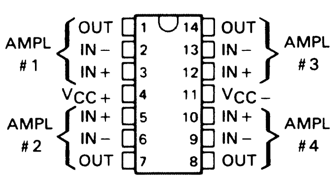
TL071, TL071A, TL071B
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



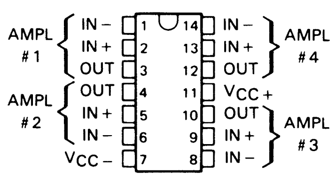
TL072, TL072A, TL072B
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL074, TL074A, TL074B
D, J, OR N DUAL-IN-LINE
OR W FLAT PACKAGE
(TOP VIEW)

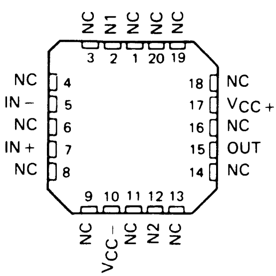


TL075
N DUAL-IN-LINE PACKAGE
(TOP VIEW)

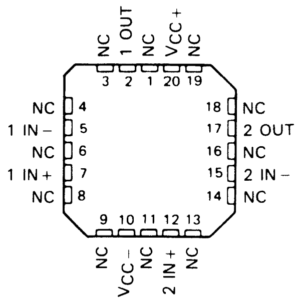


NC—No internal connection

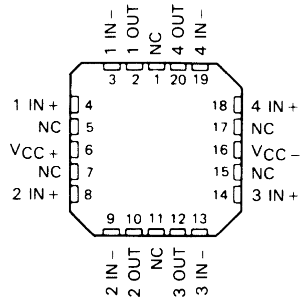
TL071
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



TL072
FK CHIP-CARRIER PACKAGE
(TOP VIEW)

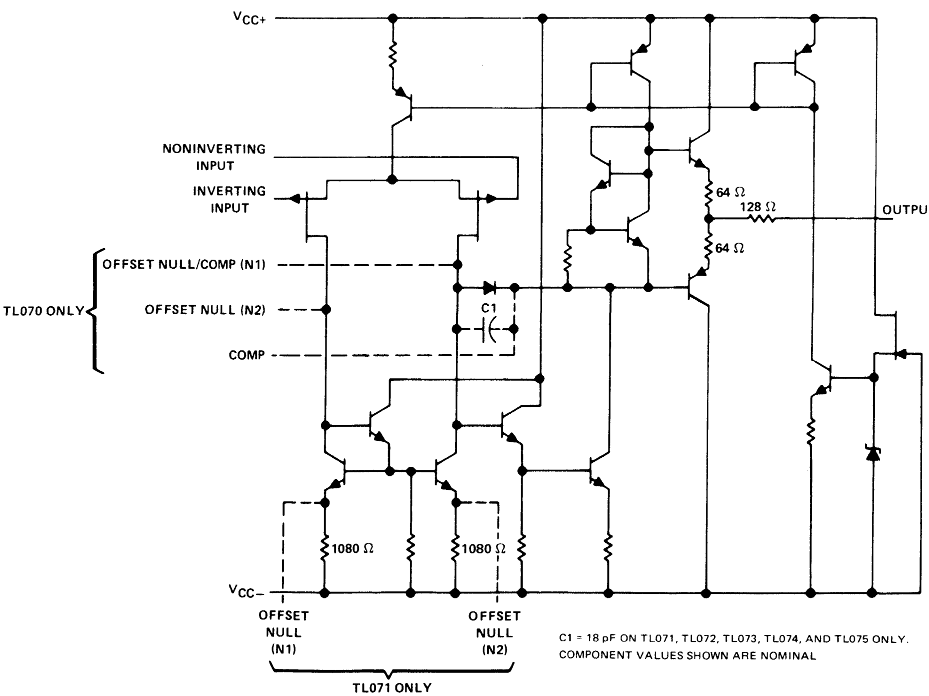


TL074
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



NC — No internal connection

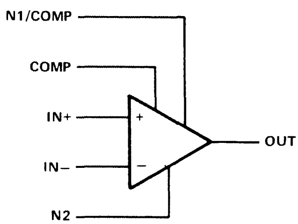
schematic (each amplifier)



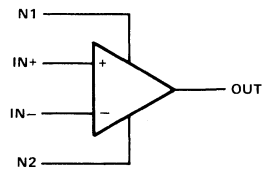
C1 = 18 pF ON TL071, TL072, TL073, TL074, AND TL075 ONLY.
COMPONENT VALUES SHOWN ARE NOMINAL

symbols

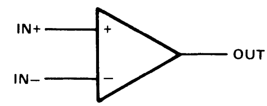
TL070



TL071



TL072 (EACH AMPLIFIER)
TL074 (EACH AMPLIFIER)



DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES					
	TL070	TL071	TL072	TL074	TL075
TL07_M	*	FK, JG	FK, JG	FK, J, W	*
TL07_I	D, JG, P	D, JG, P	D, JG, P	D, J, N	*
TL07_C	D, JG, P	D, JG, P	D, JG, P	D, J, N	N
TL07_AC	D, JG, P	D, JG, P	D, JG, P	D, J, N	*
TL07_BC	*	D, JG, P	D, JG, P	D, J, N	*

*These combinations are not defined by this data sheet.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL07_M	TL07_I	TL07_C TL07_AC TL07_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		680	680	680	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, FK, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG packages, TL07_M chips are alloy-mounted; TL07_I, TL07_C, TL07_AC, and TL07_BC chips are glass mounted.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL071M, TL072M MIN	TL071M, TL072M TYP	TL071M, TL072M MAX	TL074M MIN	TL074M TYP	TL074M MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	9	mV
			T_A = −55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55° to 125°C			10			10		μV/°C
I_{IO}	Input offset current‡*	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = −55°C to 125°C			20			20	nA
I_{IB}	Input bias current‡*	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = −55°C to 125°C			50			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	±15 −12		±11	±15 −12		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C,	R_L = 10 kΩ	±12	±13.5		±12	±13.5		V
		T_A = −55°C to 125°C	R_L ≥ 10 kΩ	±12			±12			
			R_L ≥ 2 kΩ	±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, T_A = 25°C	R_L ≥ 2 kΩ,	35	200		35	200		V/mV
		V_O = ±10 V, T_A = −55°C to 125°C	R_L ≥ 2 kΩ,	15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	V_O = 0,		1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100,	T_A = 25°C		120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.
*For M suffix devices these parameters are guaranteed but not tested.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITONS†		TL070I TL071I TL072I TL074I			TL070C TL071C TL072C TL074C TL075C			TL070AC TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	10		3	6		2	3	mV
			T_A = full range			8			13			7.5			5	mV
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = full range			10			10			10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	100		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	V_O = 0	T_A = 25°C		30	200		30	200		30	200		30	200	pA
			T_A = full range			20			7			7			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	+15 −12		±11	+15 −12		±11	+15 −12		±11	+15 −12		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C,	R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		T_A = full range	R_L = ≥ 10 kΩ	±12			±12			±12			±12			V
			R_L ≥ 2 kΩ	±10	±12		±10	±12		±10	±12		±10	±12		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, T_A = 25°C	R_L ≥ 2 kΩ,	50	200		25	200		50	200		50	200		V/mV
		V_O = ±10 V, T_A = full range	R_L ≥ 2 kΩ,	25			15			25			25			V/mV
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		70	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		70	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	V_O = 0,		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100,	T_A = 25°C		120			120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 25°C to 85°C for TL07_I and 0°C to 70°C for TL07_C, TL07_AC, and TL07_BC.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

Operational Amplifiers 3

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07_M MIN	TL07_M TYP	TL07_M MAX	ALL OTHERS MIN	ALL OTHERS TYP	ALL OTHERS MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	8	13		8	13		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,		0.1			0.1		μs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		10			10		%
V_n	Equivalent input noise voltage	$R_S = 100$ Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current		f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)} = 10$ V, $R_L \geq 2$ kΩ,	$R_S \leq 1$ kΩ, f = 1 kHz		0.003			0.003		%

PARAMETER MEASUREMENT INFORMATION

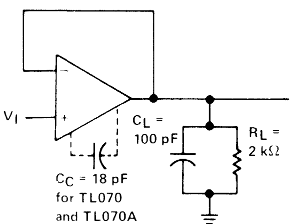


FIGURE 1—UNITY-GAIN AMPLIFIER

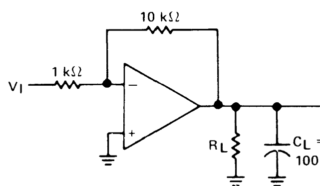


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

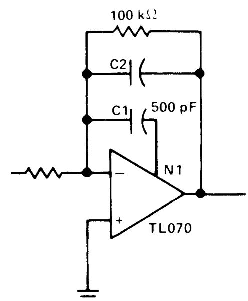


FIGURE 3—FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

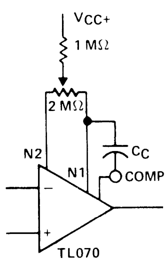


FIGURE 4

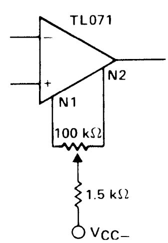


FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

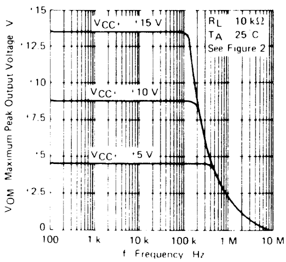


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

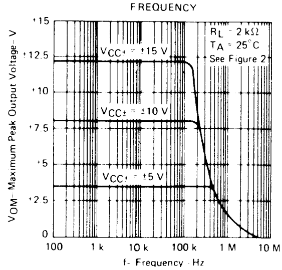


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

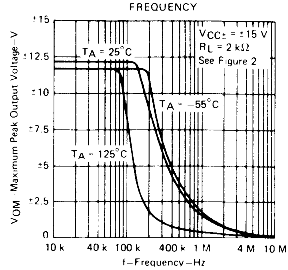


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

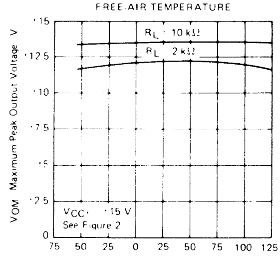


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

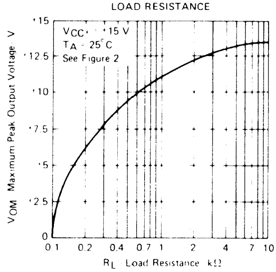


FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

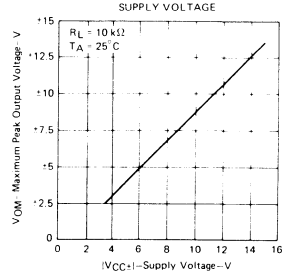


FIGURE 11

TOTAL POWER DISSIPATED vs FREE-AIR TEMPERATURE

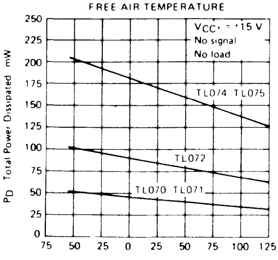


FIGURE 12

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

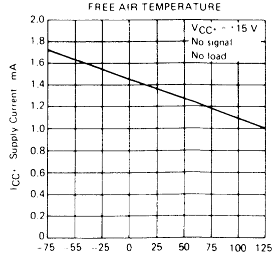


FIGURE 13

SUPPLY CURRENT vs SUPPLY VOLTAGE

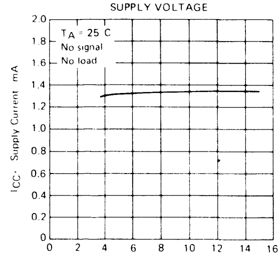


FIGURE 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 18-pF compensation capacitor is used with TL070 and TL070A.

3 Operational Amplifiers

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

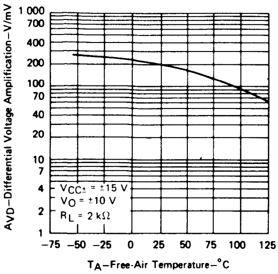


FIGURE 15

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT vs FREQUENCY

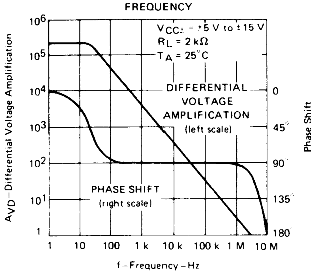


FIGURE 16

TL070 DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY WITH FEED FORWARD COMPENSATION

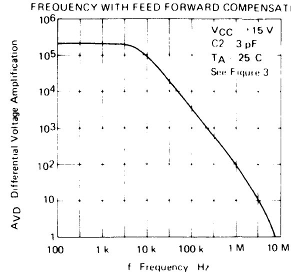


FIGURE 17

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

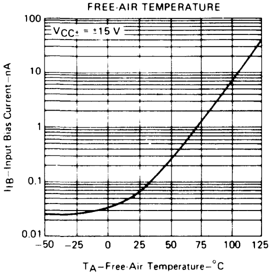


FIGURE 18

NORMALIZED UNITY-GAIN BANDWIDTH and PHASE SHIFT vs FREE-AIR TEMPERATURE

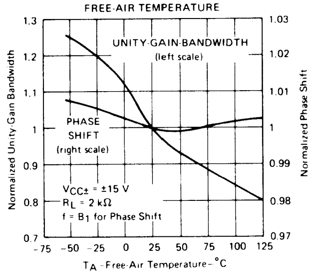


FIGURE 19

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

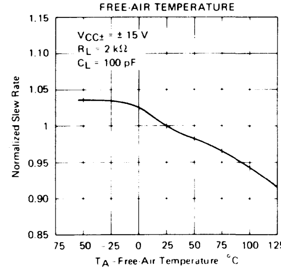


FIGURE 20

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

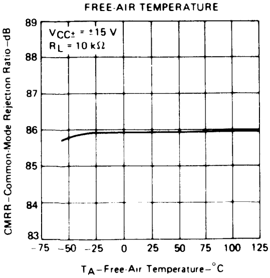


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

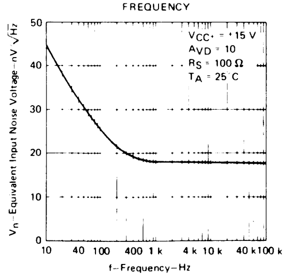


FIGURE 22

TOTAL HARMONIC DISTORTION vs FREQUENCY

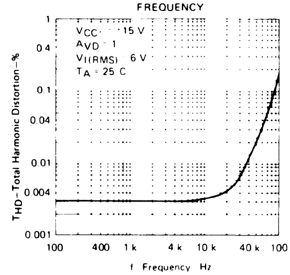


FIGURE 23

† Data at high and low temperatures are applicable only with the rated operating free-air temperature ranges of the vaious devices. A 18-pF compensation capacitor is used with TL070 and TL070A.

TYPICAL CHARACTERISTICS

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

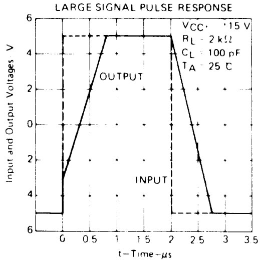


FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

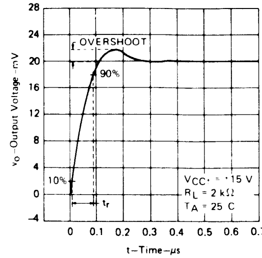


FIGURE 25

TYPICAL APPLICATION DATA

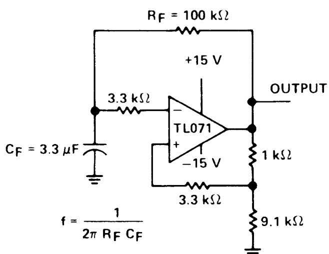


FIGURE 26–0.5-Hz SQUARE-WAVE OSCILLATOR

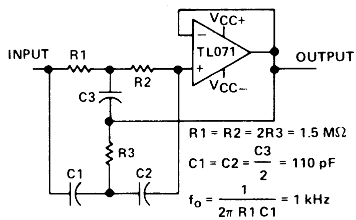
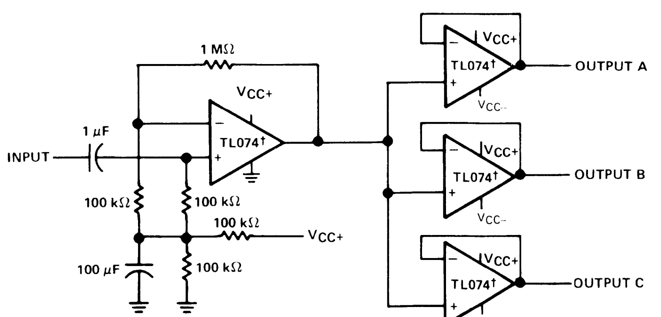


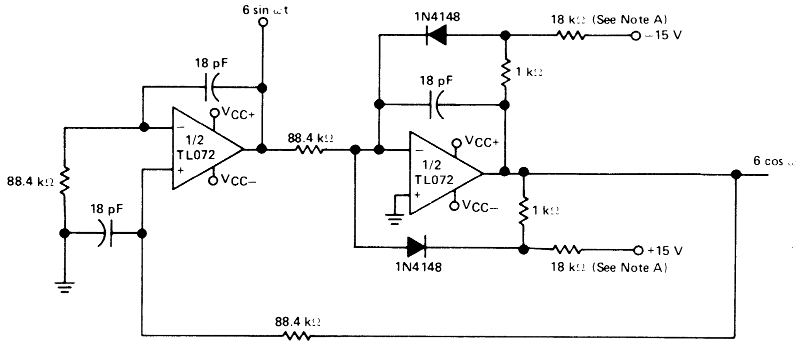
FIGURE 27–HIGH-Q NOTCH FILTER



† or TL075

FIGURE 28–AUDIO DISTRIBUTION AMPLIFIER

TYPICAL APPLICATION DATA



Note A: These resistor values may be adjusted for a symmetrical output.

FIGURE 29—100-KHz QUADRATURE OSCILLATOR

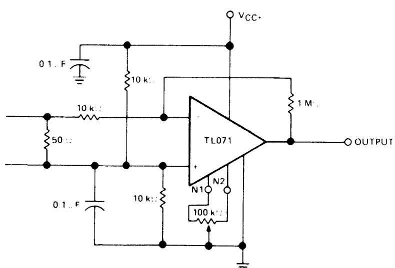


FIGURE 30—AC AMPLIFIER

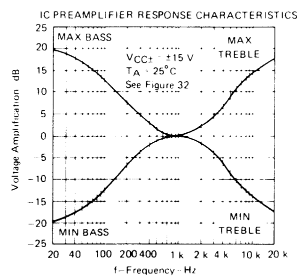


FIGURE 31

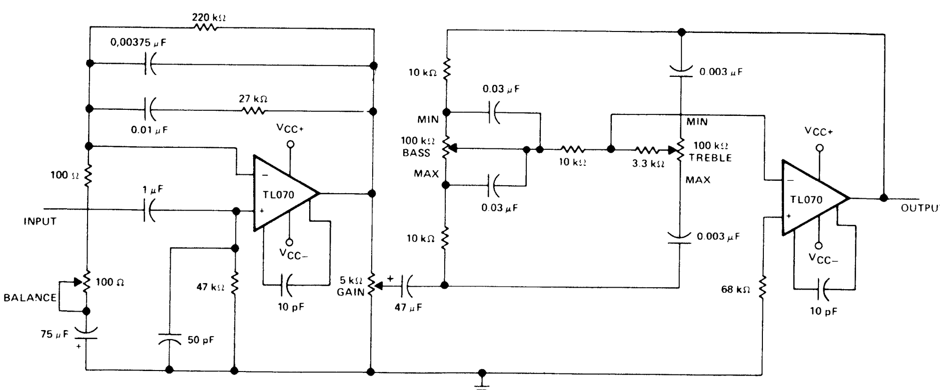


FIGURE 32—IC PREAMPLIFIER

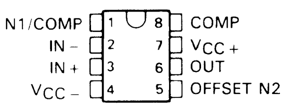
TYPES TL080 THRU TL085, TL080A THRU TL084A TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

D2297, FEBRUARY 1977—REVISED SEPTEMBER 1983

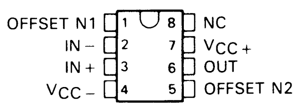
24 DEVICES COVER MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

- Low-Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% TYP
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- **Common mode input voltage range includes Vcc+**

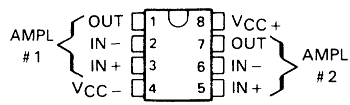
TL080, TL080A
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



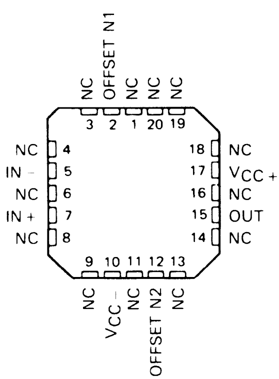
TL081, TL081A, TL081B
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



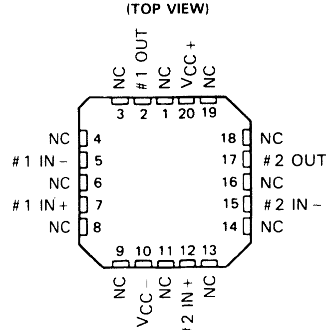
TL082, TL082A, TL082B
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL081M . . . FK
CHIP CARRIER PACKAGE
(TOP VIEW)



TL082M . . . FK
CHIP CARRIER PACKAGE
(TOP VIEW)



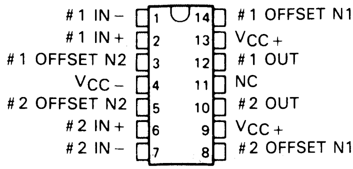
NC No internal connection

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

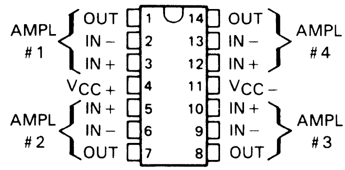
	TL080	TL081	TL082	TL083	TL084	TL085
TL08_M	JG	FK, JG	FK, JG	FK, J	FK, J, W	•
TL08_I	JG, P	JG, P	JG, P	J, N	J, N	•
TL08_C	JG, P	JG, P	JG, P, D	J, N	J, N, D	N
TL08_AC	JG, P	JG, P	JG, P, D	J, N	J, N, D	•
TL08_BC	•	JG, P	JG, P	•	J, N	•

•These combinations are not defined by this data sheet.

TL083, TL083A
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

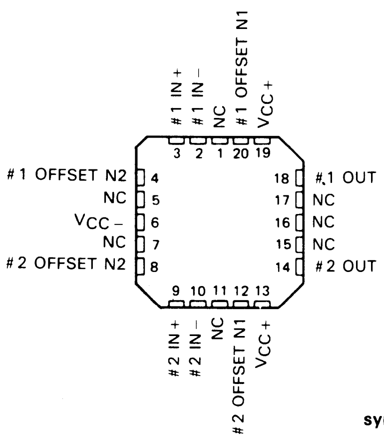


TL084, TL084A, TL084B
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

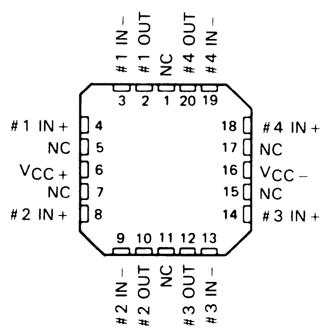


Pins 9 and 13 are internally interconnected

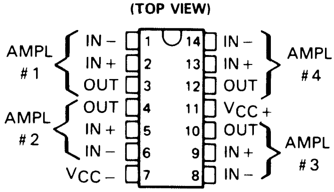
TL083M . . . FK
CHIP CARRIER PACKAGE
(TOP VIEW)



TL084M . . . FK
CHIP CARRIER PACKAGE
(TOP VIEW)



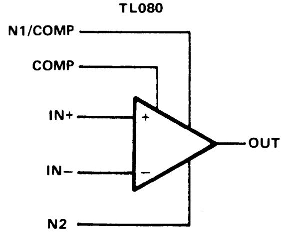
TL085
N DUAL-IN-LINE PACKAGE
(TOP VIEW)



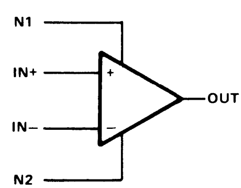
NC—No internal connection

symbols

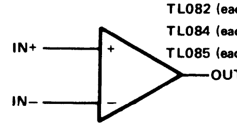
TL080



TL081
TL083 (each amplifier)



TL082 (each amplifier)
TL084 (each amplifier)
TL085 (each amplifier)

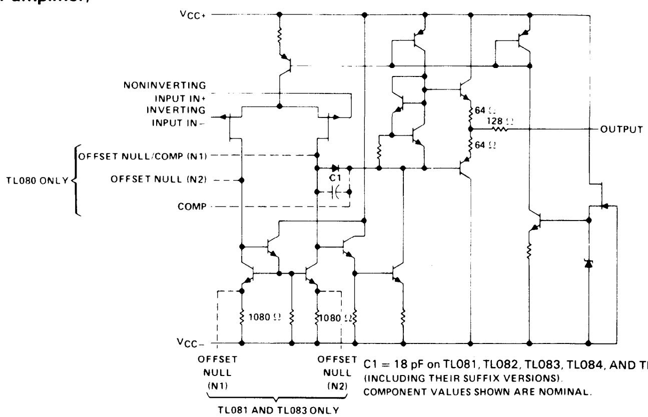


description

The TL08_ JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08_ family.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

schematic (each amplifier)



C1 = 18 pF on TL081, TL082, TL083, TL084, AND TL085 ONLY (INCLUDING THEIR SUFFIX VERSIONS).
COMPONENT VALUES SHOWN ARE NOMINAL.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_M	TL08_I	TL08_C TL08_AC TL08_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		680	680	680	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, J, JG, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the J and JG packages, TL08_M chips are alloy-mounted; TL08_I, TL08_C, TL08_AC, and TL08_BC chips are glass-mounted.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL080M, TL081M TL082M, TL083M MIN	TYP	MAX	TL084M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	9	mV
			$T_A = -55°C$ to $125°C$			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, $T_A = -55°C$ to $125°C$			10			10		μV/°C
I_{IO}	Input offset current‡*	$V_O = 0$	$T_A = 25°C$		5	100		5	100	pA
			$T_A = -55°C$ to $125°C$			20			20	nA
I_{IB}	Input bias current‡*	$V_O = 0$	$T_A = 25°C$		30	200		30	200	pA
			$T_A = -55°C$ to $125°C$			50			50	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	±15 −12		±11	±15 −12		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		V
		$T_A = -55°C$ to $125°C$	$R_L \geq 10\ k\Omega$	±12			±12			
			$R_L \geq 2\ k\Omega$	±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $T_A = 25°C$	$R_L \geq 2\ k\Omega$,	25	200		25	200		V/mV
		$V_O = \pm 10$ V, $T_A = -55°C$ to $125°C$	$R_L \geq 2\ k\Omega$,	15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$,	$T_A = 25°C$		120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.
*For M suffix devices these parameters are guaranteed but not tested.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

	PARAMETER	TEST CONDITONS†		TL080I TL081I TL082I TL083I TL084I			TL080C TL081C TL082C TL083C TL084C TL085C			TL080AC TL081AC TL082AC TL083AC TL084AC			TL081BC TL082BC TL084BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	15		3	6		2	3	mV
			T_A = full range			9			20			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$, T_A = full range			10			10			10			10		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	200		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	200		30	400		30	200		30	200	pA
			T_A = full range			20			10			7			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	+15 −12		±11	+15 −12		±11	+15 −12		±11	+15 −12		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		T_A = full range	$R_L \geq 10\ k\Omega$	±12			±12			±12			±12			
			$R_L \geq 2\ k\Omega$	±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$, $T_A = 25°C$		50	200		25	200		50	200		50	200		V/mV
		$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$, T_A = full range		25			15			25			25			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	86		70	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $V_O = 0$, $R_S = 50\ \Omega$, $T_A = 25°C$		80	86		70	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, $V_O = 0$, $T_A = 25°C$			1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25°C$			120			120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 25°C to 85°C for TL08_I and 0°C to 70°C for TL08_C, TL08_AC, and TL08_BC.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	8	13		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		0.1		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 100 Ω,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)}$ = 10 V, $R_L \geq$ 2 kΩ,	$R_S \leq$ 1 kΩ, f = 1 kHz		0.003%		

PARAMETER MEASUREMENT INFORMATION

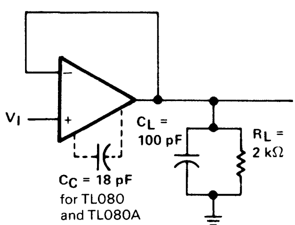


FIGURE 1—UNITY-GAIN AMPLIFIER

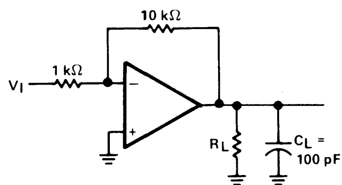


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

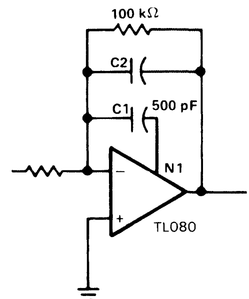


FIGURE 3—FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

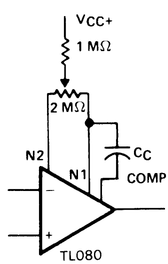


FIGURE 4

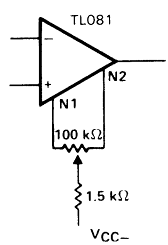


FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

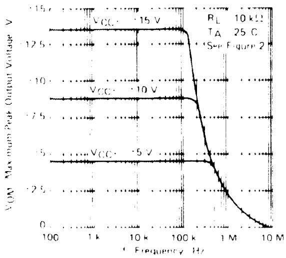


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

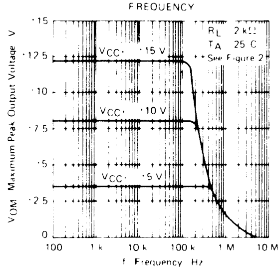


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

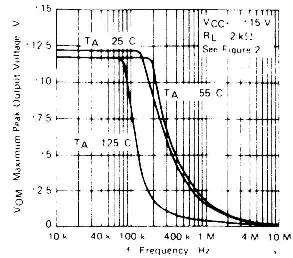


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

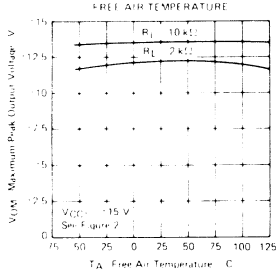


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

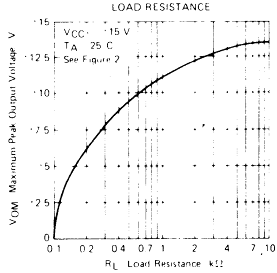


FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

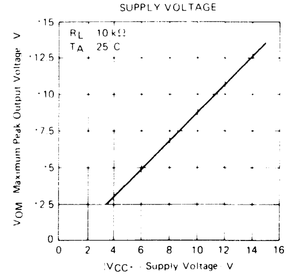


FIGURE 11

3

Operational Amplifiers

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

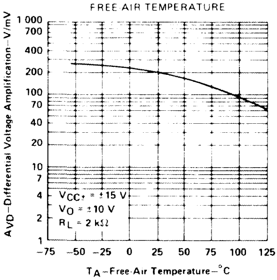


FIGURE 12

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT vs FREQUENCY

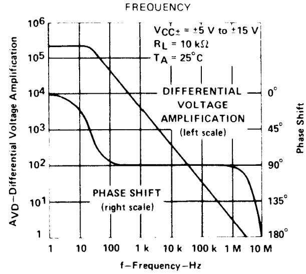


FIGURE 13

TL080, TL080A DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY WITH FEED-FORWARD COMPENSATION

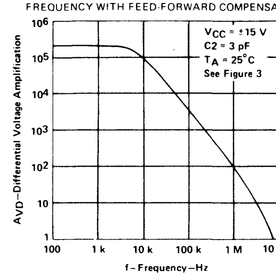


FIGURE 14

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATED vs FREE-AIR TEMPERATURE

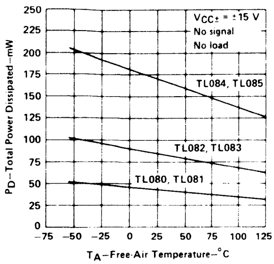


FIGURE 15

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

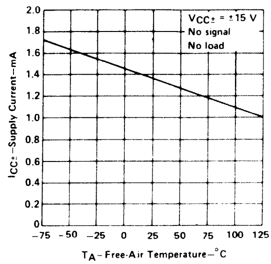


FIGURE 16

SUPPLY CURRENT vs SUPPLY VOLTAGE

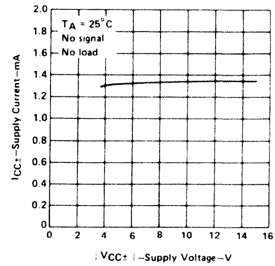


FIGURE 17

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

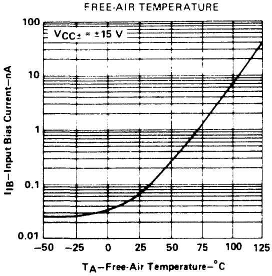


FIGURE 18

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

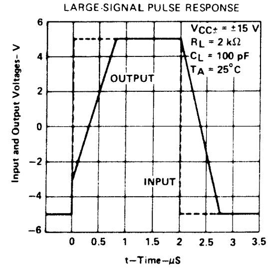


FIGURE 19

OUTPUT VOLTAGE vs ELAPSED TIME

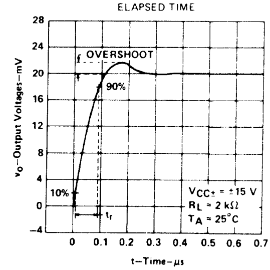


FIGURE 20

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

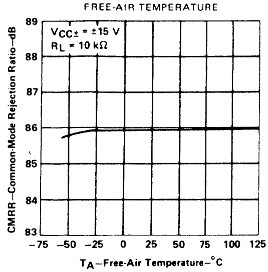


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

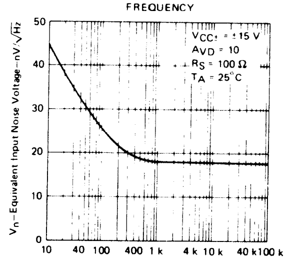


FIGURE 22

TOTAL HARMONIC DISTORTION vs FREQUENCY

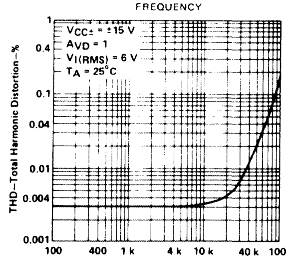


FIGURE 23

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

TYPICAL APPLICATION DATA

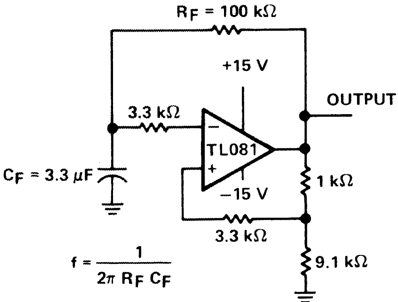


FIGURE 24—0.5-Hz SQUARE-WAVE OSCILLATOR

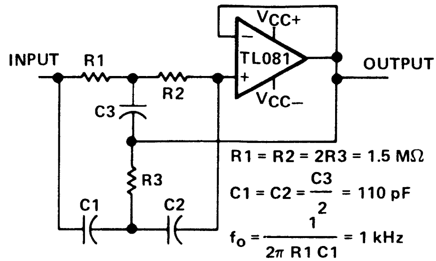
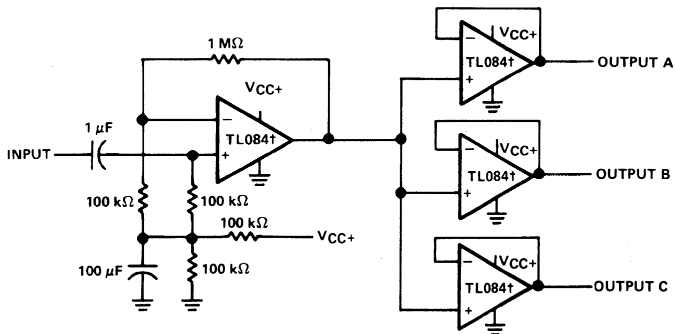
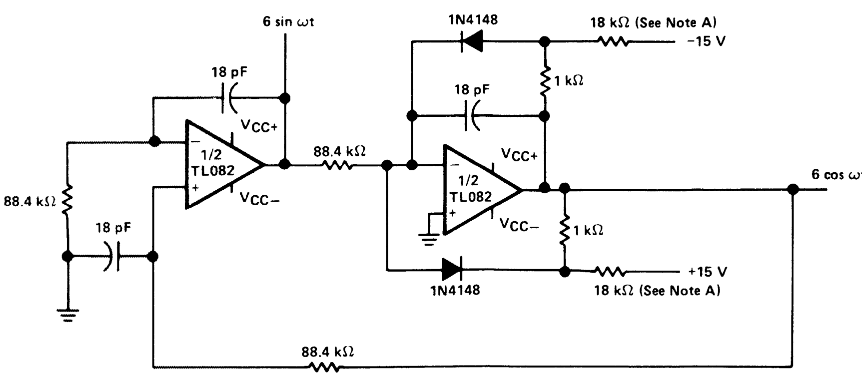


FIGURE 25—HIGH-Q NOTCH FILTER



† or TL085

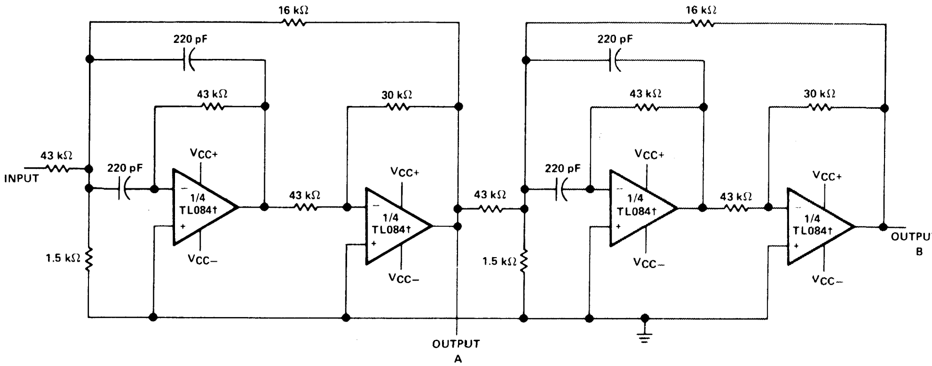
FIGURE 26—AUDIO DISTRIBUTION AMPLIFIER



NOTE A: These resistor values may be adjusted for a symmetrical output.

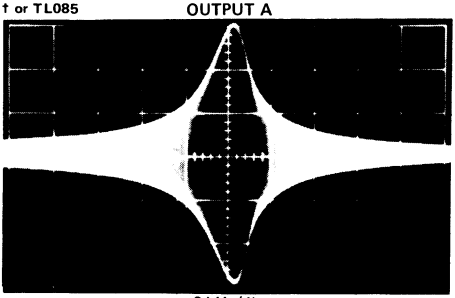
FIGURE 27—100-kHz QUADRATURE OSCILLATOR

TYPICAL APPLICATION DATA



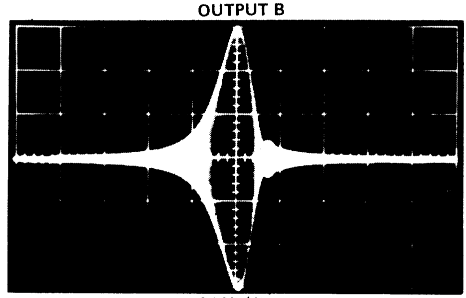
† or TL085

OUTPUT A



2 kHz/div
SECOND-ORDER BANDPASS FILTER
f_o = 100 kHz, Q = 30, GAIN = 4

OUTPUT B



2 kHz/div
CASCADED BANDPASS FILTER
f_o = 100 kHz, Q = 69, GAIN = 16

FIGURE 28—POSITIVE-FEEDBACK BANDPASS FILTER

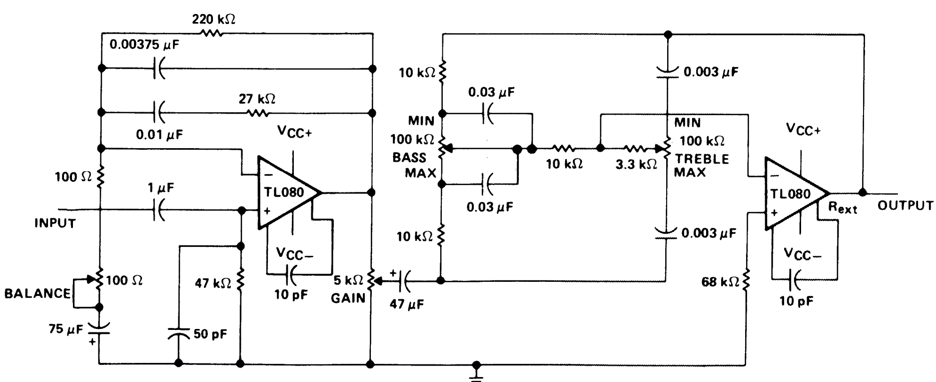


FIGURE 29—IC PREAMPLIFIER

TYPES TL087, TL088, TL287, TL288
JFET-INPUT OPERATIONAL AMPLIFIERS

D2484, MARCH 1979 – REVISED AUGUST 1983

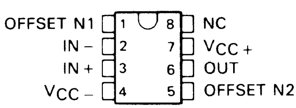
- **Low Input Offset Voltage . . . 0.5 mV Max**
- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Common mode input voltage range includes Vcc+**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Low Total Harmonic Distortion . . . 0.003% Typ**

description

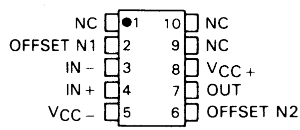
These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset current, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

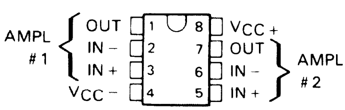
TL087, TL088
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



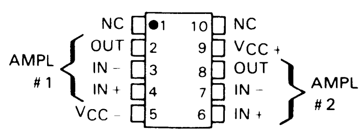
TL088M
U FLAT PACKAGE
(TOP VIEW)



TL287, TL288
D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

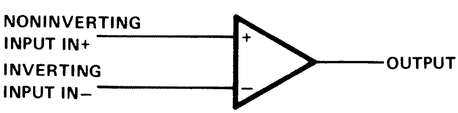


TL288M
U FLAT PACKAGE
(TOP VIEW)



NC – No internal connection

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL088M TL288M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	JG or P package	680	680	680	mW
	U package	675			mW
	D package		725	725	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG package, TL088M and TL288M chips are alloy-mounted; TL087I, TL088I, TL287I, TL288I, TL087C, TL088C, TL287C, and TL288C chips are glass-mounted.
6. The offset voltage null circuit for the TL087 or the TL088 is the same as the TL081. See figure 5 page 3-126.

electrical characteristics, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS†		TL088M TL288M MIN	TL088M TL288M TYP	TL088M TL288M MAX	TL087I TL088I TL287I TL288I MIN	TL087I TL088I TL287I TL288I TYP	TL087I TL088I TL287I TL288I MAX	TL087C TL088C TL287C TL288C MIN	TL087C TL088C TL287C TL288C TYP	TL087C TL088C TL287C TL288C MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$, $V_O = 0$, $T_A = 25°C$	TL087, TL287					0.1	0.5		0.1	0.5	mV
			TL088, TL288		0.1	3		0.1	1		0.1	1	
		$R_S = 50\ \Omega$, $V_O = 0$, T_A = full range	TL087, TL287						2			1.5	
			TL088, TL288			6			3			2.5	
α_{VIO}	Temperature coefficient of input offset voltage	$R_S = 50\ \Omega$,	T_A = full range		10			10			10		μV/°C
I_{IO}	Input offset current	$T_A = 25°C$			5	100		5	100		5	100	pA
		T_A = full range				25			3			2	nA
I_{IB}	Input bias current‡	$T_A = 25°C$			30	400		30	200		30	200	pA
		T_A = full range				100			20			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		$V_{CC-}+4$ to $V_{CC+}-4$			$V_{CC-}+4$ to $V_{CC+}-4$			$V_{CC-}+4$ to $V_{CC+}-4$			V
V_{OPP}	Maximum-peak-to-peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	24	27		24	27		24	27		V
		T_A = full range	$R_L \geq 10\ k\Omega$	24			24			24			
			$R_L \geq 2\ k\Omega$	20			20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $T_A = 25°C$	$V_O = \pm 10$ V,	50	200		50	200		50	200		V/mV
		$R_L \geq 2\ k\Omega$, T_A = full range	$V_O = \pm 10$ V,	25			25			25			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$, $V_{IC} = V_{ICR}$ min,	$V_O = 0$, $T_A = 25°C$	80	95		80	95		80	95		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$R_S = 50\ \Omega$, $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25°C$	$V_O = 0$ V,	80	95		80	95		80	95		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		1.4	2.8		1.4	2.8		1.4	2.8	mA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for TL_88M; −25°C to 85°C for TL_8_I; and 0°C to 70°C for TL_8_C.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics $V_{CC} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL080M TL288M MIN	TYP	MAX	TL087I TL087C TL287I TL287C TL088I TL088C TL288I TL288C MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, $A_{VD} = 1$				8	13		V/μs
t_r	Rise time	$V_I = 20$ mV,	$R_L = 2$ kΩ,					0.1		μs
	Overshoot factor	$C_L = 100$ pF,	$A_{VD} = 1$					10%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω,	f = 1 kHz					18		nV/√Hz

TYPICAL CHARACTERISTICS†

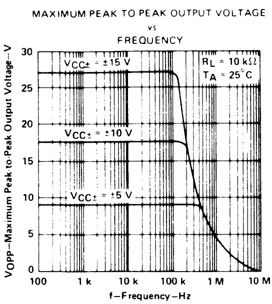


FIGURE 1

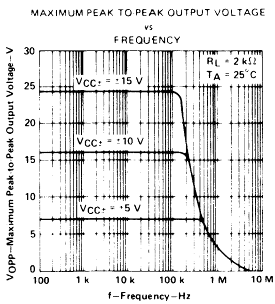


FIGURE 2

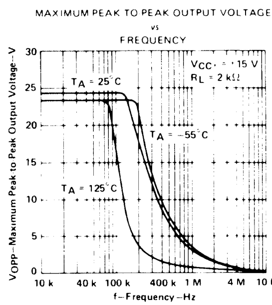


FIGURE 3

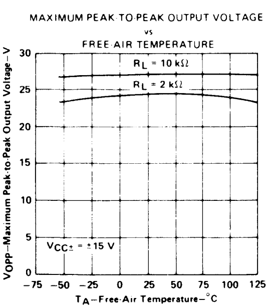


FIGURE 4

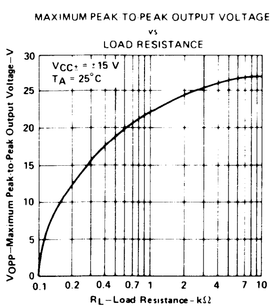


FIGURE 5

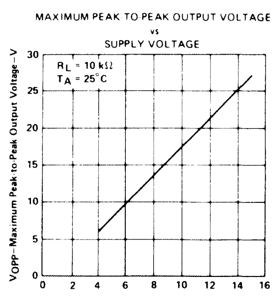


FIGURE 6

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

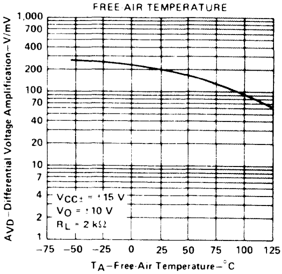


FIGURE 7

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

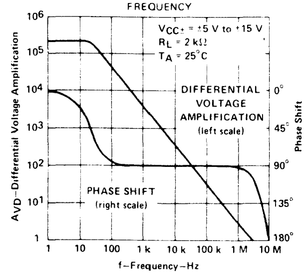


FIGURE 8

NORMALIZED UNITY-GAIN BANDWIDTH
and PHASE SHIFT
vs
TEMPERATURE

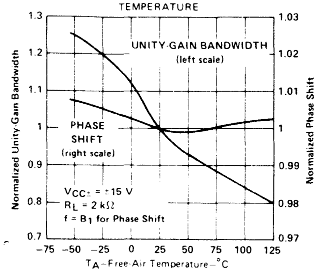


FIGURE 9

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

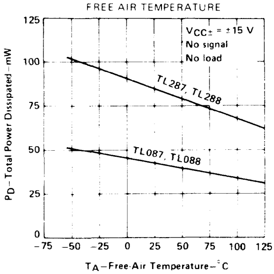


FIGURE 10

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

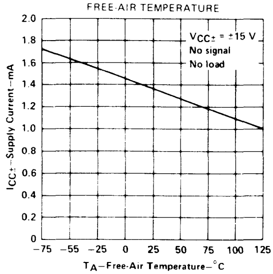


FIGURE 11

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

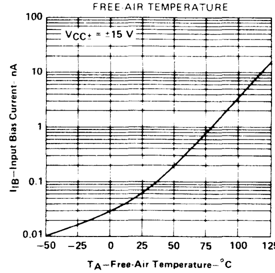


FIGURE 12

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

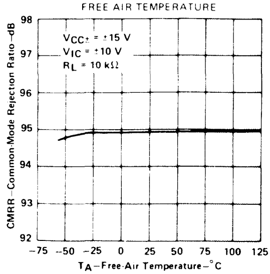


FIGURE 13

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

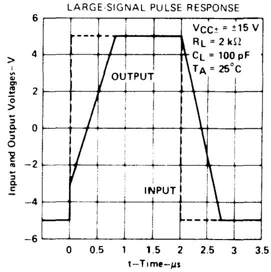


FIGURE 14

OUTPUT VOLTAGE
vs
ELAPSED TIME

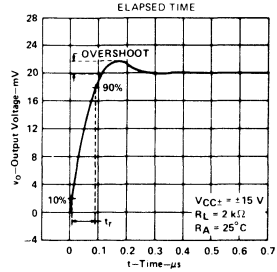


FIGURE 15

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NORMALIZED SLEW RATE
vs
TEMPERATURE

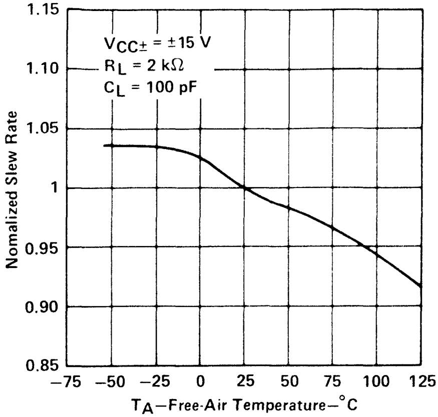


FIGURE 16

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

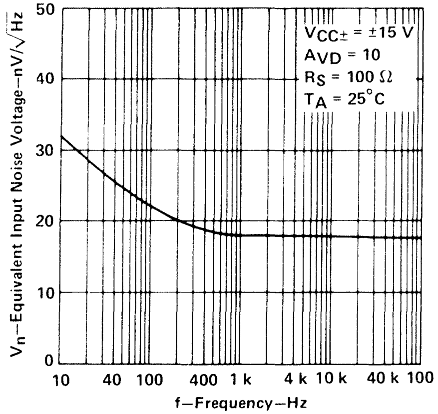


FIGURE 17

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

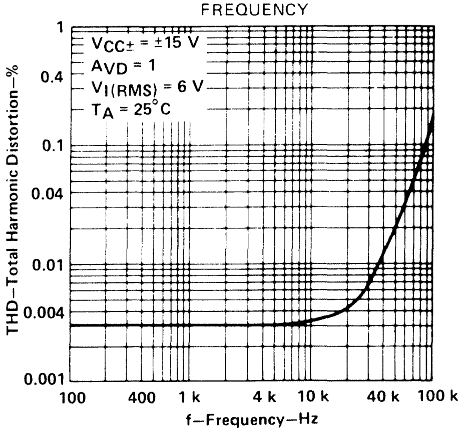


FIGURE 18

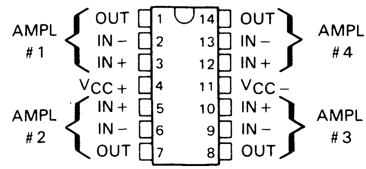
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPE TL136C
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

D2604, NOVEMBER 1981 – REVISED AUGUST 1983

- Continuous-Short Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Unity-Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers

D, J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



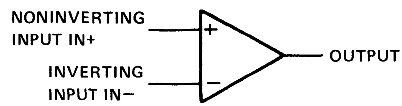
description

The TL136C is a quad high-performance operational amplifier with each amplifier electrically similar to uA741 except that offset null capability is not provided.

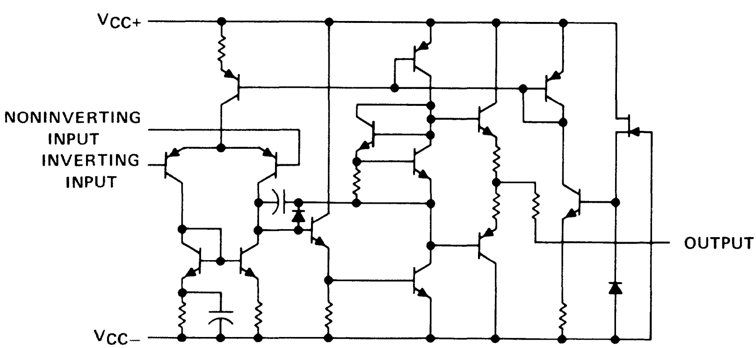
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The TL136C is characterized for operation from 0 °C to 70 °C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	18 V
Supply voltage V_{CC-} (see Note 1)	−18 V
Differential input voltage (see Note 2)	±30 V
Input voltage (any input, see Notes 1 and 3)	±15 V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N package	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the J package, the chips are glass-mounted.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		0.5	6	mV
			0°C to 70°C			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	200	nA
			0°C to 70°C			300	
I_{IB}	Input bias current	V_O = 0	25°C		40	500	nA
			0°C to 70°C			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		V
		R_L = 2 kΩ	25°C	20	26		
		R_L ≥ 2 kΩ	0°C to 70°C	20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	20	300		V/mV
			0°C to 70°C	15			
B_1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C	0.3	5		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±9 V to ±15 V, R_S = 50 Ω	25°C		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, R_S = 100 Ω, f = 1 kHz, BW = 1 Hz	25°C		7.5		nV/√Hz
I_{CC}	Supply current (All four amplifiers)	No load, V_O = 0 V	25°C		5	11.3	mA
			0°C		6	13.7	
			70°C		4.5	11.3	
P_D	Total power dissipation (All four amplifiers)	No load, V_O = 0 V	25°C		150	340	mW
			0°C		180	400	
			70°C		135	300	
$V_{o1}V_{o2}$	Crosstalk attenuation Open loop	R_S = 1 kΩ, f = 10 kHz	25°C		105		dB
	Crosstalk attenuation A_{VD}		25°C		105		

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		0.13		μs
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF		2.0		V/μs

3

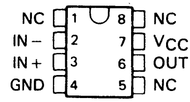
Operational Amplifiers

TYPES TL321M, TL321I, TL321C OPERATIONAL AMPLIFIERS

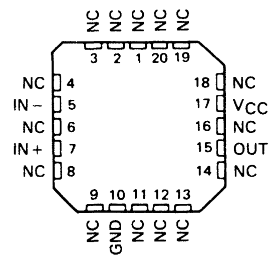
D2343, APRIL 1977—REVISED AUGUST 1983

- Wide Range of Supply Voltages Single Supply . . . 3 V to 30 V or Dual Supplies
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground
- Low Input Bias and Offset Parameters
  Input Offset Voltage . . . 2 mV TYP
  Input Offset Current . . . 3 nA Typ (TL321M)
  Input bias Current . . . 45 nA Typ
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V
- Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ
- Internal Frequency Compensation

TL321M . . . JG
TL321I, TL321C . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

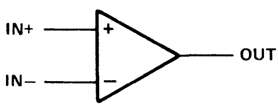


TL321M . . . FK
CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



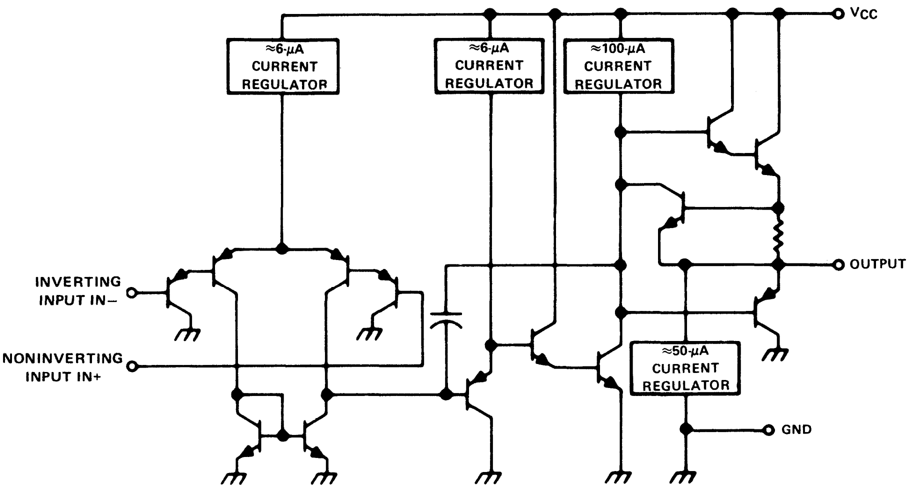
description

The TL321 is a high-gain, frequency-compensated operational amplifier that was designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 30 volts and Pin 7 is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the TL321 can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-volt supplies.

The TL321M is characterized for operation over the full military temperature range of −55 °C to 125 °C. The TL321I is characterized for operation from −25 °C to 85 °C. The TL321C is characterized for operation from 0 °C to 70 °C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	32 V
Differential input voltage (see Note 2)	±32 V
Input voltage range (either input)	−0.3 V to 32 V
Duration of output short-circuit to ground at (or below) 25°C free-air temperature ($V_{CC} \leq 15$ V) (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	680 mW
Operating free-air temperature range: TL321M	−55°C to 125°C
TL321I	−25°C to 85°C
TL321C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK, or JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG package, TL321M chips are alloy-mounted; TL321I and TL321C chips are glass-mounted.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL321M, TL321I MIN	TL321M, TL321I TYP	TL321M, TL321I MAX	TL321C MIN	TL321C TYP	TL321C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_S = 50 kΩ	25°C		2	5		2	7	mV
			Full range			7			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	30		5	50	nA
			Full range			100			150	
I_{IB}	Input bias current	V_O = 1.4 V,	25°C		−45	−150		−45	−250	nA
			Full range			−300			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			V
		V_{CC} = 30 V, $R_L \geq$ 10 kΩ	Full range	27	28		27	28		
		$R_L \geq$ 2 kΩ	25°C	3.5			3.5			
V_{OL}	Low-level output voltage	$R_L \leq$ 10 kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \geq$ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, R_S = 50 Ω	25°C	70	85		65	85		dB
k_{SVR}	Supply voltage rejection ratio($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V, R_S = 50 Ω	25°C	65	100		65	100		dB
I_O	Output current, Source	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−25	−40		−20	−40		mA
			Full range	−10	−20		−10	−20		
	Output current, Sink	V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
			Full range	5	8		5	8		
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	50		12	50		μA
I_{CC}	Supply current	No load V_O = 15 V, V_{CC} = 30 V	Full range			2			2	mA
		No load V_O = 2.5 V, V_{CC} = 5 V	Full range		0.4	1			1	

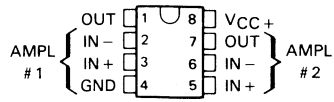
†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for TL321M, −25°C to 85°C for TL321I, and 0°C to 70°C for TL321C.

TYPES TL322M, TL322I, TL322C DUAL LOW-POWER OPERATIONAL AMPLIFIERS

D2567, OCTOBER 1979—REVISED SEPTEMBER 1983

- **Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**

TL322M . . . JG PACKAGE
TL322I, TL322C . . . D, JG, OR P PACKAGE
(TOP VIEW)

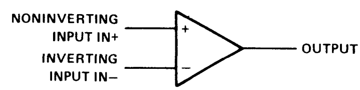


description

The TL322M, TL322I, and the TL322C are dual operational amplifiers similar in performance to the MC3403. They are designed to operate from a single supply over a range of voltages from 3 volts to 36 volts. Operation from split supplies is also possible provided the difference between the two supplies is 3 volts to 36 volts. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC-} 1.5 V. Quiescent supply currents per amplifier are typically less than one-half those of the uA741.

The TL322M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL322I is characterized for operation from −40°C to 85°C. The TL322C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL322M	TL322I	TL322C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}		36	36	36	V
Differential input voltage (see Note 2)		±36	±36	±36	V
Input voltage (see Notes 1 and 3)		±18	±18	±18	V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 4)		680	680	680	mW
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-}.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in Section 2. In the JG package, TL322M chips are alloy mounted and TL322I and TL322C chips are glass mounted.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL322M MIN	TL322M TYP	TL322M MAX	TL322I MIN	TL322I TYP	TL322I MAX	TL322C MIN	TL322C TYP	TL322C MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		2	8		2	8		2	10	mV
			Full range			10			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		10			10			10		µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		30	75		30	75		30	50	nA
			Full range			250			250			200	
α_{IIO}	Temperature coefficient of input offset current	$V_O = 0$	25°C		50			50			50		pA/°C
I_{IB}	Input bias current	$V_O = 0$	25°C		−0.2	−0.5		−0.2	−0.5		−0.2	−0.5	µA
			Full range			−1.15			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 13	V_{CC-} to 13.5		V_{CC-} to 13	V_{CC-} to 13.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		±12	±12.5		±12	±13.5		V
		$R_L = 2\ k\Omega$	25°C	±10	±13		±10	±12		±10	±13		
			Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	25°C		200		20	200		20	200		V/mV
			Full range	25			15			15			
B_{OM}	Maximum-output swing bandwidth	$V_{OPP} = 20$ V, $A_{VD} = 1$, THD ≤ 5%, $R_L = 2\ k\Omega$	25°C		9			9			9		kHz
B_1	Unity-gain bandwidth	$V_O = 50$ mV, $R_L = 10\ k\Omega$	25°C		1			1			1		MHz
ϕ_m	Phase margin	$R_L = 2\ k\Omega$, $C_L = 200$ pF	25°C		60°			60°			60°		
r_i	Input resistance	f = 20 Hz	25°C		1		0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75			75		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 2.5$ V to ±15 V, $R_S = 50\ \Omega$	25°C		30	150		30	150		30	150	µV/V
I_{OS}	Short-circuit output current§	$V_O = 0$	25°C	±10	±30	±45	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	$V_O = 0$, No load	25°C		1.4	2.5		1.4	4		1.4	4	mA

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for T_A is −55°C to 125°C for TL322M; −40°C to 85°C for TL322I, and 0°C to 70°C for TL322C.

‡ The V_{ICR} limits are directly linked volt-for-volt to supply voltage, viz the positive limit is 2 volts less than V_{CC+}.

§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL322M			TL322I			TL322C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω		2	8			8		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V		30	75			75		30	50	nA
I_{IB}	Input bias current			−0.2				−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing§	R_L = 10 kΩ	3.3	3.5		3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	$V_{CC+} - 1.7$			$V_{CC+} - 1.7$			$V_{CC+} - 1.7$			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	V_{CC} = ±2.5 V to ±15 V						150			150	μV/V
I_{CC}	Supply current	V_O = 2.5 V, No load		1.2	2.5		1.2	4		1.2	4	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, f = 1 kHz to 20 kHz		120			120			120		dB

†All characteristics are specified under open-loop conditions.
§Output will swing essentially to ground.

switching characteristics: $V_{CC\pm}$ = ±15 V, A_{VD} = 1, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = 100 pF, See Figure 1		0.6		V/μs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		μs
t_f	Fall time			0.35		μs
	Overshoot factor			20%		
	Crossover distortion	V_{IPP} = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

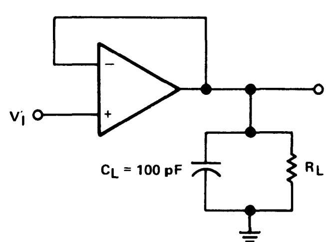


FIGURE 1—UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs TEMPERATURE

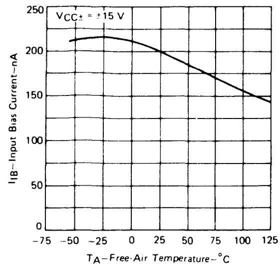


FIGURE 2

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

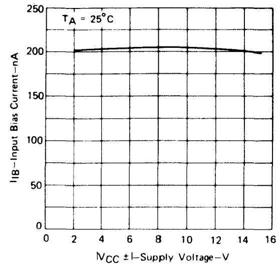


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

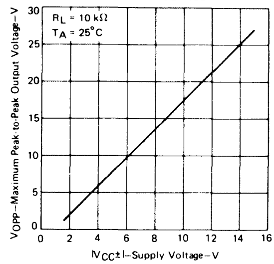


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

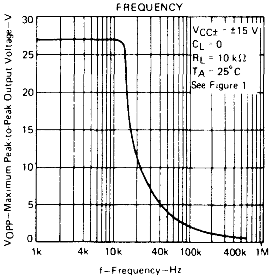


FIGURE 5

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

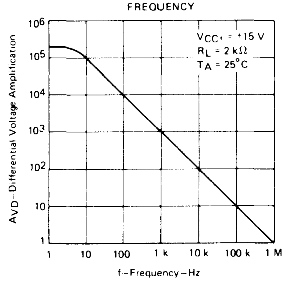


FIGURE 6

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

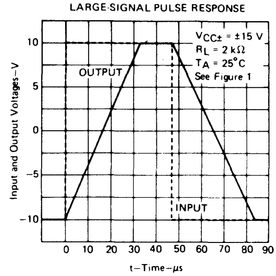
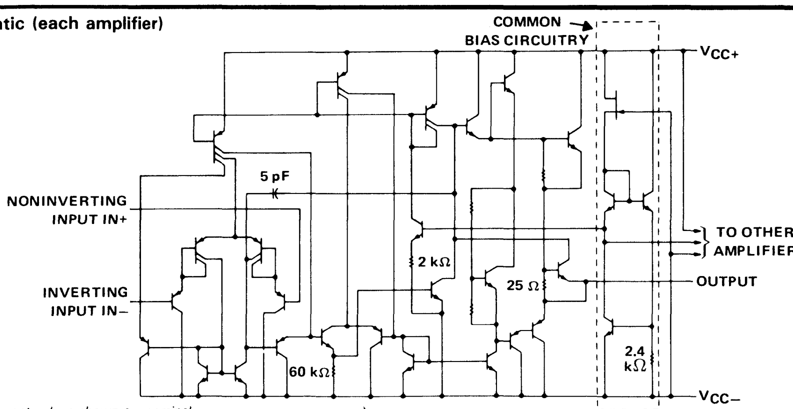


FIGURE 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

schematic (each amplifier)

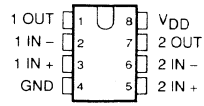


All component values shown are nominal

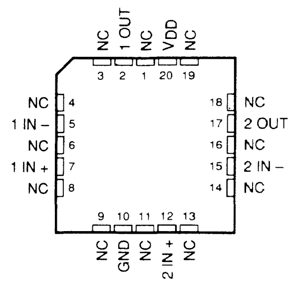
AUGUST 1988

- **Power Dissipation as Low as 10 μW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 450 μV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days**
- **High Impedance LinCMOS Inputs I_{IB} = 600 fA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**

D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



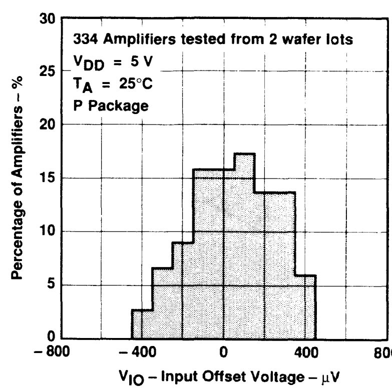
NC – No internal connection

description

The TLC1078 is an ultra-low offset voltage, high gain CMOS operational amplifier. This high performance along with 110 kHz bandwidth and 47 V/ms slew rate is achieved on just 150 μW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1078 is an ideal solution for low voltage battery-operated systems. The 20 mA output drive capability means that the TLC1078 can easily drive small resistive and large capacitive loads when needed, while

DISTRIBUTION OF TLC1078 INPUT OFFSET VOLTAGE



AVAILABLE OPTIONS

T_A	PACKAGE			
	Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	TLC1078CD	TLC1078CP	TLC1078CJG	—
– 40°C to 85°C	TLC1078ID	TLC1078IP	TLC1078IJG	—
– 55°C to 125°C	—	—	TLC1078MJG	TLC1078MFK

NOTE 1: D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC1078CDR).

description (continued)

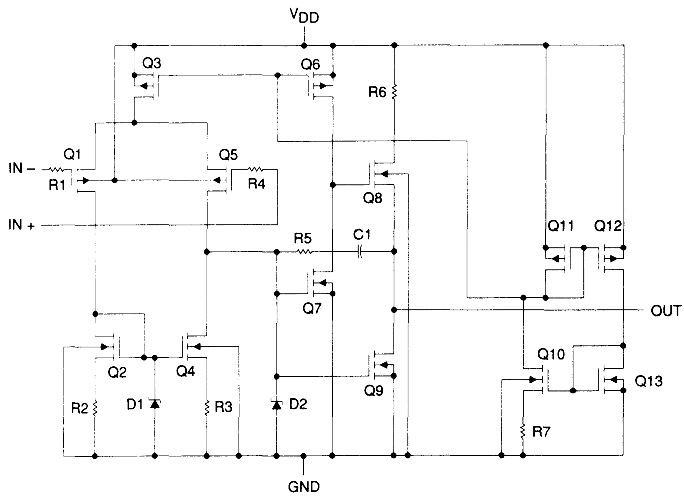
maintaining ultra-low standby power dissipation.

Since this device is functionally compatible as well as pin compatible with the TLC27L2 and TLC27L7, the TLC1078 easily upgrades existing designs that can benefit from its improved performance.

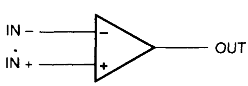
The TLC1078 incorporates internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC1078 design also inhibits latchup of the device inputs and outputs even with surge currents as large as 100 mA.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C. The wide range of packaging options includes small-outline and chip carrier versions for high-density system applications.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... ± V_{DD}
Input voltage range, V_I (any input) .... – 0.3 V to V_{DD}
Input current, I_I (each input) .... ± 5 mA
Output current, I_O (each output) .... ± 30 mA
Total current into V_{DD} terminal (see Note 4) .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... – 55°C to 125°C
I-suffix .... – 40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... – 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package .... 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	– 0.2		3.5	– 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	– 0.2		8.5	– 0.2		8.5	V
Input voltage, V_I	V_{DD} = 5 V	0		3.5	– 0.2		3.5	– 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	– 0.2		8.5	– 0.2		8.5	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		160	450		180	600	μV
			Full range			800			950	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	480		500	825		V/mV
			0°C	250	700		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		19	34		29	46	μA
			0°C		24	42		36	66	
			70°C		15	28		22	40	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			39		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		160	450		180	600	μV
			Full range			950			1100	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	480		500	825		V/mV
			−40°C	250	900		500	1550		
			85°C	150	330		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		19	34		29	46	μA
			−40°C		31	54		49	86	
			85°C		15	26		20	36	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			42°		
			85°C		28°			32°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

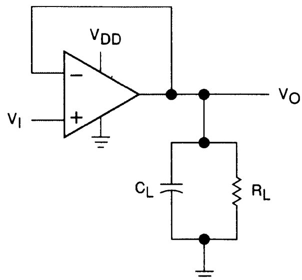
PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		160	450		180	600	μV
			Full range			1250			1400	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	− 0.3 to 4.2		0 to 9	− 0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			− 55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			− 55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	480		500	825		V/mV
			− 55°C	250	950		500	1750		
			125°C	75	200		150	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			− 55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			− 55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		19	34		29	46	μA
			− 55°C		35	60		56	96	
			125°C		14	24		18	30	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

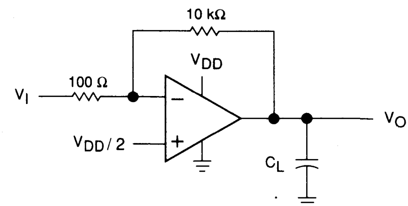
PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			− 55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			− 55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			− 55°C		39°			43°		
			125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



C_L includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



C_L includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1078 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

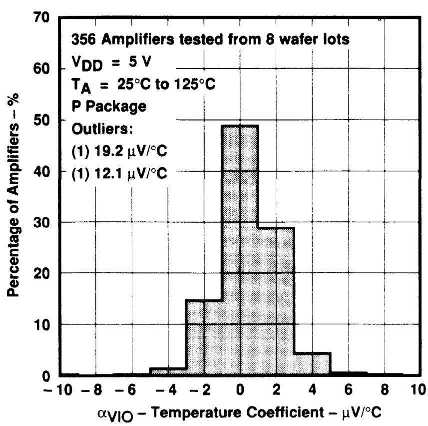


FIGURE 3

DISTRIBUTION OF TLC1078 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

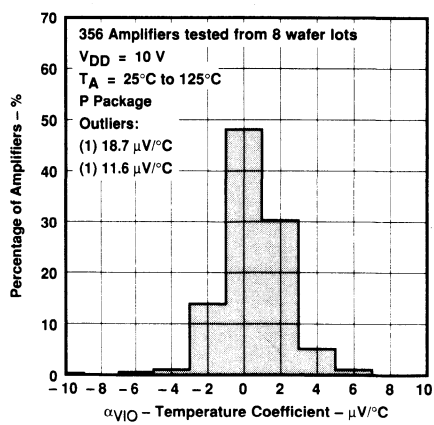


FIGURE 4

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

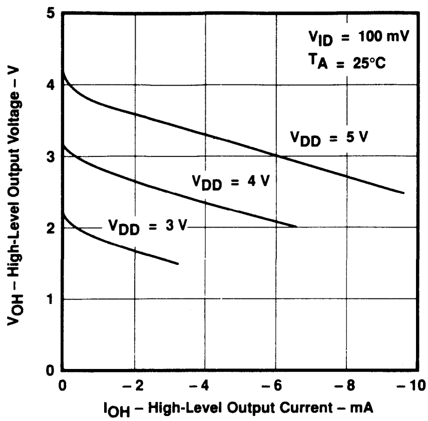


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

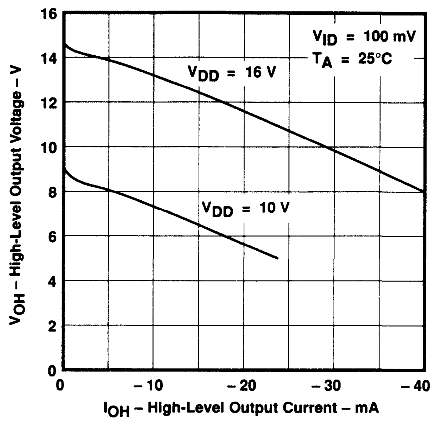


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

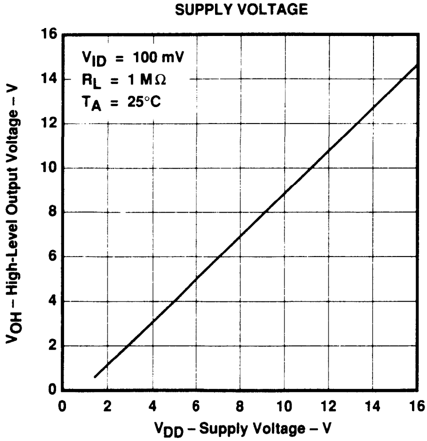


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

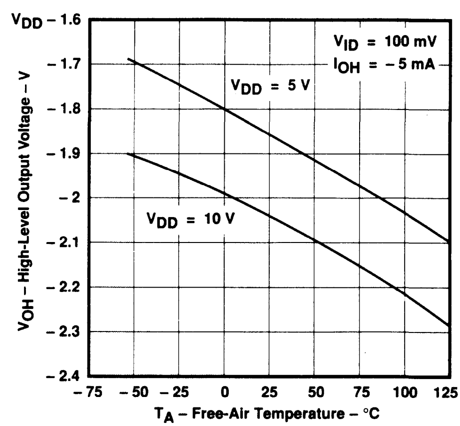


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

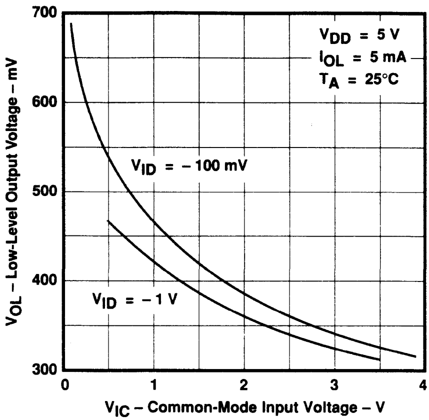


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

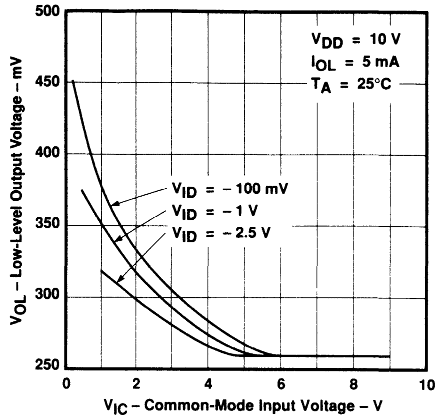


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

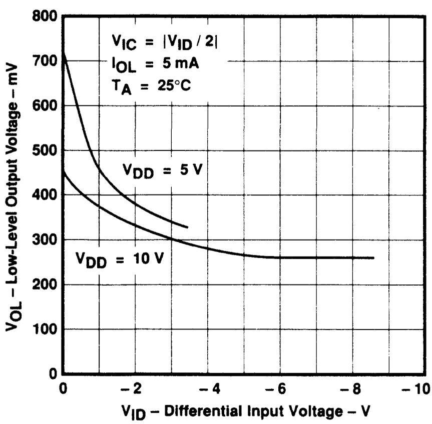


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

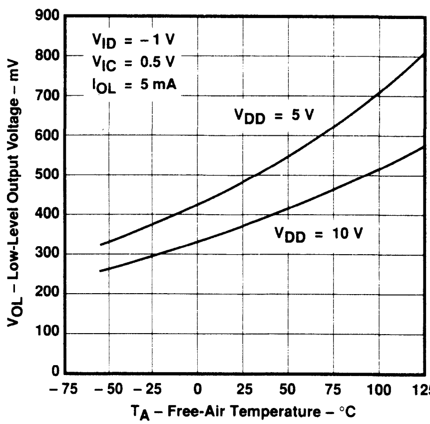


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

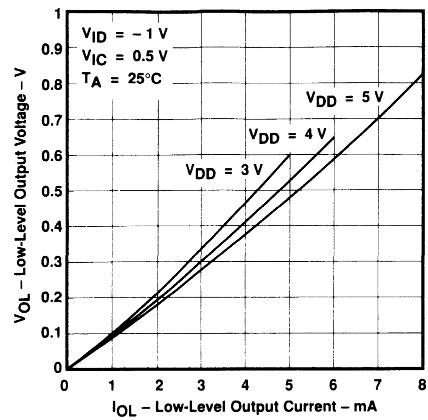


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

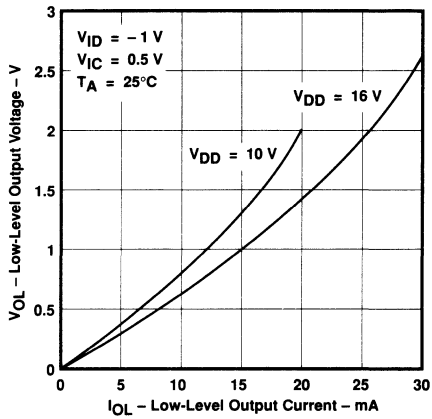


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

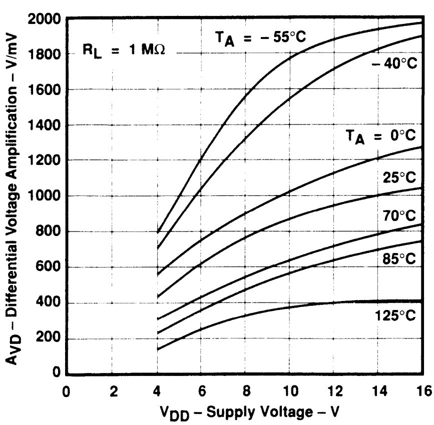


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

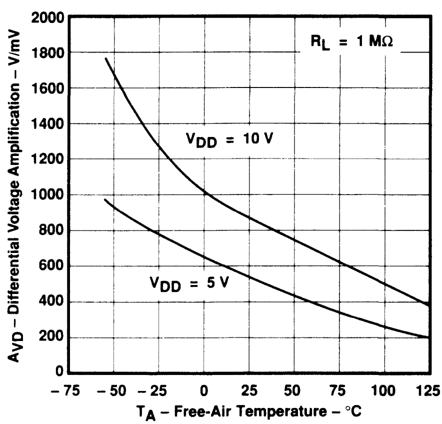


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

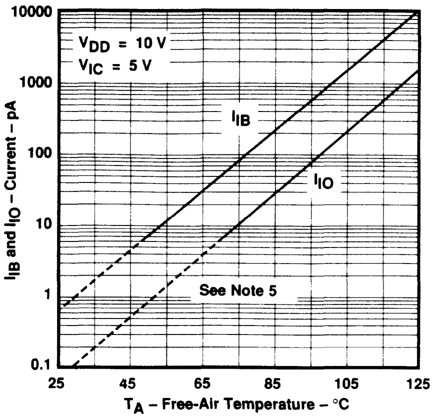


FIGURE 17

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

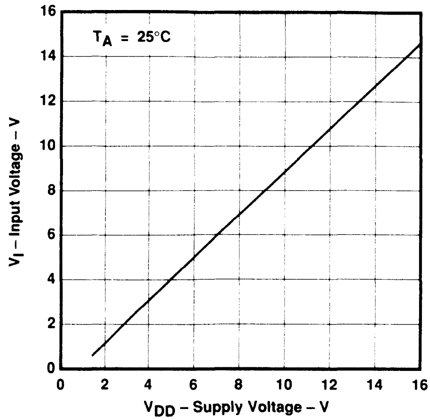


FIGURE 18

SUPPLY CURRENT vs SUPPLY VOLTAGE

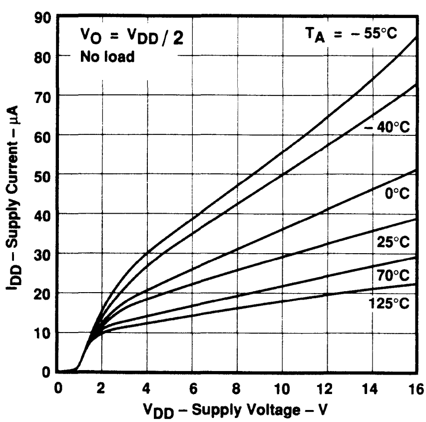


FIGURE 19

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

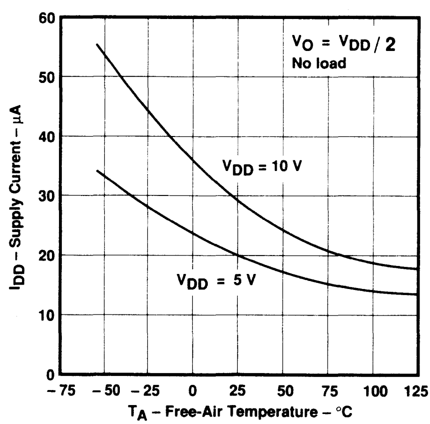


FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

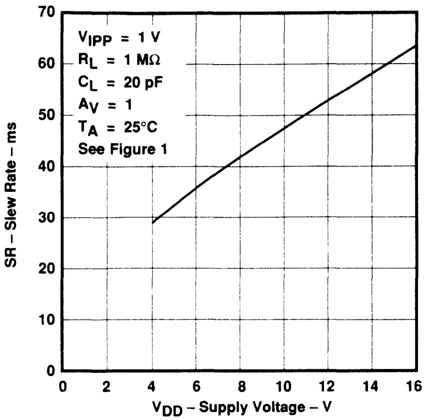


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

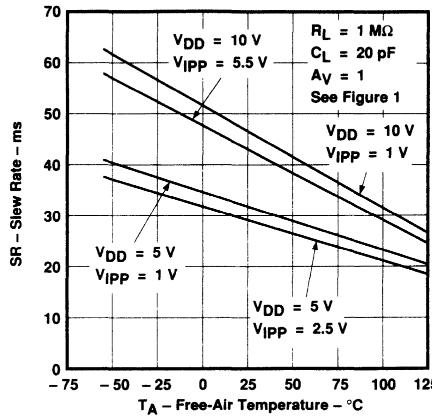


FIGURE 22

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

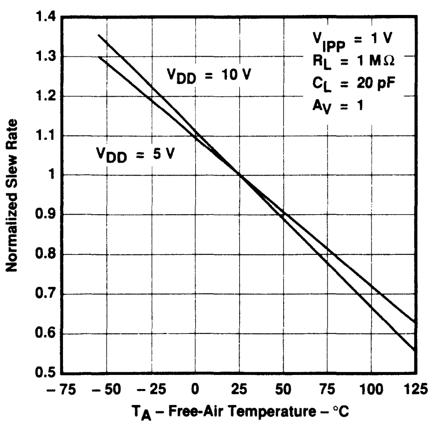


FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

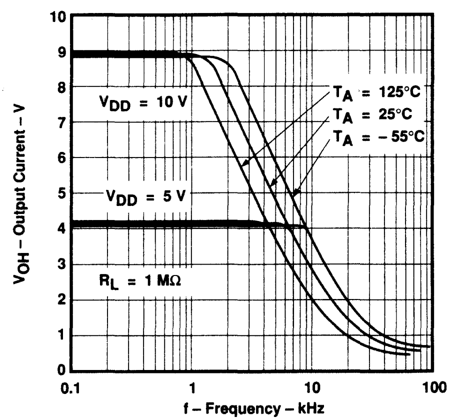


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

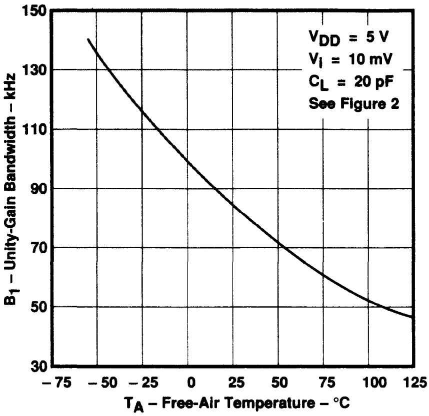


FIGURE 25

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

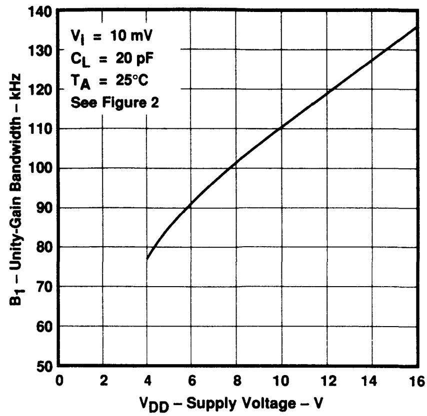


FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

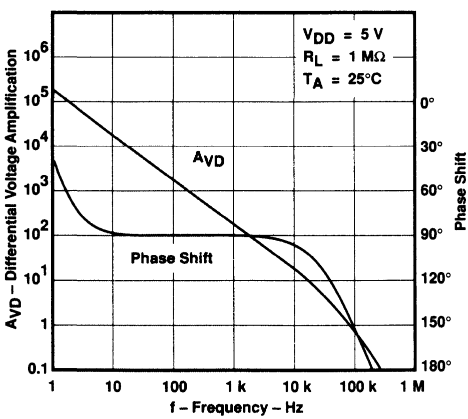


FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

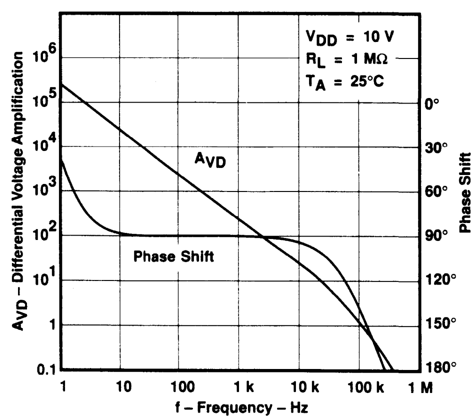


FIGURE 28

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

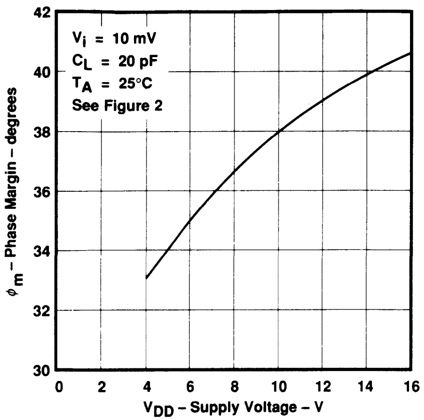


FIGURE 29

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

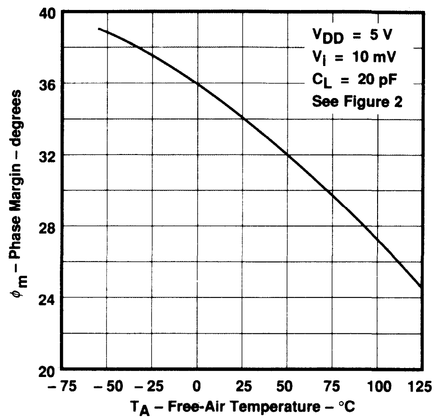


FIGURE 30

PHASE MARGIN
vs
CAPACITIVE LOAD

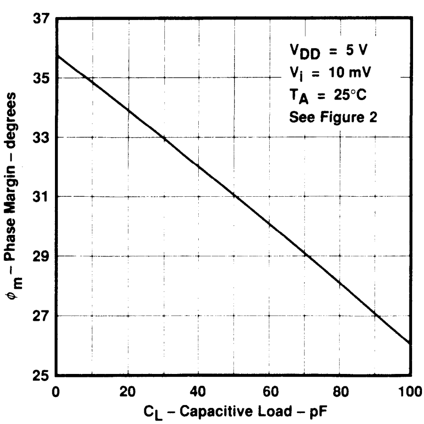


FIGURE 31

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

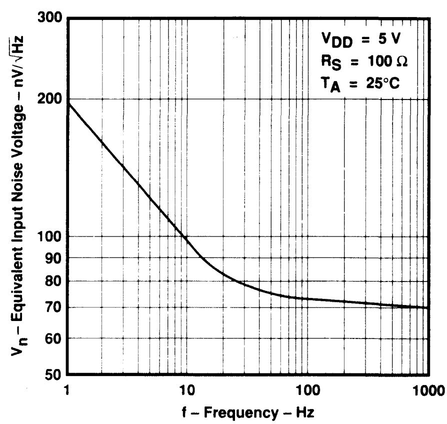
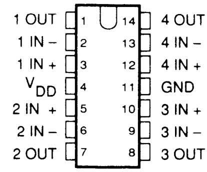


FIGURE 32

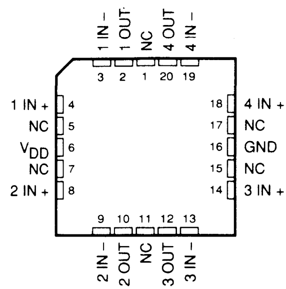
†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

- **Power Dissipation as Low as 10 μW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 850 μV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days**
- **High Impedance LinCMOS Inputs I_{IB} = 600 fA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD Protection Circuitry**
- **14 Pin Small-Outline Package Option Also Available in Tape-and-Reel**

D, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC1079 is an ultra-low offset voltage, high gain CMOS operational amplifier. This high performance along with 110 kHz bandwidth and 47 V/ms slew rate is achieved on just 150 μW power dissipation per amplifier.

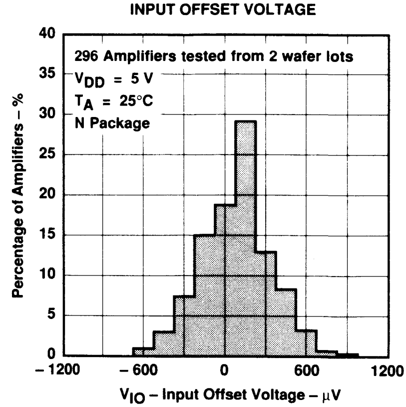
With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1079 is an ideal solution for low voltage battery-operated systems. The 20 mA output drive capability means that the TLC1079 can easily drive small resistive and large capacitive loads when needed, while

AVAILABLE OPTIONS

T_A	PACKAGE			
	Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	TLC1079CD	TLC1079CN	TLC1079CJ	—
− 40°C to 85°C	TLC1079ID	TLC1079IN	TLC1079IJ	—
− 55°C to 125°C	—	—	TLC1079MJ	TLC1079MFK

NOTE 1: D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC1079CDR).

DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE



description (continued)

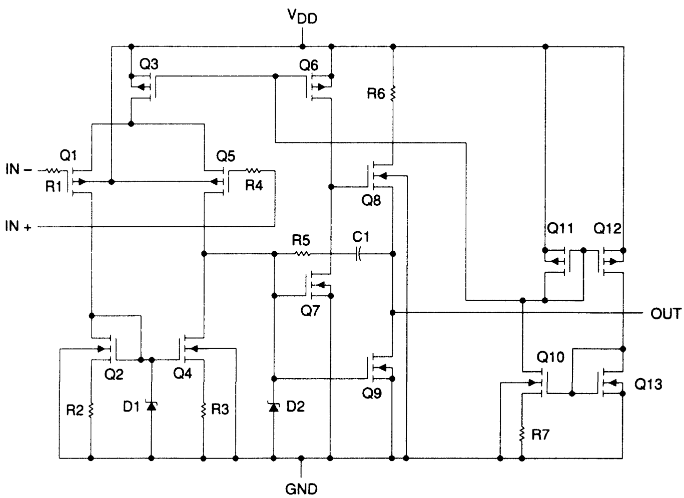
maintaining ultra-low standby power dissipation.

Since this device is functionally compatible as well as pin compatible with the TLC27L4 and TLC27L9, the TLC1079 easily upgrades existing designs that can benefit from its improved performance.

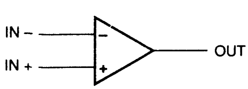
The TLC1079 incorporates internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC1079 design also inhibits latchup of the device inputs and outputs even with surge currents as large as 100 mA.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I- suffix devices are characterized for operation from – 40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C. The wide range of packaging options includes small-outline and chip carrier versions for high-density system applications.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... – 0.3 V to V_{DD}
Input current, I_I (each input) .... ± 5 mA
Output current, I_O (each output) .... ± 30 mA
Total current into V_{DD} terminal (see Note 4) .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... – 55°C to 125°C
I-suffix .... – 40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... – 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .... 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4 The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	440 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M- SUFFIX			I- SUFFIX			C- SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	– 0.2		3.5	– 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	– 0.2		8.5	– 0.2		8.5	V
Input voltage, V_I	V_{DD} = 5 V	0		3.5	– 0.2		3.5	– 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	– 0.2		8.5	– 0.2		8.5	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1200			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	480		500	825		V/mV
			0°C	250	700		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		39	68		57	92	μA
			0°C		48	84		72	132	
			70°C		31	56		44	80	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			39		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1350			1650	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	− 0.2 to 4	− 0.3 to 4.2		− 0.2 to 9	− 0.3 to 9.2		V
			Full range	− 0.2 to 3.5			− 0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			− 40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			− 40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	480		500	825		V/mV
			− 40°C	250	900		500	1550		
			85°C	150	330		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			− 40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			− 40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		39	68		57	92	μA
			− 40°C		62	108		98	172	
			85°C		29	52		40	72	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			− 40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			− 40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			− 40°C		38°			42°		
			85°C		28°			32°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

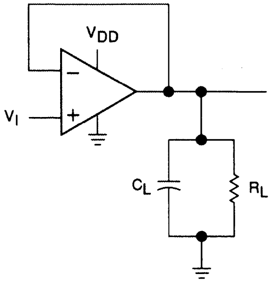
PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1600			1900	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	250	480		500	825		V/mV
			−55°C	250	950		500	1750		
			125°C	75	200		150	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD} / 2, V_{IC} = V_{DD} / 2, No load	25°C		39	68		57	92	μA
			−55°C		69	120		111	192	
			125°C		27	48		35	60	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

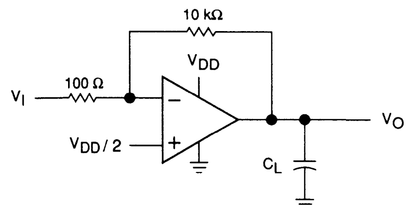
PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−55°C		39°			43°		
			125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



C_L includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



C_L includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1079 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

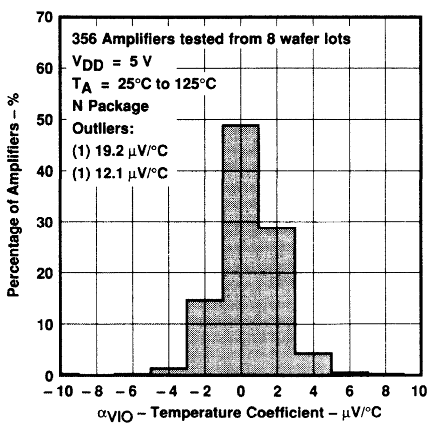


FIGURE 3

DISTRIBUTION OF TLC1079 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

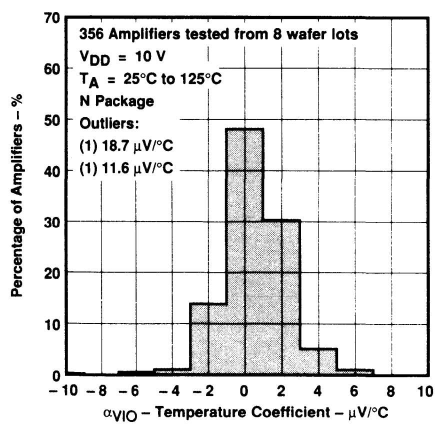


FIGURE 4

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

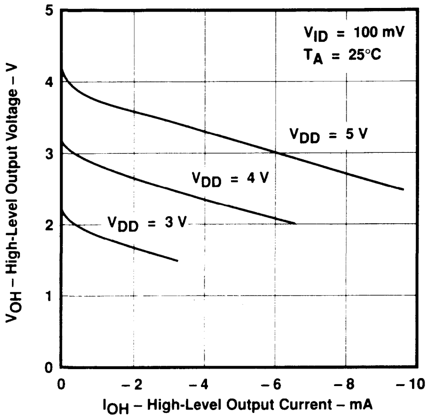


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

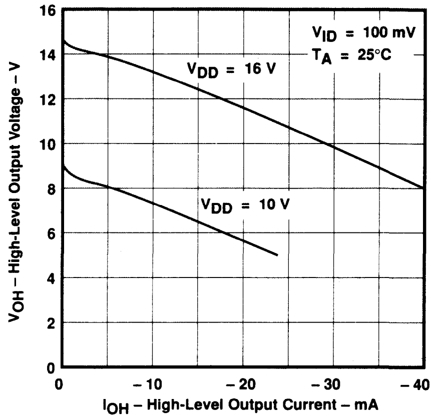


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

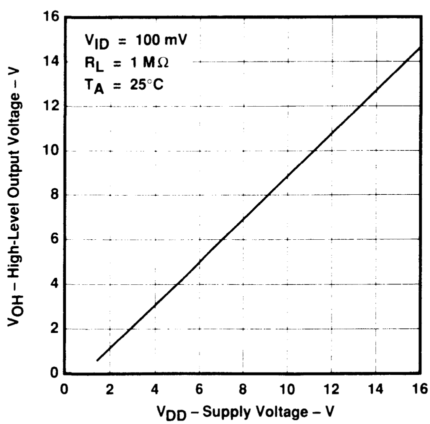


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

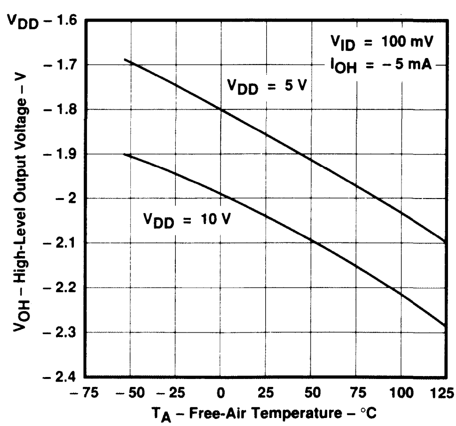


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

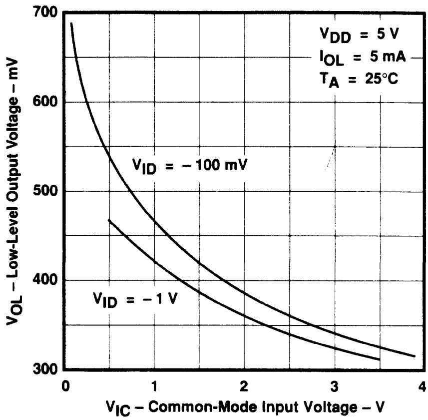


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

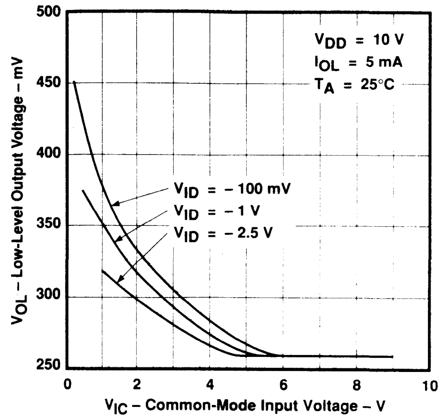


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

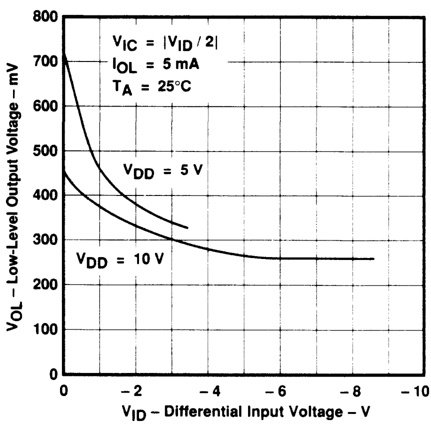


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

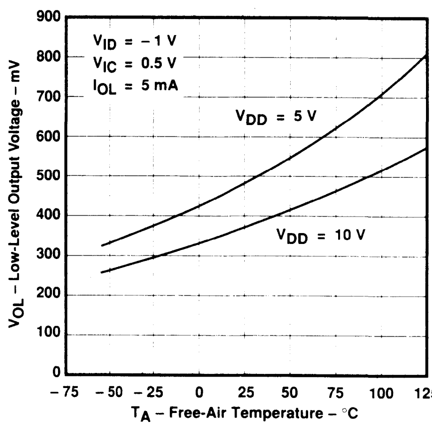


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

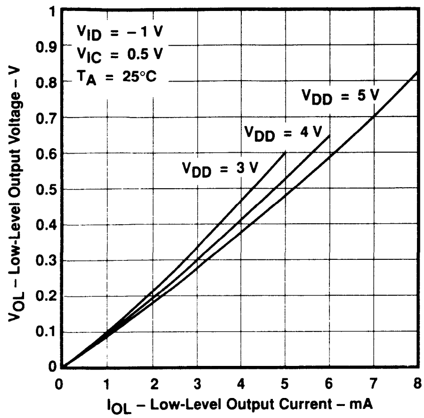


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

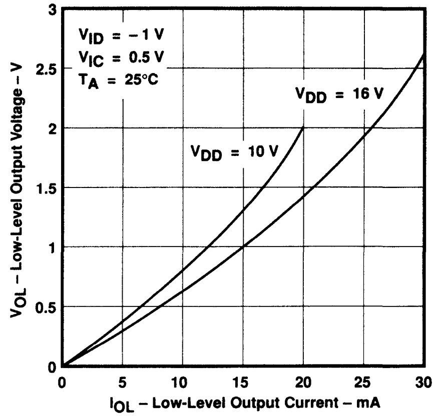


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

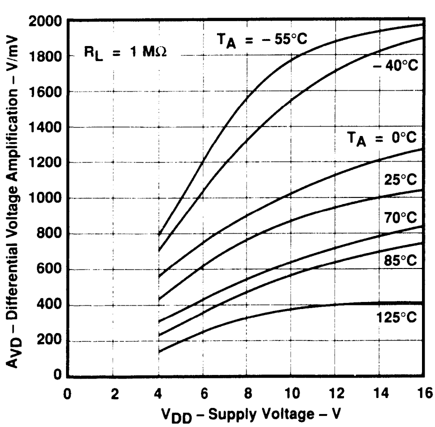


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

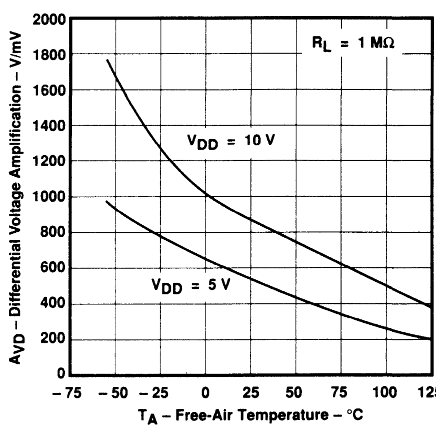


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

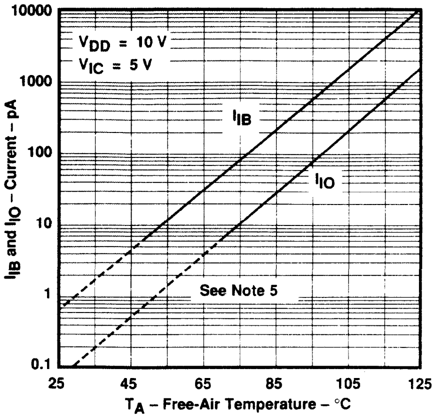


FIGURE 17

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

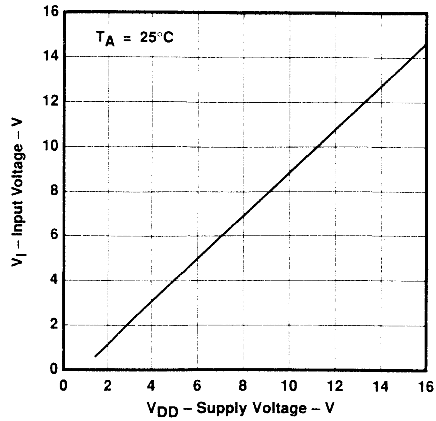


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

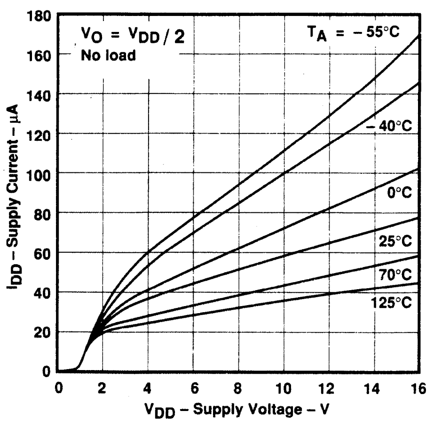


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

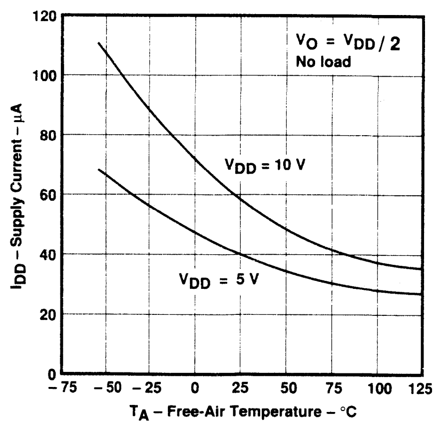


FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE vs SUPPLY VOLTAGE

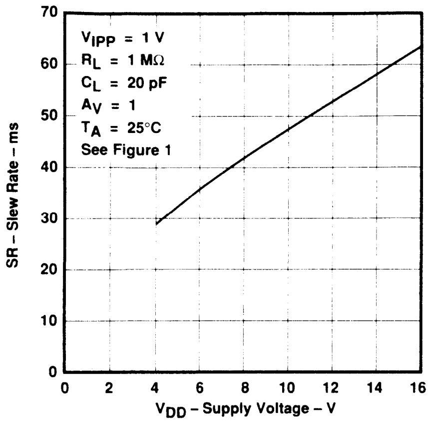


FIGURE 21

SLEW RATE vs FREE-AIR TEMPERATURE

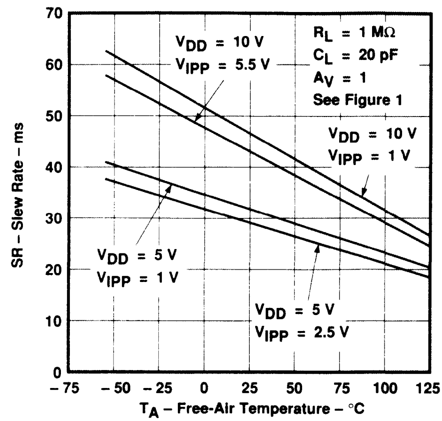


FIGURE 22

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

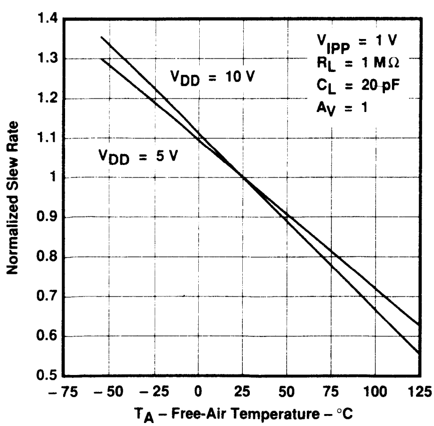


FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

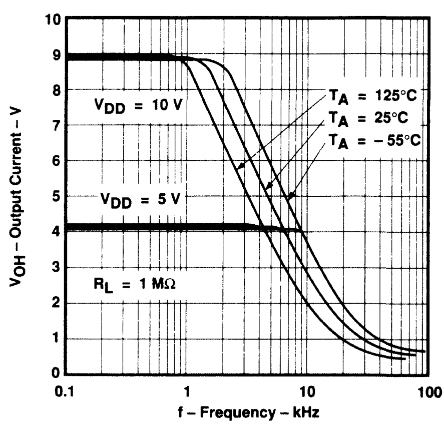


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

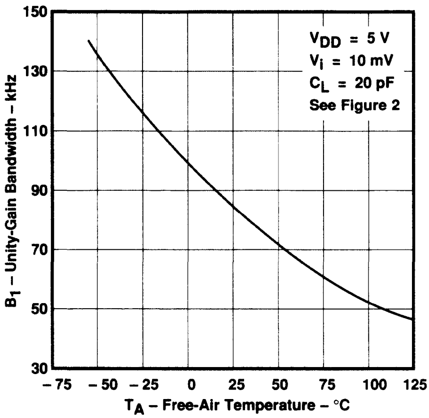


FIGURE 25

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

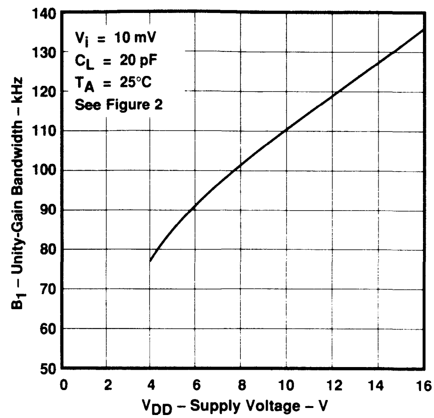


FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

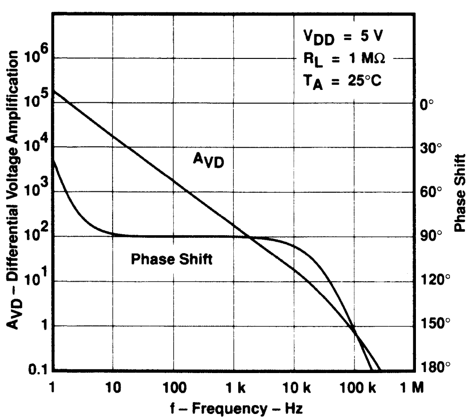


FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

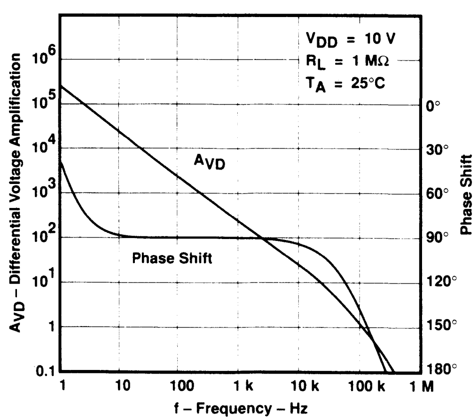


FIGURE 28

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

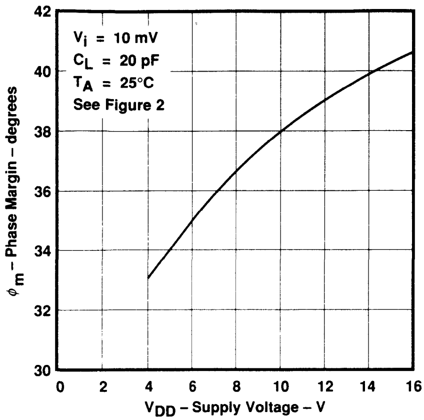


FIGURE 29

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

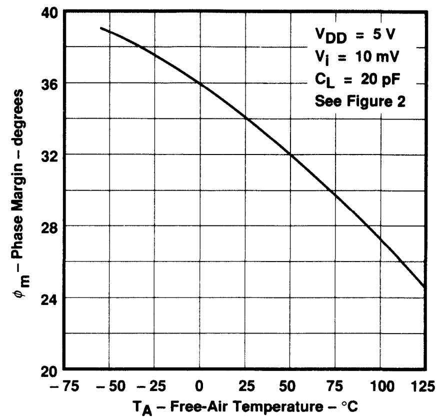


FIGURE 30

PHASE MARGIN
vs
CAPACITIVE LOAD

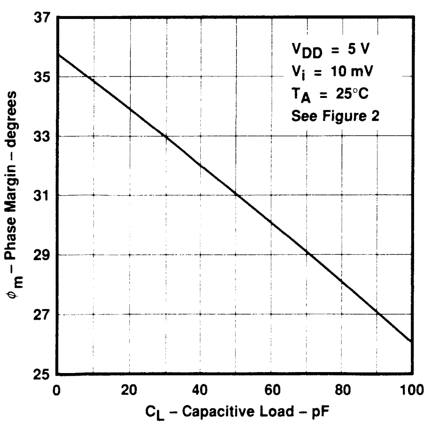


FIGURE 31

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

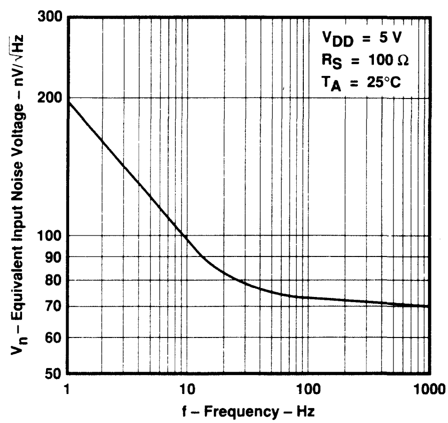


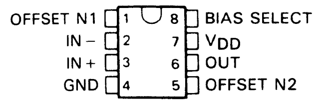
FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

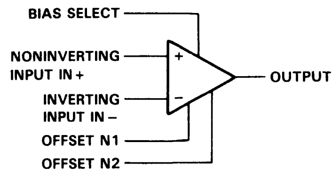
D2751, JULY 1983—REVISED OCTOBER 1987

- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Low Noise . . . 30 nV $\sqrt{Hz}$ Typ at 1 kHz (High Bias)**

D, JG, OR P PACKAGE
(TOP VIEW)



symbol



description

The TLC251C, TLC251AC, and TLC251BC are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The series features guaranteed operation down to a 1.4 V supply and is stable at unity gain.

The TLC251C series is characterized for operation from 0°C to 70°C.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. Remote and

DEVICE FEATURES

PARAMETER	LOW BIAS	MEDIUM BIAS	HIGH BIAS
Supply current (Typ)	10 μA	150 μA	1000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC251C	10 mV	10 mV	10 mV
TLC251AC	5 mV	5 mV	5 mV
TLC251BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

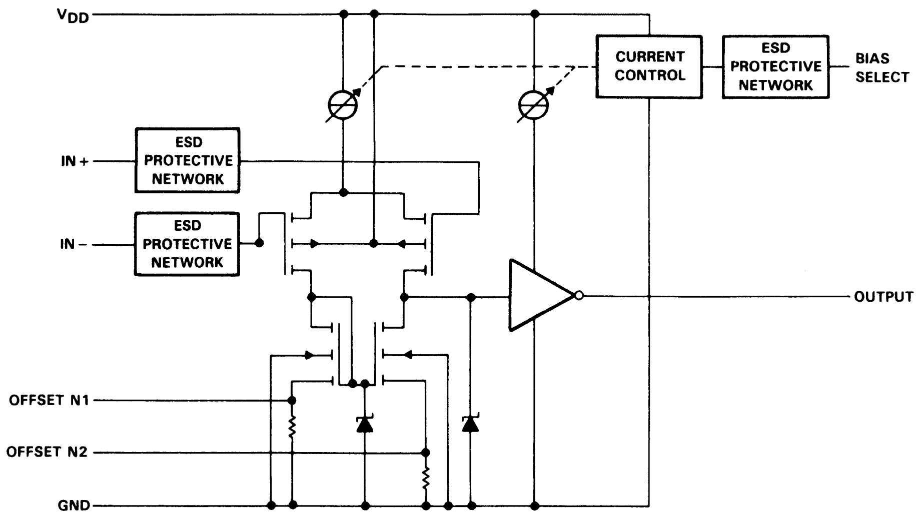
† The long-term drift value applies after the first month.

LinCMOS is a trademark of Texas Instruments Incorporated

description (continued)

inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251C series. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251C series is well suited to solve the difficult problems associated with single battery and solar cell-powered applications.

schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage (see Note 2) . . . . ±18 V
Input voltage range (any input) . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
JG (glass mounted)	825 mW	6.6 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 3 V	0		3	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C
Bias Select pin voltage		See application notes			

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C	Low		0.7		µV/°C
					Medium		2		
					High		5		
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	−0.2 to 9			V
V_{OM}	Peak output voltage range‡		V_{ID} = 100 mV	25°C	Any	8	8.6		V
				0°C to 70°C		7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	Low	30	500		V/mV
					Medium	20	280		
					High	10	40		
				0°C to 70°C	Low	25			
					Medium	15			
					High	7.5			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	Any	70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	Low	70	88		dB
					Medium	70	88		
					High	65	82		
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C	Any		−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV				15		
$I_{IH(SEL)}$	High-level input current to bias select		$V_{I(SEL)}$ = 0 V	25°C	High		10.5		µA
$I_{IL(SEL)}$	Low-level input current to bias select		$V_{I(SEL)}$ = 10 V	25°C	Low		1.3		µA
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C	Low		10	20	µA
					Medium		150	300	
					High		1000	2000	
				0°C to 70°C	Low			30	
					Medium			400	
					High			2200	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V

PARAMETER			TEST CONDITIONS†		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
αV_{IO}	Average temperature coefficient of input offset voltage			0°C to 70°C	Any		1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				300	
I_{IB}	Input bias current		V_O =0.2 V	25°C	Any		1		pA
				0°C to 70°C				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	Any		450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C	Low		20		V/mV
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, V_{IC} = V_{IC} min	25°C	Any		77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C	Low		2		μA
					High		12		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1	Unity-gain bandwidth	C_L = 10 pF	Low		12		kHz
			High		75		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.01		
	Overshoot factor	See Figure 1	Low		35%		
			High		30%		

operating characteristics, V_{DD} = 10 V, T_A = 25 °C

PARAMETER	TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1 Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50Ω	Low		0.1		MHz
		Medium		0.7		
		High		2.3		
SR Slew rate at unity gain	See Figure 1	Low		0.04		V/μs
		Medium		0.6		
		High		4.5		
Overshoot factor	See Figure 1	Low		30%		
		Medium		35%		
		High		35%		
ϕ_m Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = pF	Low		43°		
		Medium		43°		
		High		50°		
V_n Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	Low		70		nV/$\sqrt{Hz}$
		Medium		38		
		High		30		

PARAMETER MEASUREMENT INFORMATION

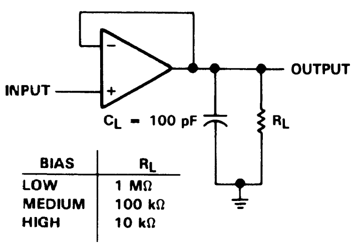


FIGURE 1. UNITY-GAIN AMPLIFIER

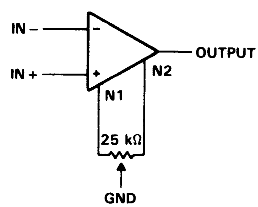


FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
BIAS SELECT PIN VOLTAGE

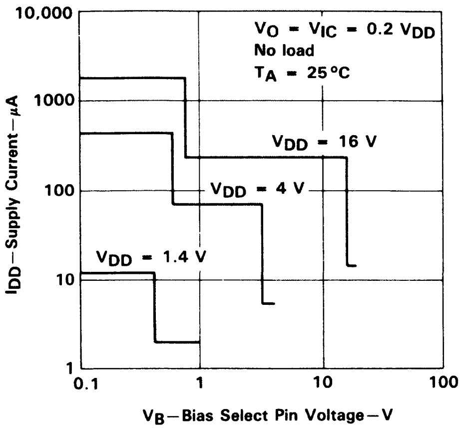


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

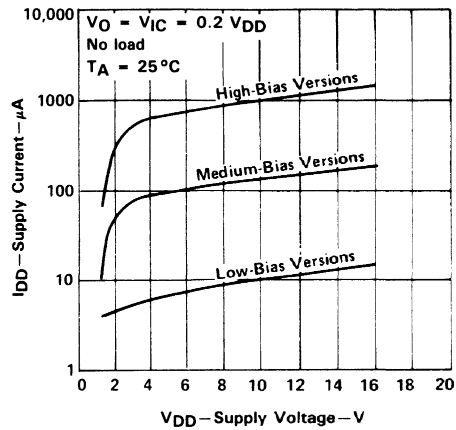


FIGURE 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

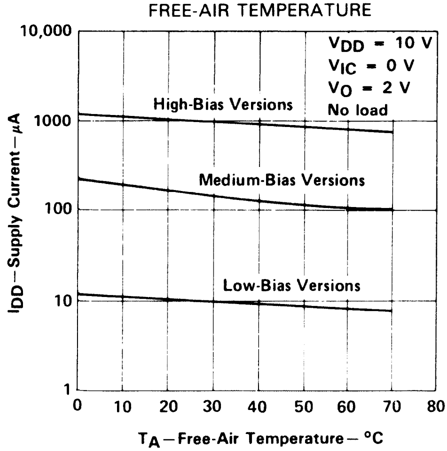


FIGURE 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

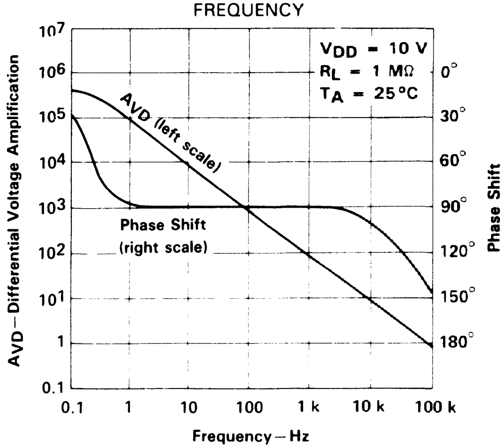


FIGURE 6

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

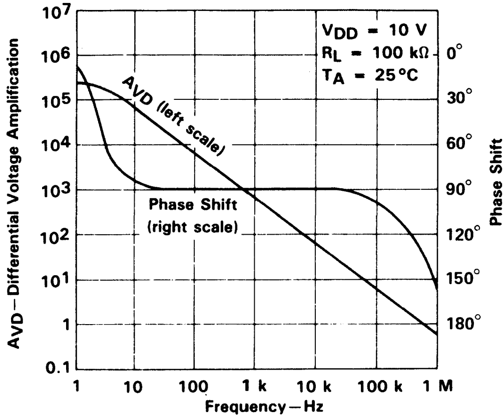


FIGURE 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

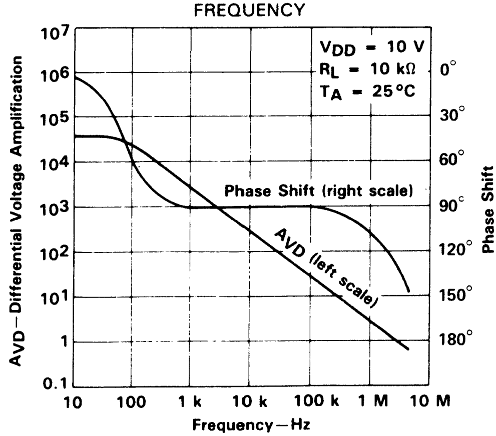


FIGURE 8

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

using the bias select pin

The TLC251C series has a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium and low-bias modes at V_{DD} = 1.4 V are typically 2 μA, and in the high mode are typically 12 μA. The following table shows the recommended bias select pin connections at V_{DD} = 10 V:

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}‡
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

†The Bias Select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.
‡For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

input offset nulling

The TLC251C series offers external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At I_{DD} settings of 150 and 1000 μA (medium and high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low bias or when the amplifier is used below 4 V, total nulling may not be possible on all units.

supply configurations

Even though the TLC251C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

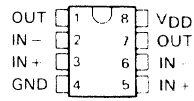
circuit layout precautions

The user is cautioned that when ever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

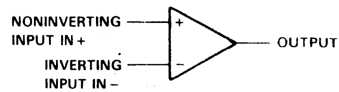
D2752, JUNE 1983 REVISED OCTOBER 1987

- A Suffix Versions Offer 5-mV V_{IO}
- B Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise . . . 30 nV/$\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)

D, JG, OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC252C, TLC25L2C, and TLC25M2C are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers guaranteed operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC252C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252C series devices. Remote and inaccessible equipment

DEVICE FEATURES

PARAMETER	TLC25L2C (LOW BIAS)	TLC25M2C (MEDIUM BIAS)	TLC252C (HIGH BIAS)
Supply current (Typ)	20 μA	300 μA	2000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC252C, TLC25L2C, TLC25M2C	10 mV	10 mV	10 mV
TLC252AC, TLC25L2AC, TLC25M2AC	5 mV	5 mV	5 mV
TLC252BC, TLC25L2BC, TLC25M2BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

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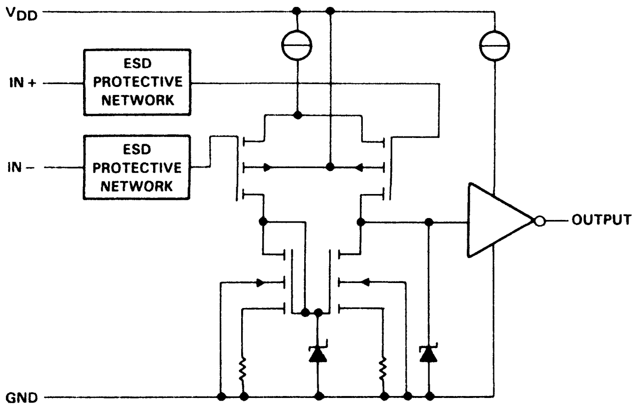
description (continued)

applications are possible using their low-voltage and low-power capabilities. The TLC252C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 8-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage (see Note 2) . . . . ±18 V
Input voltage range (any input) . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperture range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
JG (glass mounted)	825 mW	6.6 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 3 V	0		3	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C MIN	TLC252_C TYP	TLC252_C MAX	TLC25L2_C MIN	TLC25L2_C TYP	TLC25L2_C MAX	TLC25M2_C MIN	TLC25M2_C TYP	TLC25M2_C MAX	UNIT
V_O	Input offset voltage	TLC25_2C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0°C to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2200			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_2C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
αV_{IO}	Average temperature coefficient of input offset voltage			0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current (each amplifier)		No load, V_O = 0.2 V	25°C		12			2			2		μA

† All characteristics are measured under open loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

TEST CONDITIONS		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MHz
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		nV/√Hz
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

PARAMETER MEASUREMENT INFORMATION

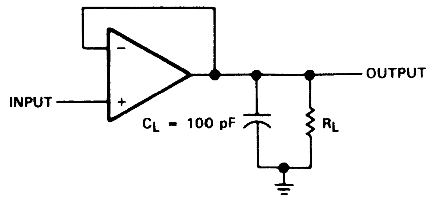


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

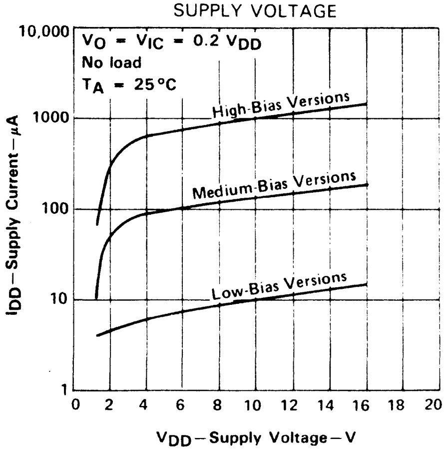


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

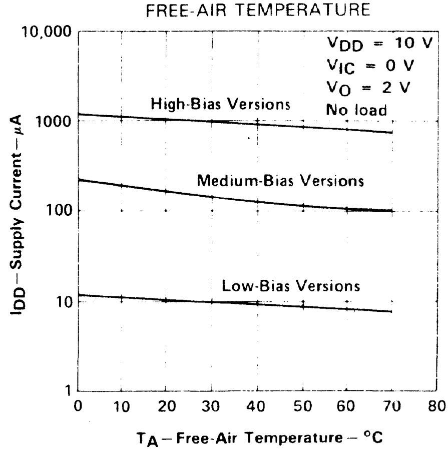


FIGURE 3

TYPICAL CHARACTERISTICS

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

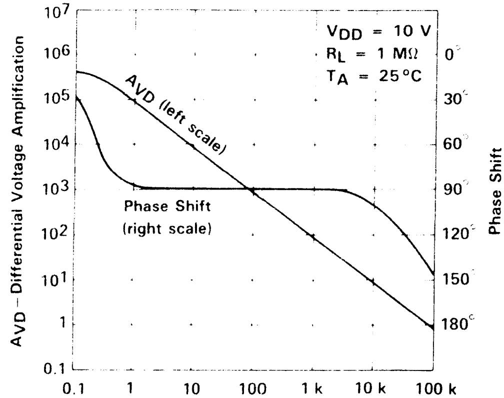


FIGURE 4

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

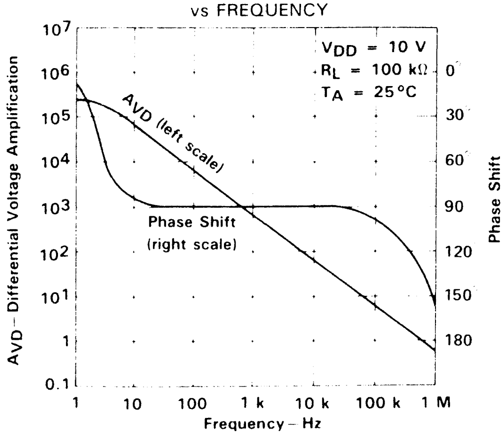


FIGURE 5

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

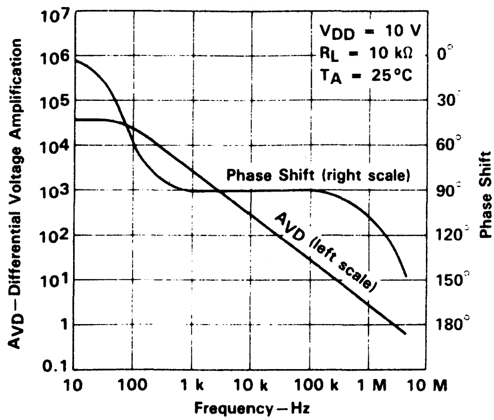


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC252C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

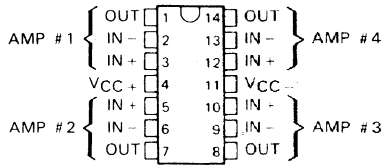
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

3 Operational Amplifiers

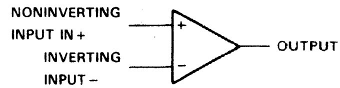
D2753, JUNE 1983—REVISED OCTOBER 1987

- A Suffix Versions Offer 5-mV V_{IO}
- B Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise . . . 30 nV/√Hz Typ at f = 1 kHz (High-Bias Versions)

D, J, OR N PACKAGE
(TOP VIEW)



symbol (each amplifier)



description

The TLC254C, TLC25L4C, and TLC25M4C are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers guaranteed operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC254C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal

DEVICE FEATURES

PARAMETER	TLC25L4C (LOW BIAS)	TLC25M4C (MEDIUM BIAS)	TLC254C (HIGH BIAS)
Supply current (Typ)	40 μA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC254C, TLC25L4C, TLC25M4C	10 mV	10 mV	10 mV
TLC254AC, TLC25L4AC, TLC25M4AC	5 mV	5 mV	5 mV
TLC254BC, TLC25L4BC, TLC25M4BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

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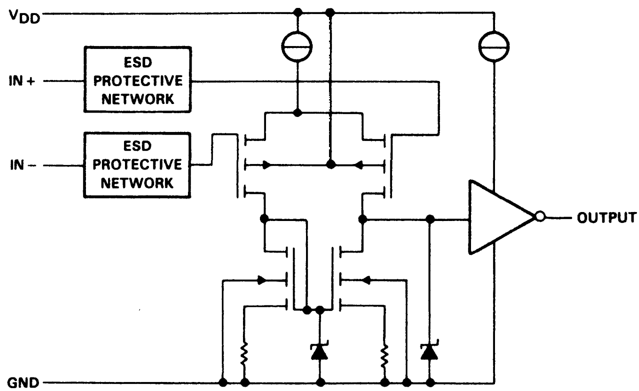
TEXAS INSTRUMENTS

description (continued)

buffering are all easily designed with the TLC254C series devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. The TLC254C series is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	±18 V
Input voltage range (any input)	−0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
J (glass mounted)	1025 mW	8.2 mW/°C	25°C
N	1150 mW	9.2 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 3 V	0		3	
	V_{DD} = 10 V	0		9	
	V_{DD} = 16 V	0		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_4C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
αV_{IO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0°C to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			55			55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2200			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values. For low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C MIN	TLC254_C TYP	TLC254_C MAX	TLC25L4_C MIN	TLC25L4_C TYP	TLC25L4_C MAX	TLC25M4_C MIN	TLC25M4_C TYP	TLC25M4_C MAX	UNIT
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current (each amplifier)		No load, V_O = 0.2 V	25°C		12			2			2		μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin and has the following values: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

TEST CONDITIONS		TEST CONDITIONS	TLC254_C MIN	TLC254_C TYP	TLC254_C MAX	TLC25L4_C MIN	TLC25L4_C TYP	TLC25L4_C MAX	TLC25M4_C MIN	TLC25M4_C TYP	TLC25M4_C MAX	UNIT
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

TEXAS INSTRUMENTS

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MHz
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		nV/√Hz
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

PARAMETER MEASUREMENT INFORMATION

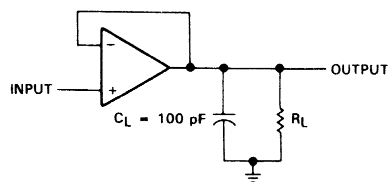


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

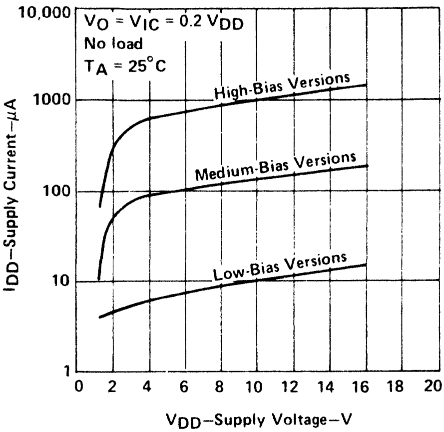


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

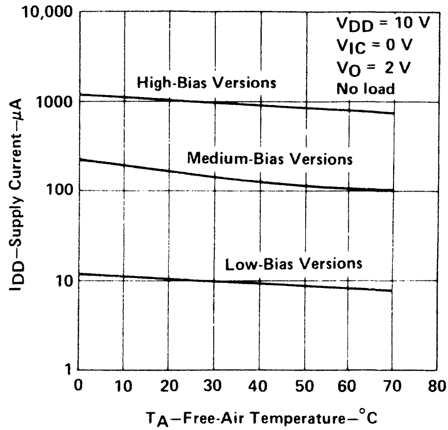


FIGURE 3

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

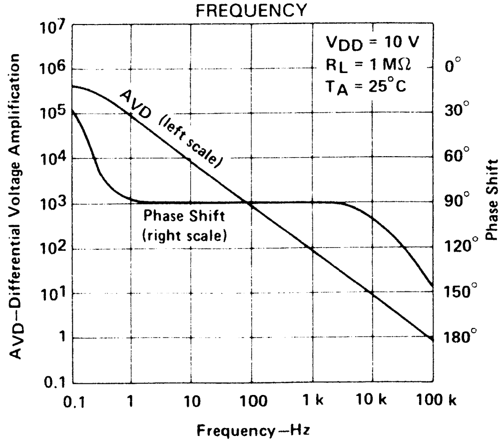


FIGURE 4

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

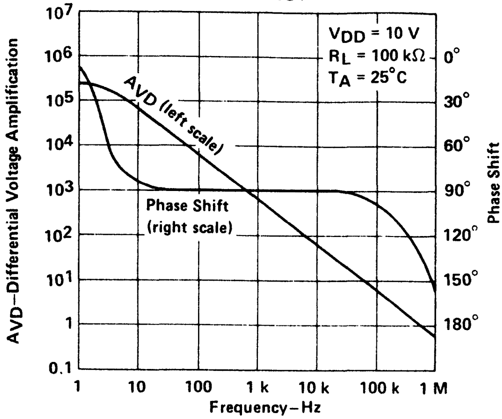


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

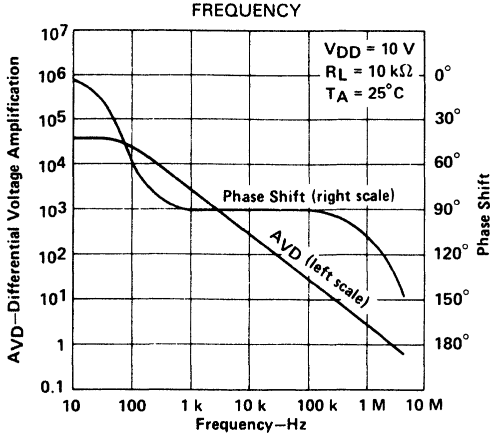


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC254C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

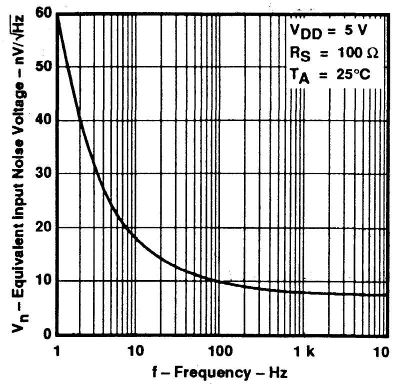
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

- **100% Noise Test . . .**
  25 nV/√Hz Max, f = 10 Hz
  12 nV/√Hz Max, f = 1 kHz
- **Low Input Offset Voltage . . . 200 μV Max**
- **Excellent Offset Voltage Stability with Temperature . . . 0.5 μV/°C Typ**
- **Low Input Bias Current . . . 1 pA Typ at T_A = 25°C**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**

description

The TLC2201, TLC2201A, and TLC2201B are precision, low-noise operational amplifiers using Texas Instruments Advanced LinCMOS™ process. These devices combine the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

TYPICAL EQUIVALENT
INPUT NOISE VOLTAGE
vs
FREQUENCY



The combination of excellent dc and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal conditioning applications in either single-supply or split-supply configurations.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latchup. In addition, internal ESD protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

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Operational Amplifiers

AVAILABLE OPTIONS

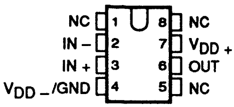
T_A	V_{IO} max AT 25°C	V_n max f = 10 Hz AT 25°C	V_n max f = 1 kHz AT 25°C	PACKAGE SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CHIP CARRIER (FK)	METAL CAN (L)
0°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BCD	TLC2201BCP	TLC2201BCJG	—	TLC2201BCL
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201ACD	TLC2201ACP	TLC2201ACJG	—	TLC2201ACL
70°C	500 μV	—	—	TLC2201CD	TLC2201CP	TLC2201CJG	—	TLC2201CL
– 40°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BID	TLC2201BIP	TLC2201BIJG	—	TLC2201BIL
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201AID	TLC2201AIP	TLC2201AIJG	—	TLC2201AIL
85°C	500 μV	—	—	TLC2201ID	TLC2201IP	TLC2201IJG	—	TLC2201IL
– 55°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BMD	TLC2201BMP	TLC2201BMJG	TLC2201BMFK	TLC2201BML
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201AMD	TLC2201AMP	TLC2201AMJG	TLC2201AMFK	TLC2201AML
125°C	500 μV	—	—	TLC2201MD	TLC2201MP	TLC2201MJG	TLC2201MFK	TLC2201ML

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC2201BCDR).

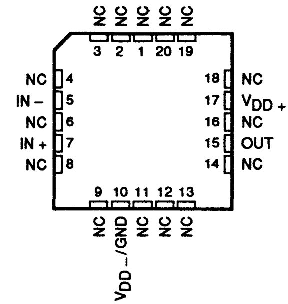
description (continued)

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

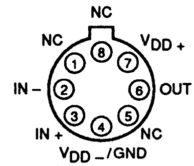
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



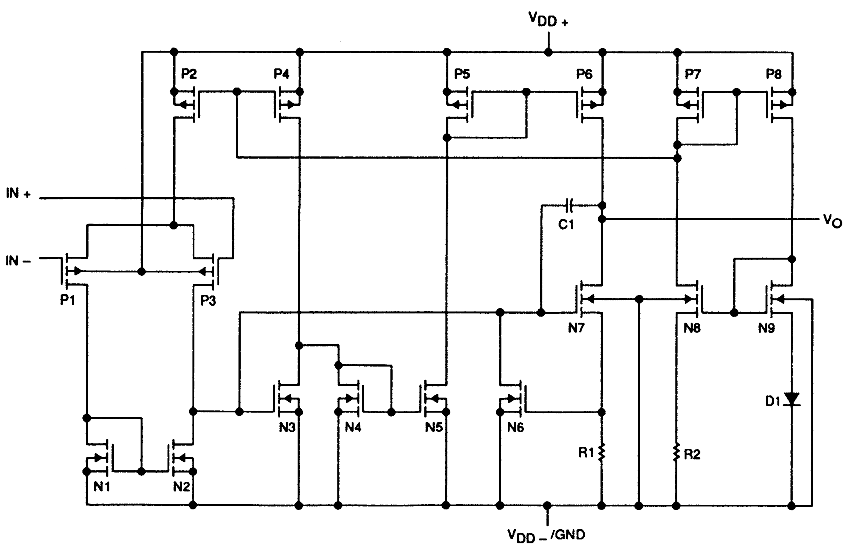
L PACKAGE
(TOP VIEW)



Pin 4 of the L package is in electrical contact with the case.

NC – No internal connection

equivalent schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) .... 8 V
Supply voltage, V_{DD-} (see Note 1) .... −8 V
Differential input voltage (see Note 2) .... ±16 V
Input voltage range, V_I (any input, see Note 1) .... ±8 V
Input current, I_I (each input) .... ±5 mA
Output current, I_O .... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Continuous total dissipation .... see Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... −55°C to 125°C
I-suffix .... −40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

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Operational Amplifiers

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	±2.3		±8	±2.3		±8	±2.3		±8	V
Common-mode input voltage, V_{IC}	V_{DD-}		$V_{DD+} - 2.3$	V_{DD-}		$V_{DD+} - 2.3$	V_{DD-}		$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	–5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		V
			Full range	– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ,	25°C	400	560		V/mV
			Full range	200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	45			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 500\ k\Omega$	25°C	400	560		400	560		V/mV
			Full range	200			200			
		$V_O = \pm4$ V, $R_L = 10\ k\Omega$	25°C	90	100		90	100		
			Full range	45			45			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm2.3$ V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°			48°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	75			75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	10			10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		−40°C to 85°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500\ k\Omega$,	25°C	400	560		V/mV
			Full range	250			
		$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	90	100		
			Full range	65			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C	2	2.7		V/µs
			Full range	1.4			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10\ k\Omega$, $C_L = 100$ pF	25°C		48°		

†Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	μV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		−40°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	250			250			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	65			65			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/μs
			Full range	1.4			1.4			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is −40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ; C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is – 40°C to 85°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ,	25°C	400	560		V/mV
			Full range	300			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	70			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/μs
			Full range	1.5			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC MIN	TLC2201AC TYP	TLC2201AC MAX	TLC2201BC MIN	TLC2201BC TYP	TLC2201BC MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		80	200		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 500$ kΩ	25°C	400	560		400	560		V/mV
			Full range	300			300			
		$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	90	100		90	100		
			Full range	70			70			
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC MIN	TLC2201AC TYP	TLC2201AC MAX	TLC2201BC MIN	TLC2201BC TYP	TLC2201BC MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/µs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION

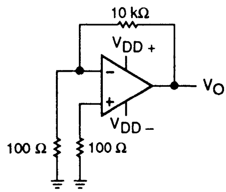
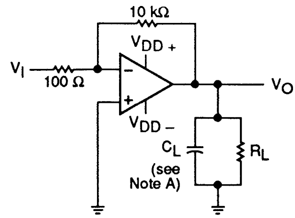
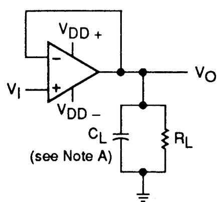


FIGURE 1. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 2. PHASE MARGIN TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 3. SLEW RATE TEST CIRCUIT

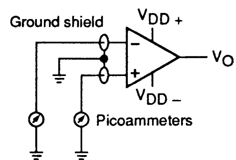


FIGURE 4. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TLC2201, TLC2201A, and TLC2201B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Texas Instruments offers automated production noise testing to meet individual applications requirements. Noise voltage at f = 10 Hz and f = 1 kHz is 100% tested on every TLC2201B device, while lot sample testing is performed on the TLC2201A. For other noise test requirements, please contact the factory.

TYPICAL CHARACTERISTICS

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			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage vs Temperature	6 7
CMRR	Common-mode rejection ratio	vs Frequency	8
V_{OM}	Maximum peak output voltage	vs Output current vs Temperature	9 10
V_{OPP}	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OH}	High-level output voltage	vs Frequency vs Current vs Temperature	12 13 14
V_{OL}	Low-level output voltage	vs Output current vs Temperature	15 16
A_{VD}	Differential voltage amplification	vs Frequency vs Temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Temperature	19 20
I_{DD}	Supply current	vs Supply voltage vs Temperature	21 22
SR	Slew rate	vs Supply voltage vs Temperature	23 24
	Pulse response	Small-signal Large-signal	25, 26 27, 28
V_{NPP}	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	29 30
	Gain-bandwidth product	vs Supply voltage vs Temperature	31 32
ϕ_m	Phase margin	vs Supply voltage vs Temperature	33 34
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

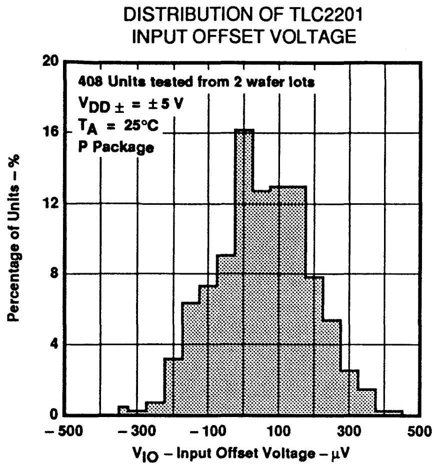


FIGURE 5

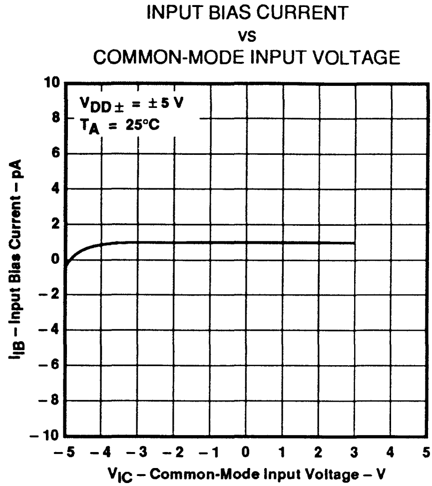


FIGURE 6

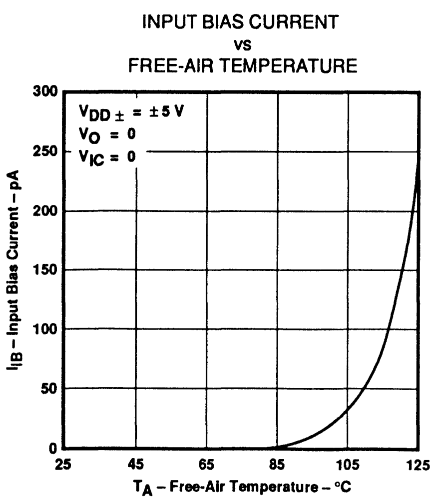


FIGURE 7

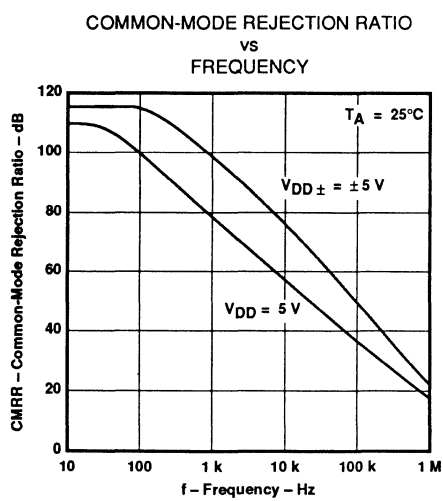


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

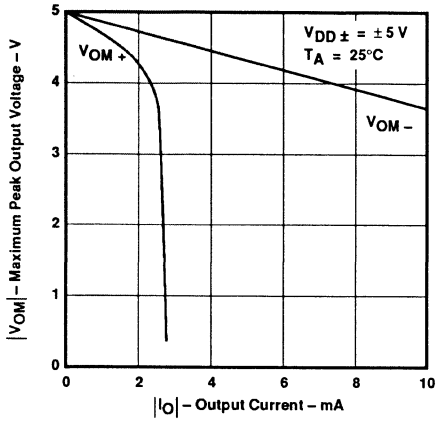


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

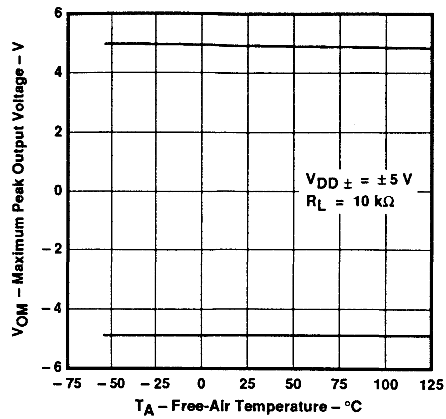


FIGURE 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

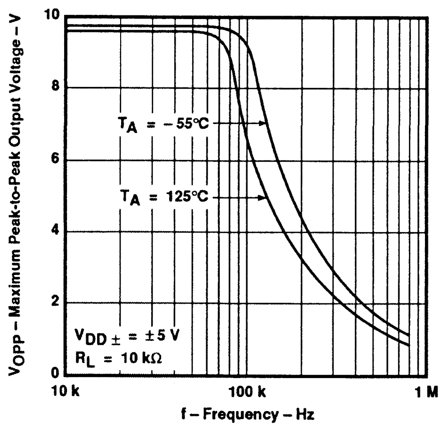


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

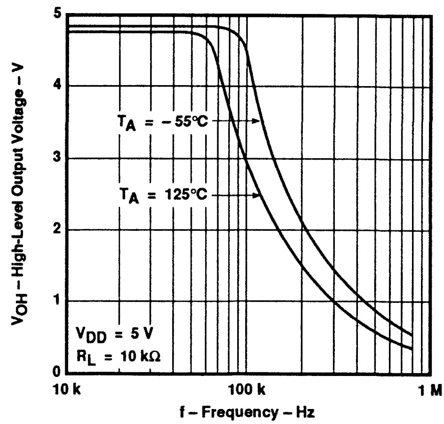


FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

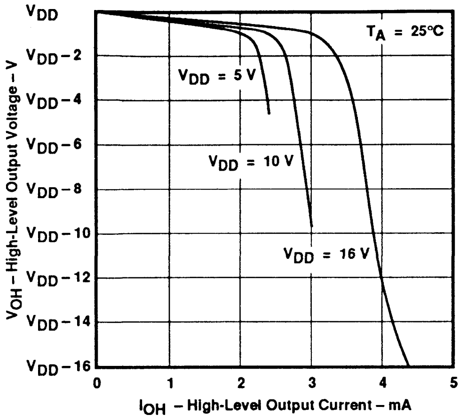


FIGURE 13

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

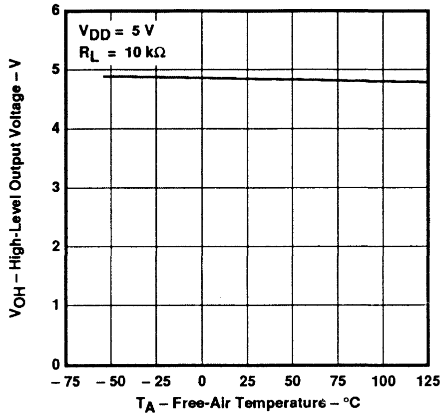


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

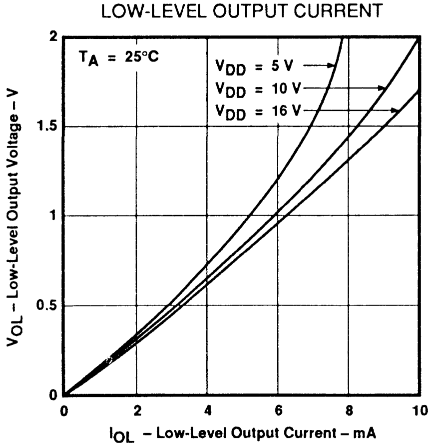


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

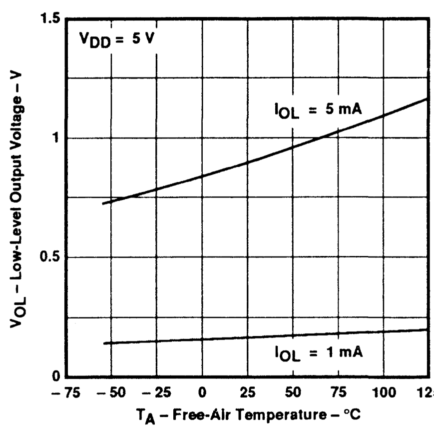


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

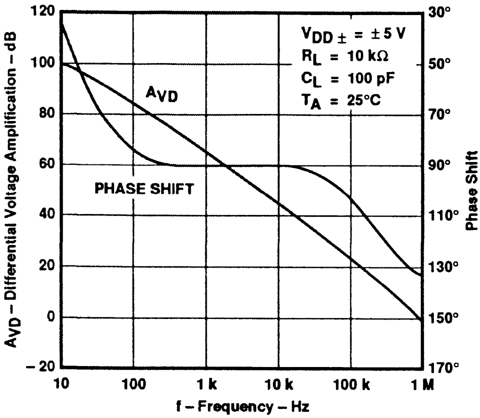


FIGURE 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

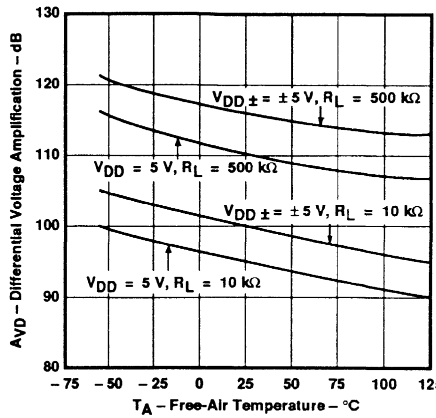


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

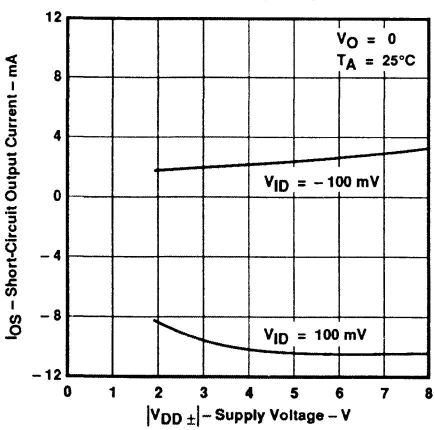


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

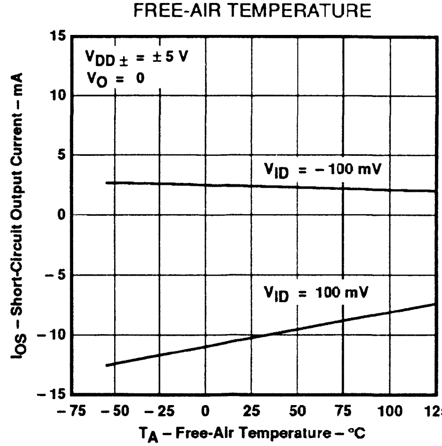


FIGURE 20

3 Operational Amplifiers

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

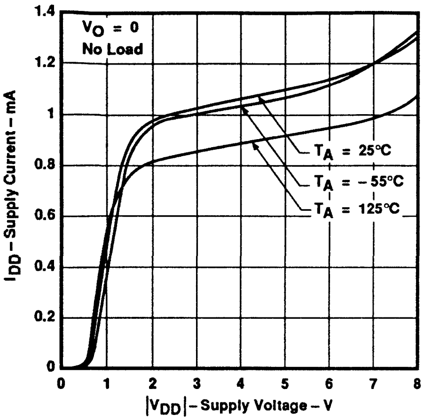


FIGURE 21

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

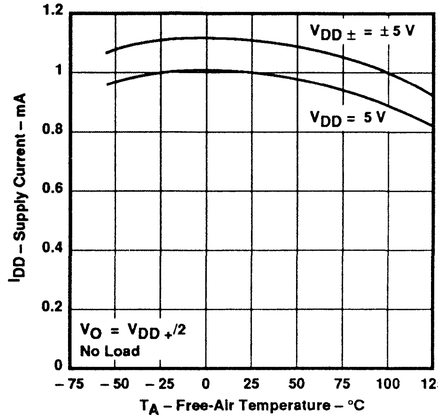


FIGURE 22

SLEW RATE
vs
SUPPLY VOLTAGE

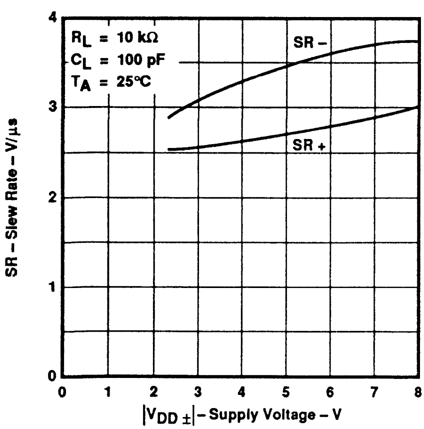


FIGURE 23

SLEW RATE
vs
FREE-AIR TEMPERATURE

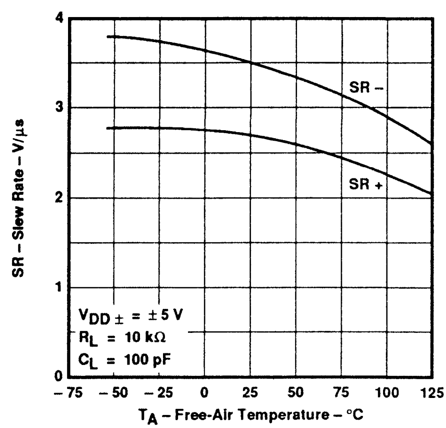


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

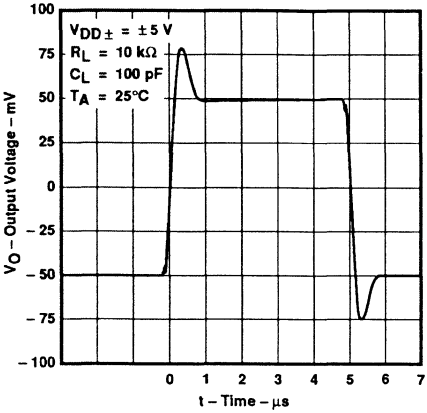


FIGURE 25

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

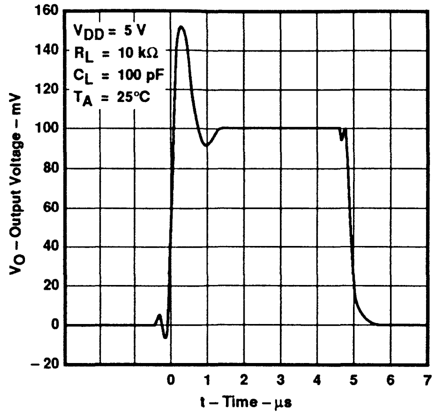


FIGURE 26

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

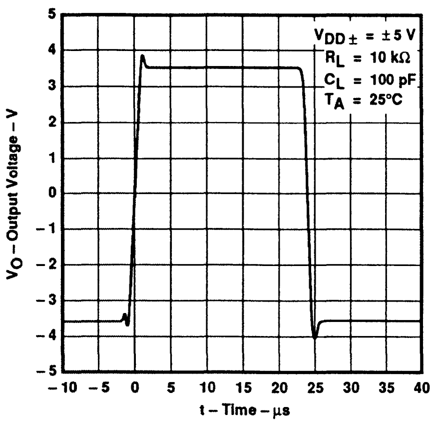


FIGURE 27

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

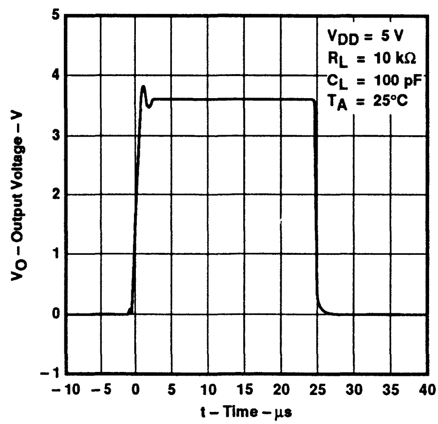


FIGURE 28

3
Operational Amplifiers

TYPICAL CHARACTERISTICS†

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

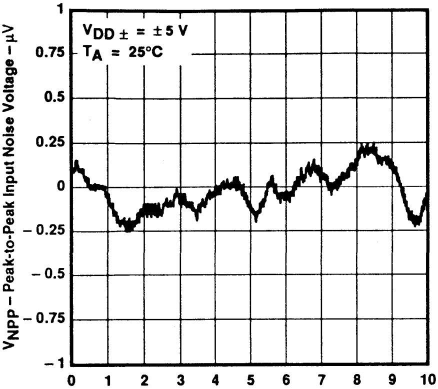


FIGURE 29

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

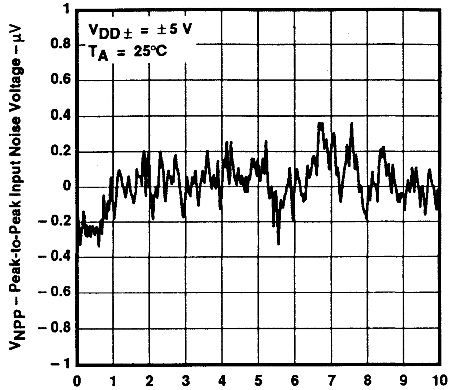


FIGURE 30

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

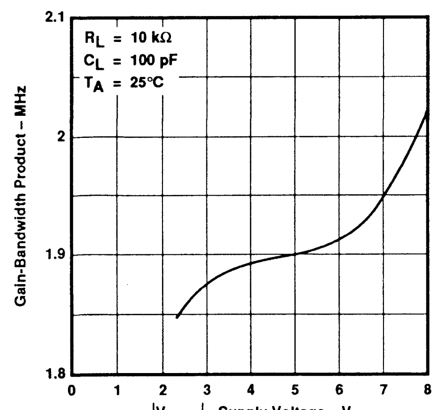


FIGURE 31

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

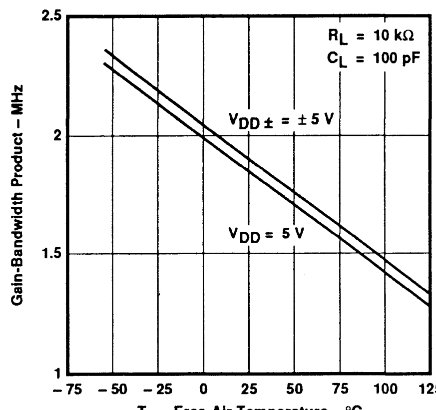


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

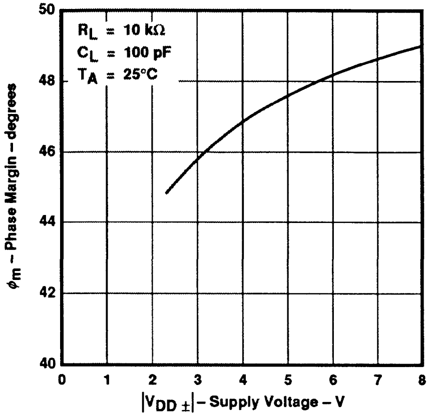


FIGURE 33

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

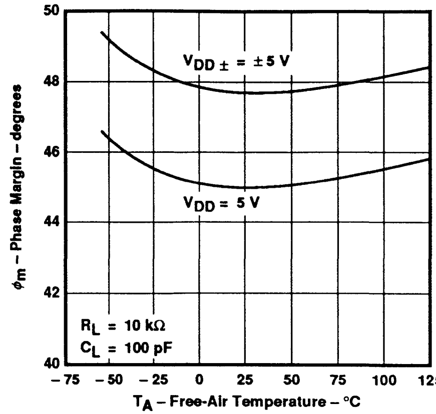


FIGURE 34

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

latchup avoidance

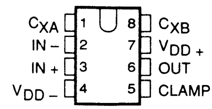
Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC2201, TLC2201A, and TLC2201B inputs and outputs are designed to withstand –100-mA surge currents without sustaining latchup; however, techniques reducing the chance of latchup should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

electrostatic discharge protection

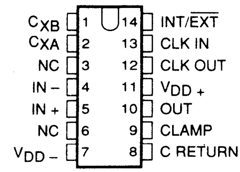
These devices use internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

- **Extremely Low Offset Voltage . . . 1 μV Max**
- **Extremely Low Change in Offset Voltage with Temperature . . . 0.003 μV/°C Typ**
- **Low Input Offset Current . . . 500 pA Max at T_A = −55°C to 125°C**
- **A_{VD} . . . 135 dB Min**
- **CMRR and k_{SVR} . . . 120 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation with External Capacitors Connected to V_{DD-}**

D008, JG, or P PACKAGE (TOP VIEW)



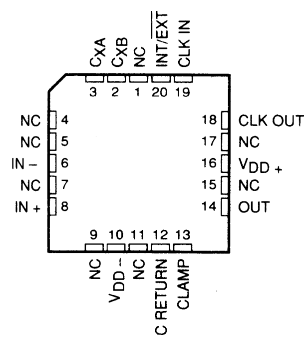
D014, J, or N PACKAGE (TOP VIEW)



description

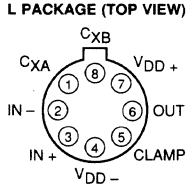
The TLC2652 and TLC2652A are high-precision chopper-stabilized operational amplifiers using Texas Instruments Advanced LinCMOS™ process. This process in conjunction with unique chopper-stabilization circuitry produces operational amplifiers whose performance matches or exceeds that of similar devices available today.

FK PACKAGE (TOP VIEW)



NC – No internal connection

L PACKAGE (TOP VIEW)



Pin 4 of the L package is in electrical contact with the case.

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE							
		8-PIN				14-PIN			20-PIN
		Small-Outline (D008)	Plastic DIP (P)	Ceramic DIP (JG)	Metal Can (L)	Small Outline (D014)	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	1 μV	TLC2652AC-8D	TLC2652ACP	TLC2652ACJG	TLC2652ACL	TLC2652AC-14D	TLC2652ACN	TLC2652ACJ	—
	3 μV	TLC2652C-8D	TLC2652CP	TLC2652CJG	TLC2652CL	TLC2652C-14D	TLC2652CN	TLC2652CJ	—
− 40°C to 85°C	1 μV	TLC2652AI-8D	TLC2652AIP	TLC2652AIJG	TLC2652AIL	TLC2652AI-14D	TLC2652AIN	TLC2652AIJ	—
	3 μV	TLC2652I-8D	TLC2652IP	TLC2652IJG	TLC2652IL	TLC2652I-14D	TLC2652IN	TLC2652IJ	—
− 55°C to 125°C	1 μV	TLC2652AM-8D	TLC2652AMP	TLC2652AMJG	TLC2652AML	TLC2652AM-14D	TLC2652AMN	TLC2652AMJ	TLC2652AMFK
	3 μV	TLC2652M-8D	TLC2652MP	TLC2652MJG	TLC2652ML	TLC2652M-14D	TLC2652MN	TLC2652MJ	TLC2652MFK

D008 and D014 packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC2652AC-8DR).

description (continued)

Chopper stabilization techniques make possible extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. In addition, low-frequency noise voltage is significantly reduced. This high precision, coupled with the extremely high input impedance of the CMOS input stage, makes the TLC2652 and TLC2652A an ideal choice for low-level signal processing applications such as strain gauges, thermocouples, and other transducer amplifiers. (For applications that require extremely low noise and higher usable bandwidth, use the TLC2654 or TLC2654A device, which has a chopping frequency of 10 kHz.)

The TLC2652 and TLC2652A input common-mode range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±1.9 V.

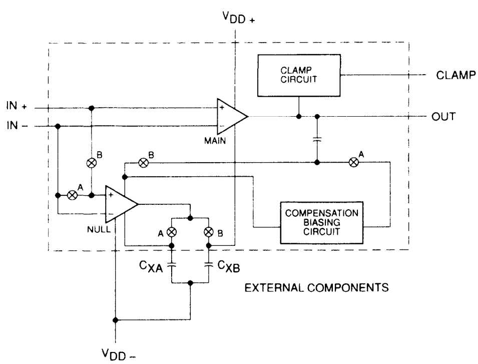
Two external capacitors are required for operation of the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is made accessible to allow the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold level of the TLC2652 and TLC2652A require no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques are used on the TLC2652 and TLC2652A to allow exceptionally fast overload recovery time. If desired, an output clamp pin is available to reduce the recovery time even further.

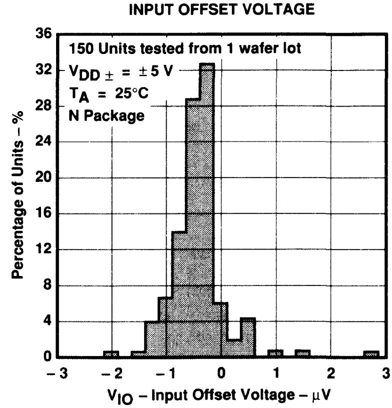
The device inputs and output are designed to withstand −100-mA surge currents without sustaining latchup. Additionally, the TLC2652 and TLC2652A incorporate internal ESD protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

functional block diagram



DISTRIBUTION OF TLC2652 INPUT OFFSET VOLTAGE



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . −8 V
Differential input voltage (see Note 2) . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . ±8 V
Voltage on CLK IN and INT/$\overline{EXT}$ pins . . . V_{DD-} to V_{DD-} +5.2 V
Input current, I_I (each input) . . . ±5 mA
Output current, I_O . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . Unlimited
Current into CLK IN and INT/$\overline{EXT}$ pins . . . ±5 mA
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . −55°C to 125°C
I-suffix . . . −40°C to 85°C
C-suffix . . . 0°C to 70°C
Storage temperature range . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, or L package . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	± 1.9		± 8	± 1.9		± 8	± 1.9		± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}		$V_{DD+} - 1.9$	V_{DD-}		$V_{DD+} - 1.9$	V_{DD-}		$V_{DD+} - 1.9$	V
Clock Input voltage	V_{DD-}		$V_{DD-} + 5$	V_{DD-}		$V_{DD-} + 5$	V_{DD-}		$V_{DD-} + 5$	V
Operating free-air temperature, T_A	− 55		125	− 40		85	0		70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AM			TLC2652M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.5	1		0.6	3	μV
			Full range			4			6	
α_{VIO}	Temperature coefficient of input offset voltage		−55°C to 125°C		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	135	150		120	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

† Full range is −55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2652AM MIN	TLC2652AM TYP	TLC2652AM MAX	TLC2652M MIN	TLC2652M TYP	TLC2652M MAX	UNIT
SR+	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/μs
			Full range	1.3			1.3			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.6			1.6			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		94			94		nV/√Hz
		f = 1 kHz	25°C		23			23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C							pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is − 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AI MIN	TLC2652AI TYP	TLC2652AI MAX	TLC2652I MIN	TLC2652I TYP	TLC2652I MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		0.5	1		0.6	3	μV
			Full range			2.95			4.95	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 3.1			– 5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 4 V, R_L = 10 kΩ	25°C	135	150		120	150		dB
			Full range	125			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	V_O = – 4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm}$ = ± 1.9 V to ± 8 V, V_O = 0, R_S = 50 Ω	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AI			TLC2652I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	2	2.8		2	2.8		V/μs
			Full range	1.4			1.4			
SR –	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94	140		94		nV/√Hz
		f = 1 kHz	25°C		23	35		23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C							pA/√Hz
	Gain-bandwidth product	f = 10 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ, $C_L = 100$ pF	25°C		48°			48°		

†Full range is – 40°C to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AC MIN	TLC2652AC TYP	TLC2652AC MAX	TLC2652C MIN	TLC2652C TYP	TLC2652C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.5	1		0.6	3	µV
			Full range			2.35			4.35	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.003	0.03		0.003	0.03	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	135	150		120	150		dB
			Full range	130			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 1.9$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2652AC MIN	TLC2652AC TYP	TLC2652AC MAX	TLC2652C MIN	TLC2652C TYP	TLC2652C MAX	UNIT
SR +	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.8		2	2.8		V/µs
			Full range	1.5			1.5			
SR −	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/µs
			Full range	1.8			1.8			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94	140		94		nV/√Hz
		f = 1 kHz	25°C		23	35		23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		µV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C							pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Normalized Input offset voltage	vs Chopping frequency	1
I_{IB}	Input bias current	vs Common-mode input voltage	2
		vs Chopping frequency	3
		vs Temperature	4
I_{IO}	Input offset current	vs Chopping frequency	5
		vs Temperature	6
	Clamp current	vs Output voltage	7
V_{OPP}	Maximum peak-to-peak output voltage swing	vs Frequency	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9, 10
		vs Temperature	11, 12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
	Gain-bandwidth product	vs Supply voltage	28
		vs Temperature	29
ϕ_m	Phase margin	vs Supply voltage	30
		vs Temperature	31
		vs Load capacitance	32
	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

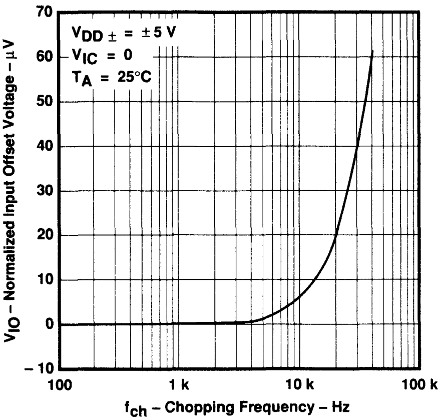


FIGURE 1

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

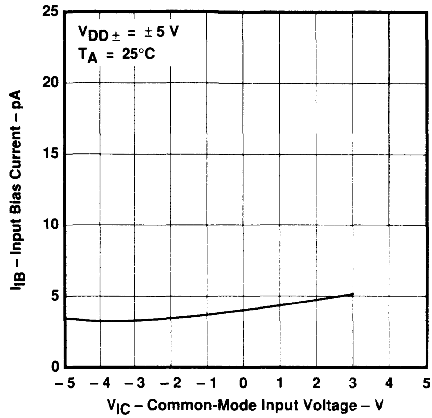


FIGURE 2

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

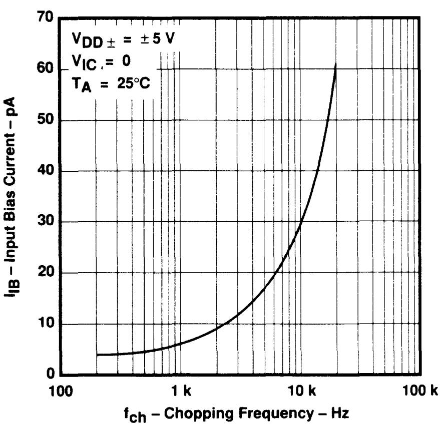


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

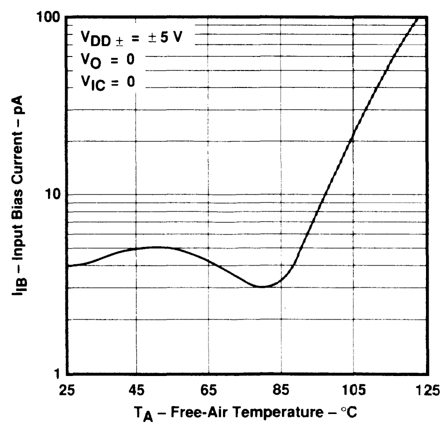


FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

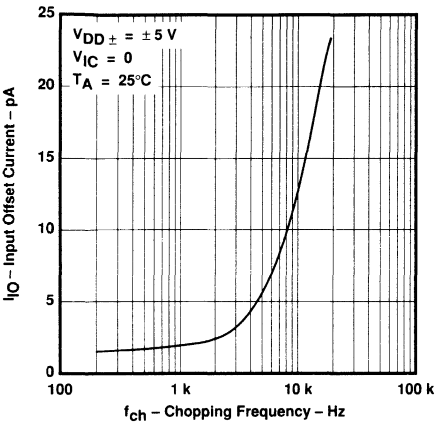


FIGURE 5

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

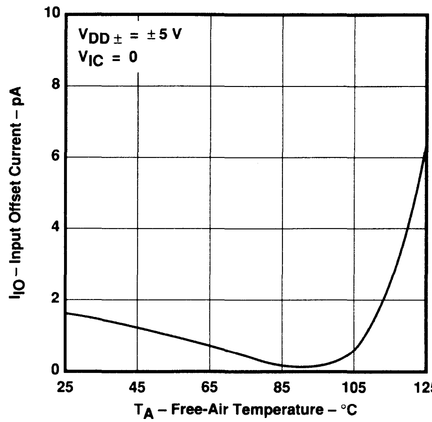


FIGURE 6

CLAMP CURRENT
vs
OUTPUT VOLTAGE

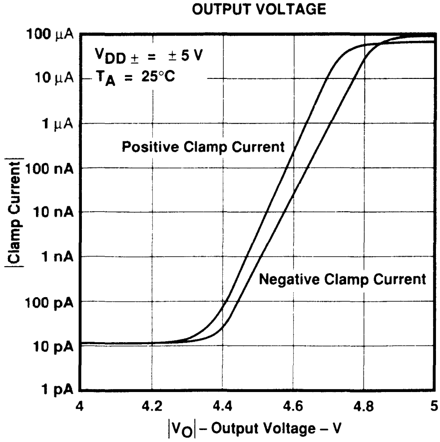


FIGURE 7

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

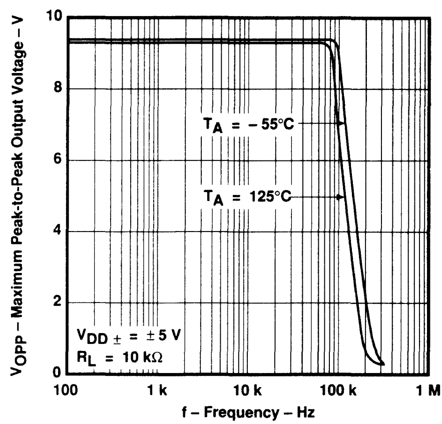


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

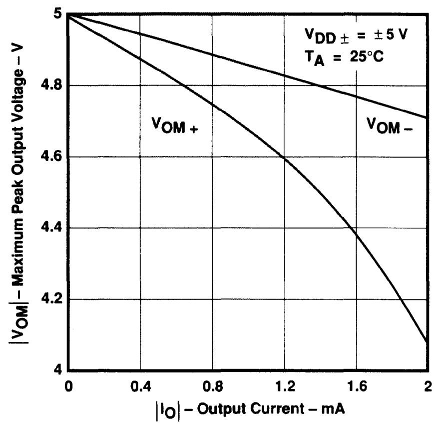


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

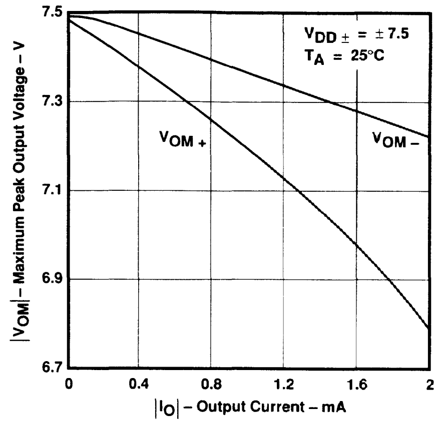


FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

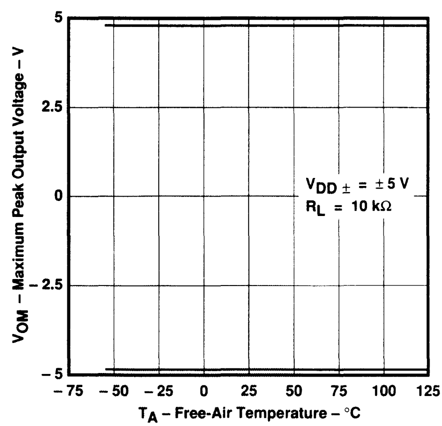


FIGURE 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

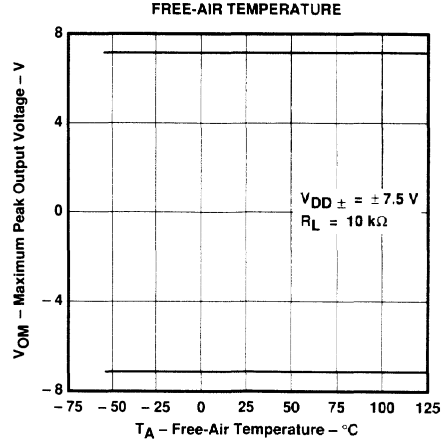


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

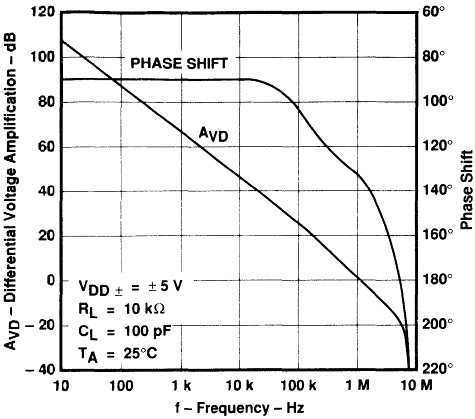


FIGURE 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

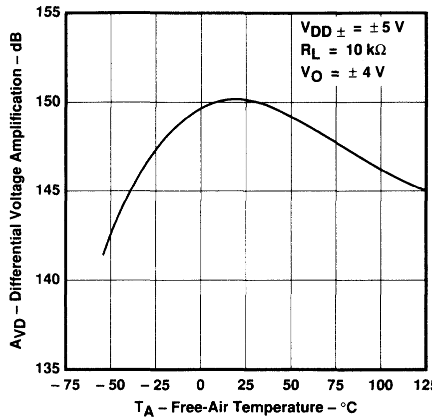


FIGURE 14

CHOPPING FREQUENCY vs SUPPLY VOLTAGE

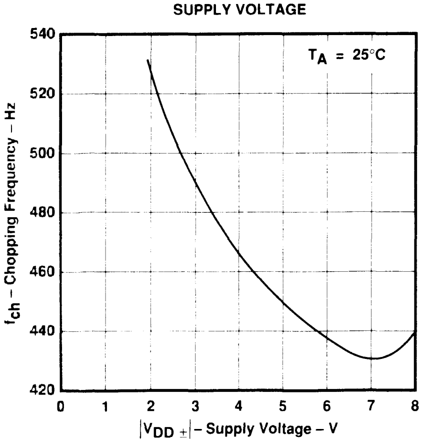


FIGURE 15

CHOPPING FREQUENCY vs FREE-AIR TEMPERATURE

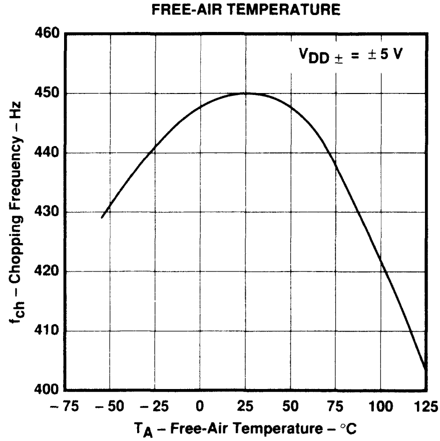


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

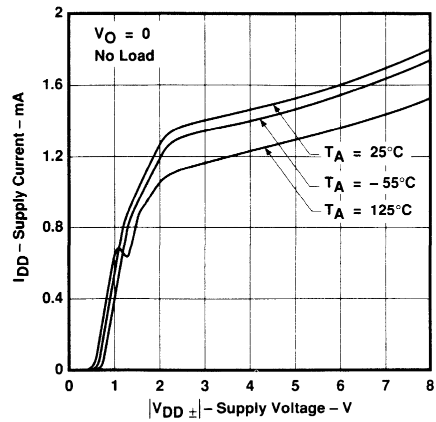


FIGURE 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

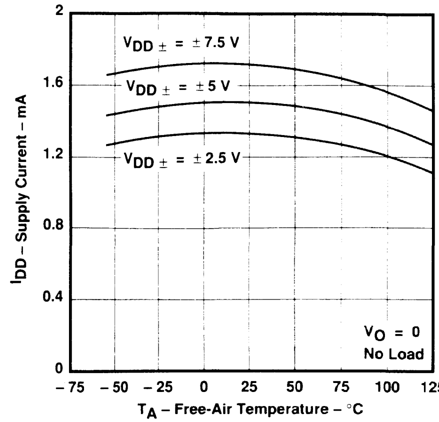


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

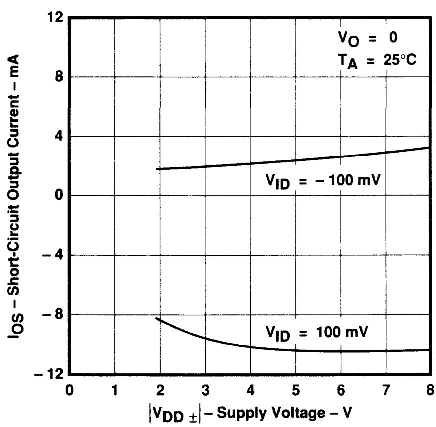


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

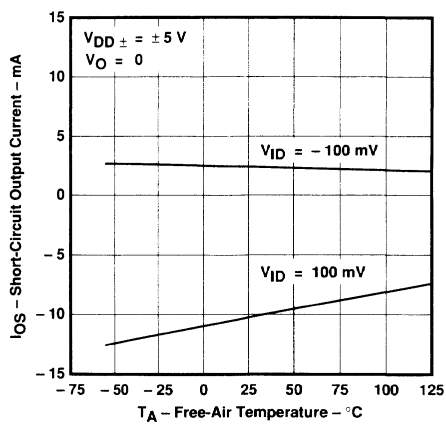


FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

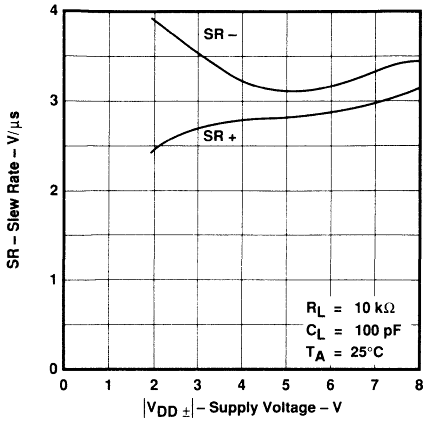


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

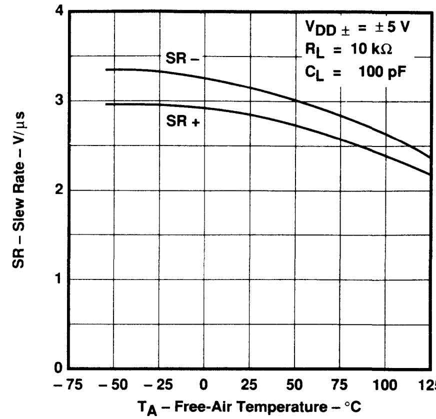


FIGURE 22

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

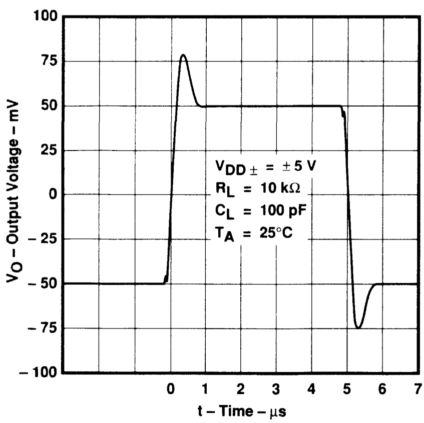


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

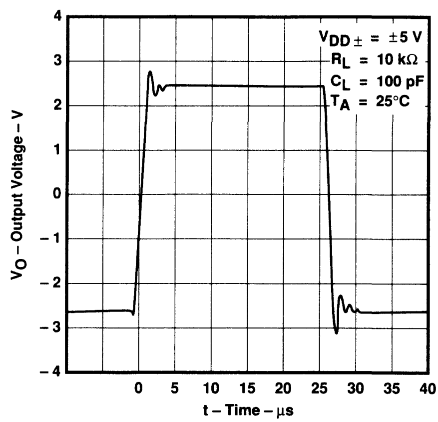


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

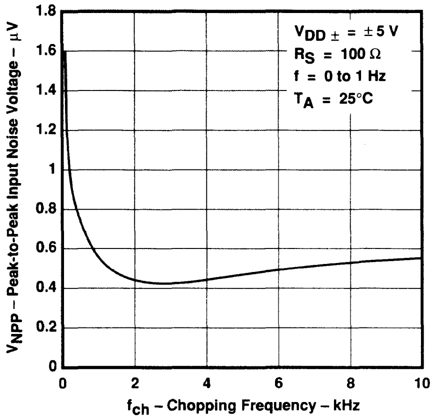


FIGURE 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

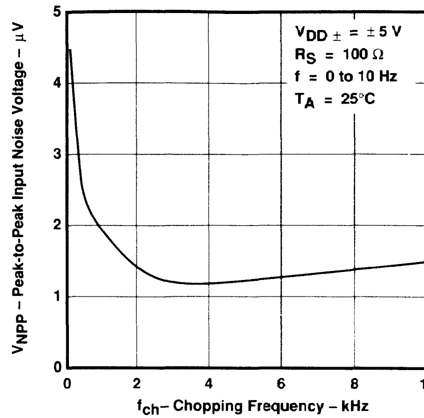


FIGURE 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

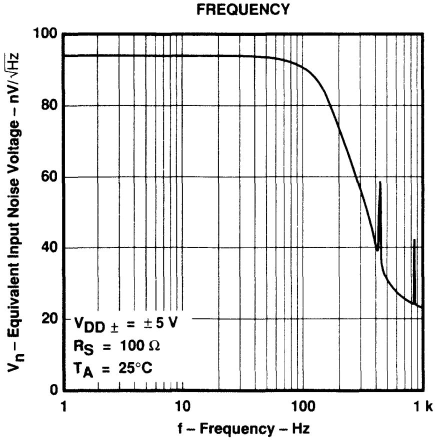


FIGURE 27

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

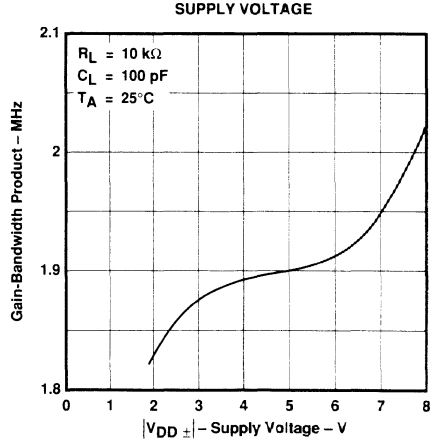


FIGURE 28

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

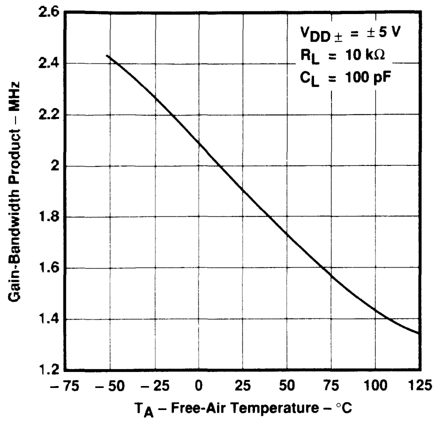


FIGURE 29

PHASE MARGIN vs SUPPLY VOLTAGE

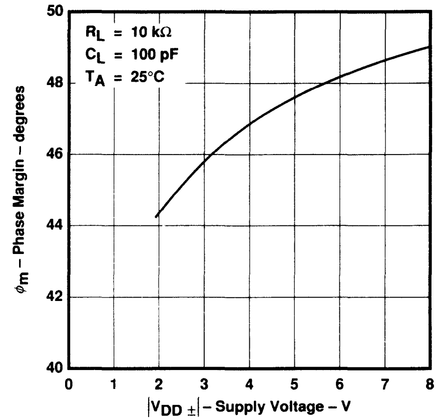


FIGURE 30

PHASE MARGIN vs FREE-AIR TEMPERATURE

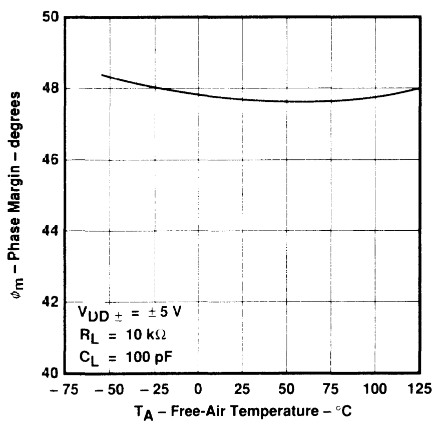


FIGURE 31

PHASE MARGIN vs LOAD CAPACITANCE

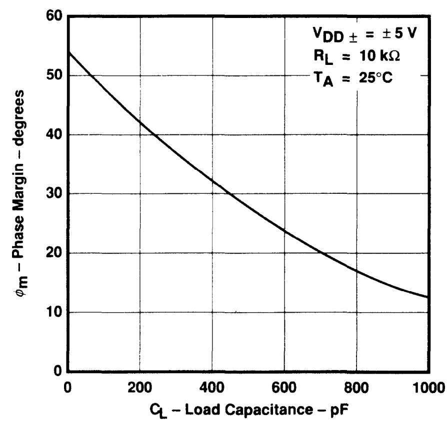


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

capacitor selection and placement

The two important factors to consider when selecting external capacitors C_{XA} and C_{XB} are leakage and dielectric absorption. Both factors can cause system degradation that can negate the performance advantages realized by using the TLC2652.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at $T_A = 125°C$. In addition, guardbands are recommended around the capacitor connections on both sides of the printed circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset voltage is needed, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2652 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 μF to 1 μF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin will cause degradation in the noise performance. This problem is eliminated on the TLC2652.

internal/external clock

The TLC2652 has an internal clock that sets the chopping frequency to a nominal value of 450 Hz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 450-Hz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. If this level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. When operating in the single-supply configuration, this feature allows the TLC2652 to be driven directly by 5-V TTL and CMOS logic. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin. The duty cycle of the external clock is not critical but should be kept between 30% and 60%.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2652, the nulling loop will attempt to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2652 is significantly faster than competitive products; however, if required, this time can be reduced further by using internal clamp circuitry accessible through the CLAMP pin.

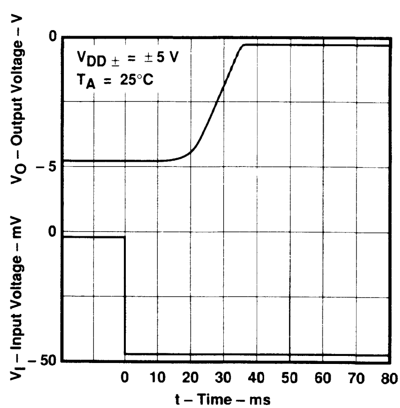


FIGURE 33. OVERLOAD RECOVERY

TYPICAL APPLICATION DATA

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2652 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 7), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage drift of the TLC2652, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.003 μV/°C typical of the TLC2652).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latchup avoidance

Because CMOS devices are susceptable to latchup due to their inherent parasitic thyristors, the TLC2652 inputs and output were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques to reduce the chance of latchup should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as is possible.

The current path established if latchup occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latchup occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2652 incorporates internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2652 on-chip control logic produces two dominant clock phases; a nulling phase and an amplifying phase. The term *chopper-stabilized* derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2652. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

TYPICAL APPLICATION DATA

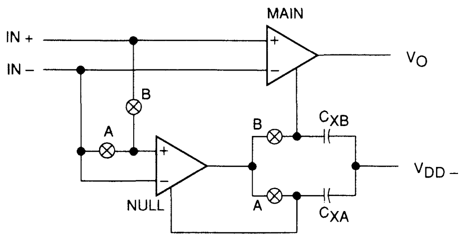


FIGURE 34. TLC2652 SIMPLIFIED BLOCK DIAGRAM

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power-supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process with its low-noise analog MOS transistors and patent-pending input stage design significantly reduces the input noise voltage.

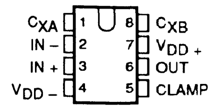
The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches.

As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2652 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

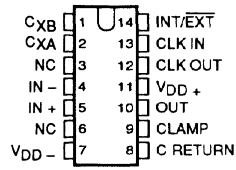
The TLC2652 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

- **Input Noise Voltage . . .**
  0.5 µV p-p Typ, f = 0 to 1 Hz
  1.5 µV p-p Typ, f = 0 to 10 Hz
  47 nV/√Hz Typ, f = 10 Hz
  13 nV/√Hz Typ, f = 1 kHz
- **High Chopping Frequency . . . 10 kHz Typ**
- **No Clock Noise Below 10 kHz**
- **No Intermodulation Error Below 5 kHz**
- **Low Input Offset Voltage . . . 10 µV Max**
- **Excellent Offset Voltage Stability with Temperature . . . 0.3 µV/°C Max**
- **A_{VD} . . . 135 dB Min**
- **CMRR . . . 110 dB Min**
- **k_{SVR} . . . 120 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation with External Capacitors Connected to V_{DD-}**

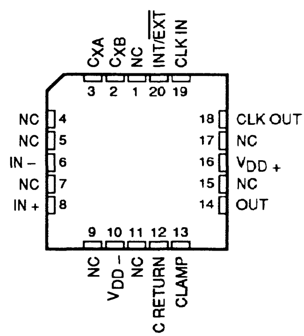
D008, JG, or P PACKAGE
(TOP VIEW)



D014, J, or N PACKAGE
(TOP VIEW)

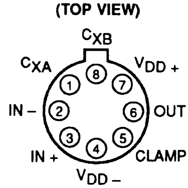


FK PACKAGE
(TOP VIEW)



NC – No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 of the L package is in electrical contact with the case

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE							
		8-PIN				14-PIN			20-PIN
		SMALL-OUTLINE (D008)	PLASTIC DIP (P)	CERAMIC DIP (JG)	METAL CAN (L)	SMALL-OUTLINE (D014)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	10 µV	TLC2654AC-8D	TLC2654ACP	TLC2654ACJG	TLC2654ACL	TLC2654AC-14D	TLC2654ACN	TLC2654ACJ	—
	20 µV	TLC2654C-8D	TLC2654CP	TLC2654CJG	TLC2654CL	TLC2654C-14D	TLC2654CN	TLC2654CJ	—
− 40°C to 85°C	10 µV	TLC2654AI-8D	TLC2654AIP	TLC2654AIJG	TLC2654AIL	TLC2654AI-14D	TLC2654AIN	TLC2654AIJ	—
	20 µV	TLC2654I-8D	TLC2654IP	TLC2654IJG	TLC2654IL	TLC2654I-14D	TLC2654IN	TLC2654IJ	—
− 55°C to 125°C	10 µV	TLC2654AM-8D	TLC2654AMP	TLC2654AMJG	TLC2654AML	TLC2654AM-14D	TLC2654AMN	TLC2654AMJ	TLC2654AMFK
	20 µV	TLC2654M-8D	TLC2654MP	TLC2654MJG	TLC2654ML	TLC2654M-14D	TLC2654MN	TLC2654MJ	TLC2654MFK

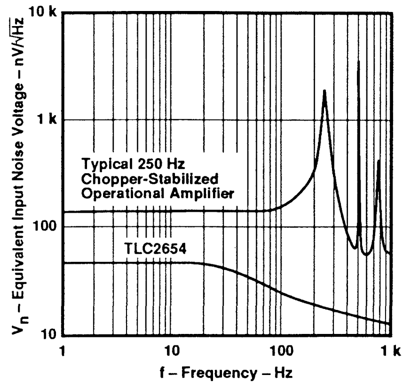
D008 and D014 packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC2654AC-8DR).

description

The TLC2654 and TLC2654A are low-noise chopper-stabilized operational amplifiers using the Advanced LinCMOS™ process. Combining this process with chopper stabilization circuitry makes possible excellent dc precision. In addition, circuit techniques have been added that give the TLC2654 and TLC2654A noise performance unsurpassed by similar devices.

Chopper stabilization techniques provide for extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. The high chopping frequency of the TLC2654 and TLC2654A provides excellent noise performance in a frequency spectrum from near dc to 10 kHz. In addition, intermodulation or aliasing error is eliminated from frequencies up to 5 kHz.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



This high dc precision and low noise, coupled with the extremely high input impedance of the CMOS input stage, make the TLC2654 and TLC2654A an ideal choice for a broad range of applications such as low-level low-frequency thermocouple amplifiers and strain gauges, as well as wide-bandwidth and subsonic circuits. (For applications requiring even greater dc precision, use the TLC2652 or TLC2652A device, which has a chopping frequency of 450 Hz.)

The TLC2654 and TLC2654A common-mode input voltage range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±2.3 V.

Two external capacitors are required to operate the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is accessible, allowing the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold of the TLC2654 and TLC2654A requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques used on the TLC2654 and TLC2654A allow exceptionally fast overload recovery time. An output clamp pin is available to reduce the recovery time further.

The device inputs and output are designed to withstand –100 mA surge currents without sustaining latchup. In addition, the TLC2654 and TLC2654A incorporate internal ESD protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) .... 8 V
Supply voltage, V_{DD-} (see Note 1) .... –8 V
Differential input voltage (see Note 2) .... ±16 V
Input voltage range, V_I (any input, see Note 1) .... ±8 V
Voltage on CLK IN and INT/$\overline{EXT}$ pins .... V_{DD-} to V_{DD-} + 5.2 V
Input current, I_I (each input) .... ±5 mA
Output current, I_O .... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Current into CLK IN and INT/$\overline{EXT}$ pins .... ±5 mA
Continuous total dissipation .... see Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix .... –55°C to 125°C
I-suffix .... –40°C to 85°C
C-suffix .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, or L package .... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

3

Operational Amplifiers

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	±2.3		±8	±2.3		±8	±2.3		±8	V
Common-mode input voltage, V_{IC}	V_{DD-}		V_{DD+} – 2.3	V_{DD-}		V_{DD+} – 2.3	V_{DD-}		V_{DD+} – 2.3	V
Clock input voltage	V_{DD-}		V_{DD-} + 5	V_{DD-}		V_{DD-} + 5	V_{DD-}		V_{DD-} + 5	V
Operating free-air temperature, T_A	–55		125	–40		85	0		70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AM			TLC2654M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		4	10		5	20	μV
			Full range			40			50	
α_{VIO}	Temperature coefficient of input offset voltage		−55°C to 125°C		0.004	0.3		0.004	0.3	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	135	155		120	155		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	125		110	125		dB
			Full range	115			105			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is −55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AM			TLC2654M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.1			1.1			
SR−	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		47			47		nV/√Hz
		f = 1 kHz	25°C		13			13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AI			TLC2654I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		4	10		5	20	µV
			Full range			30			40	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.004	0.3		0.004	0.3	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			200			200	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			200			200	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10$ kΩ, See Note 5	25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10$ kΩ	25°C	135	155		120	155		dB
			Full range	125			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100$ kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	125		110	125		dB
			Full range	120			110			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2654AI			TLC2654I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.2			1.2			
SR−	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		47	75		47		nV/√Hz
		f = 1 kHz	25°C		13	20		13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is − 40°C to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AC			TLC2654C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		4	10		5	20	μV
			Full range			24			34	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.004	0.3		0.004	0.3	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 10\ k\Omega$, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 10\ k\Omega$	25°C	135	155		120	155		dB
			Full range	130			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	$R_L = 100\ k\Omega$	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	$V_O = -4$ V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	$V_O = 0$, $V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.3$ V to ± 8 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	120	125		110	125		dB
			Full range	120			110			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AC			TLC2654C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		1.5	2		V/µs
			Full range	1.3			1.3			
SR –	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/µs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		47	75		47		nV/√Hz
		f = 1 kHz	25°C		13	20		13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		µV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
	Normalized input offset voltage	vs Chopping frequency	2
I_{IO}	Input offset current	vs Chopping frequency	3
		vs Temperature	4
I_{IB}	Input bias current	vs Common-mode voltage	5
		vs Chopping frequency	6
		vs Temperature	7
	Clamp current	vs Output voltage	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9
		vs Temperature	10
V_{OPP}	Maximum peak-to-peak output voltage swing	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	28
	Gain-bandwidth product	vs Supply voltage	29
		vs Temperature	30
	Phase margin	vs Supply voltage	31
		vs Temperature	32
ϕ_m	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2654
INPUT OFFSET VOLTAGE

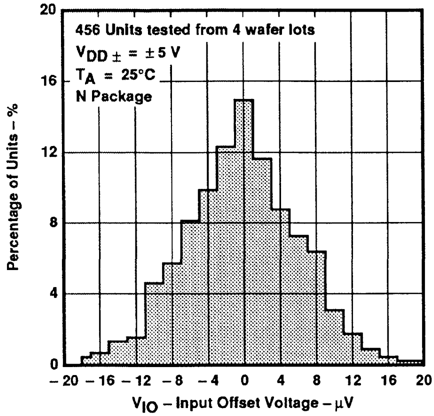


FIGURE 1

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

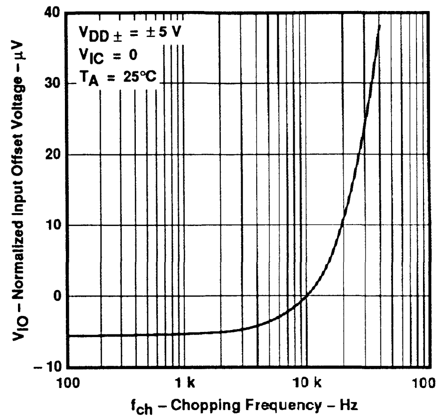


FIGURE 2

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

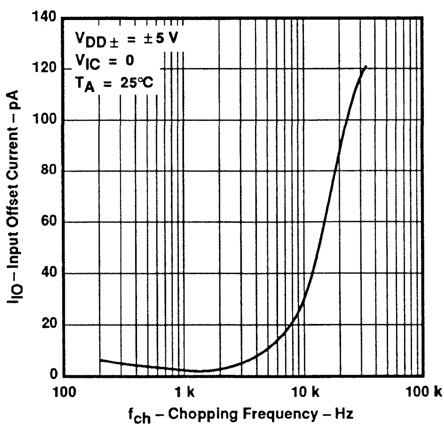


FIGURE 3

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

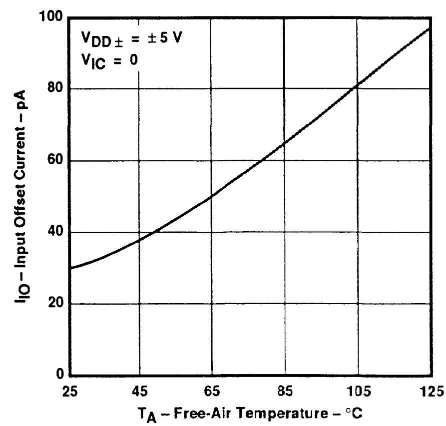


FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

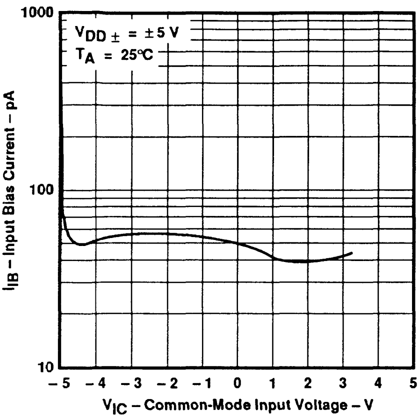


FIGURE 5

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

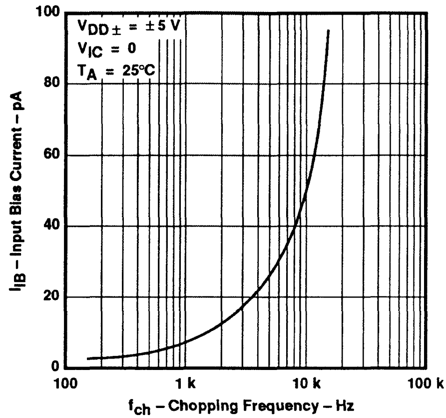


FIGURE 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

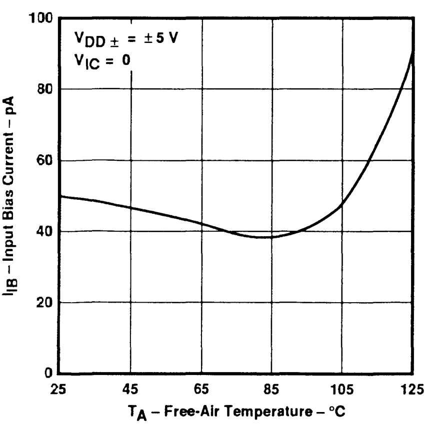


FIGURE 7

CLAMP CURRENT
vs
OUTPUT VOLTAGE

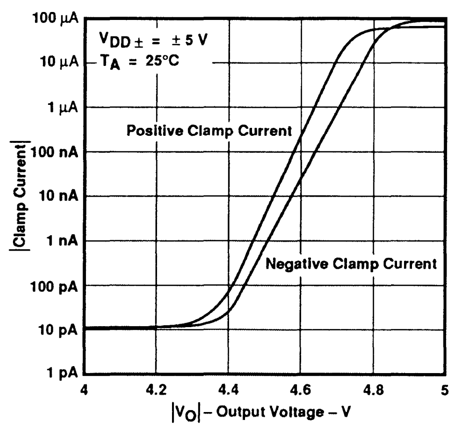


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

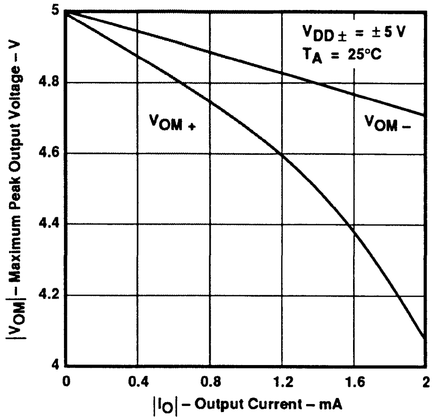


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

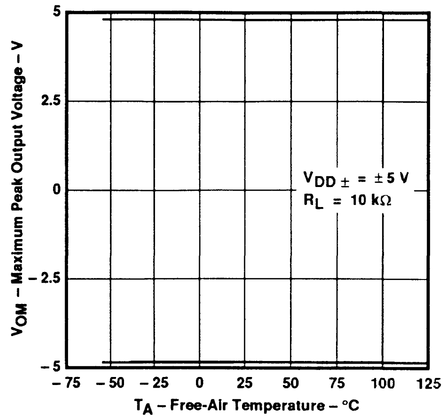


FIGURE 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

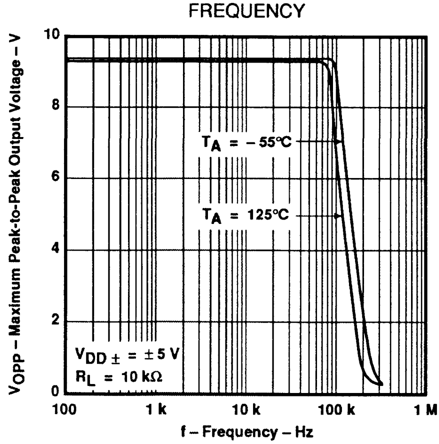


FIGURE 11

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

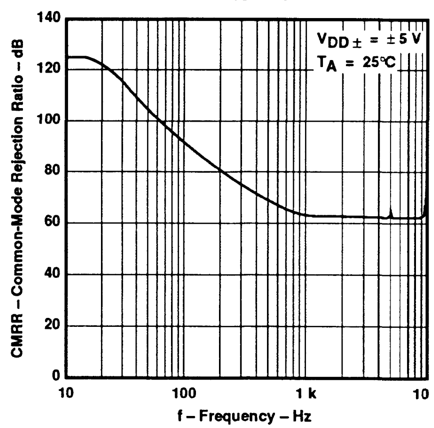


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

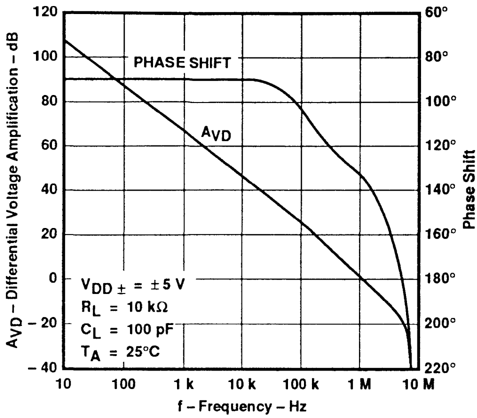


FIGURE 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

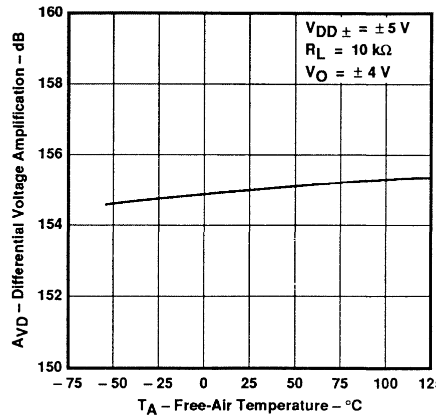


FIGURE 14

CHOPPING FREQUENCY vs SUPPLY VOLTAGE

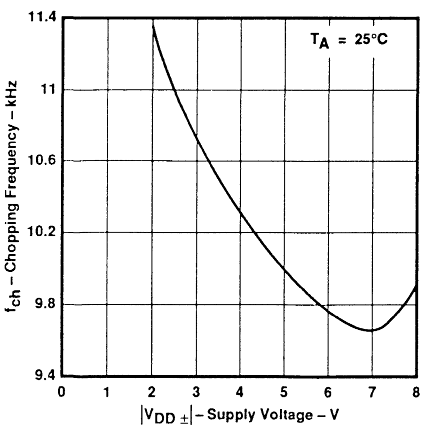


FIGURE 15

CHOPPING FREQUENCY vs FREE-AIR TEMPERATURE

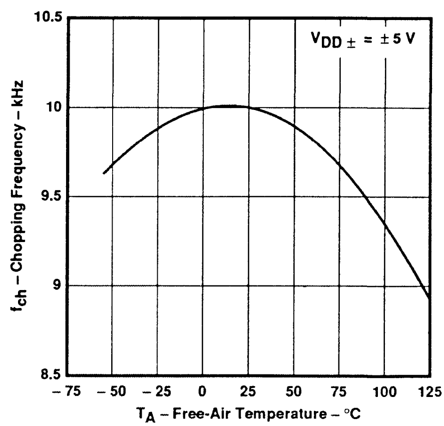


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

3 Operational Amplifiers

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

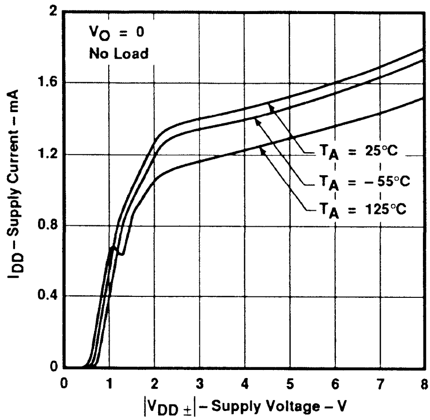


FIGURE 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

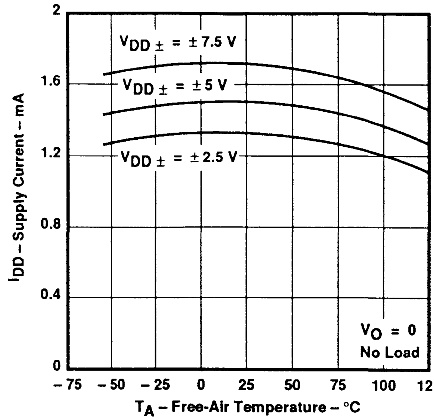


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

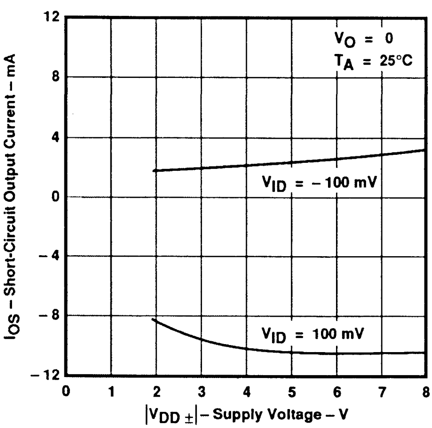


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

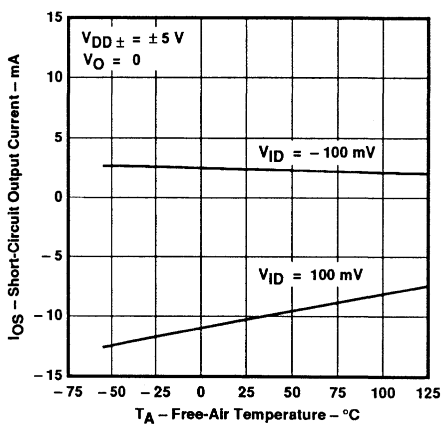


FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

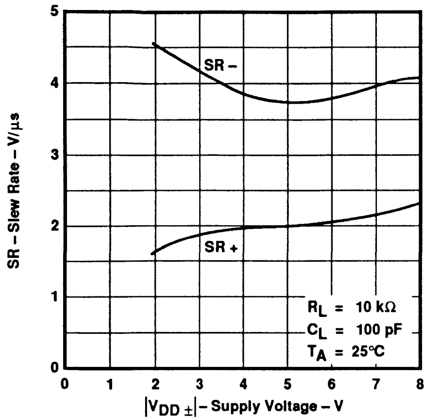


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

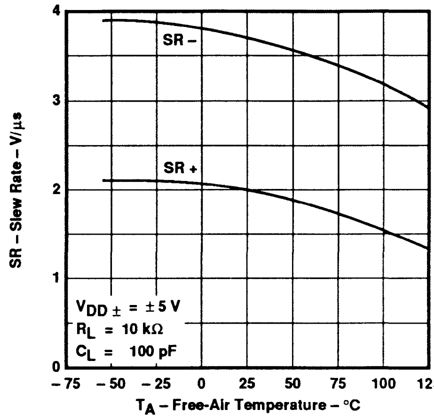


FIGURE 22

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

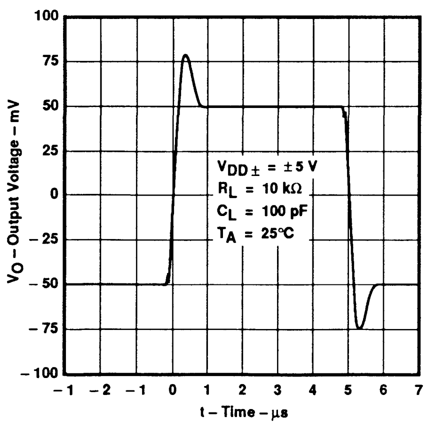


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

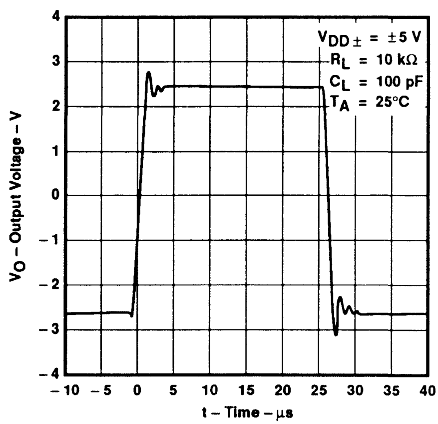


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

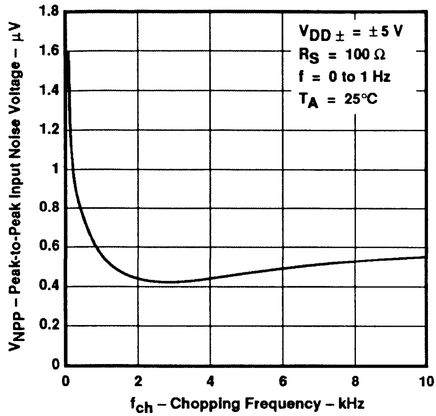


FIGURE 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

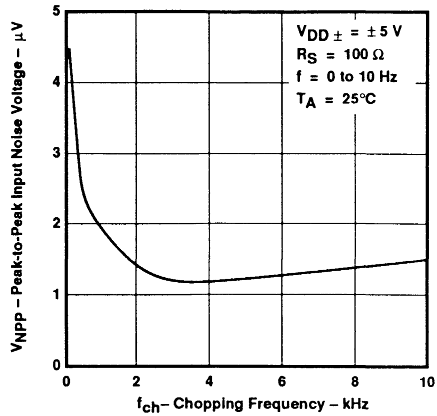


FIGURE 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

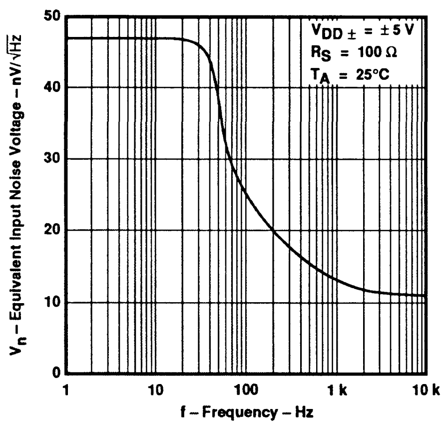


FIGURE 27

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

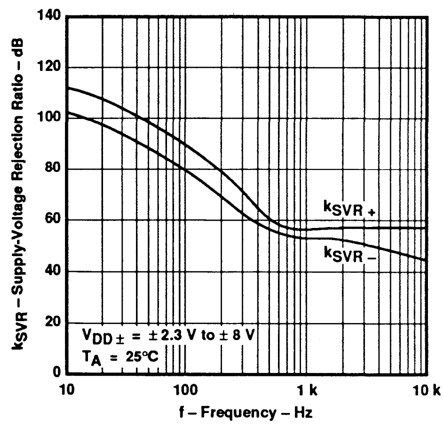


FIGURE 28

3

Operational Amplifiers

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

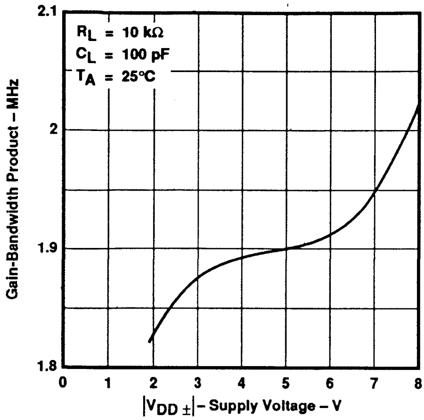


FIGURE 29

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

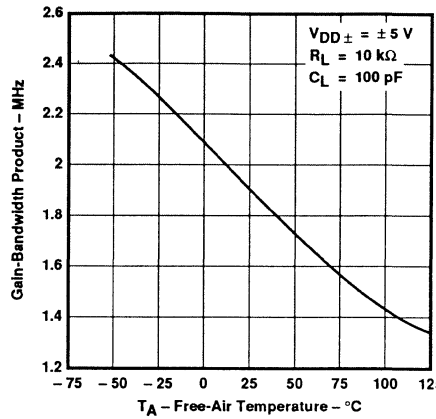


FIGURE 30

PHASE MARGIN
vs
SUPPLY VOLTAGE

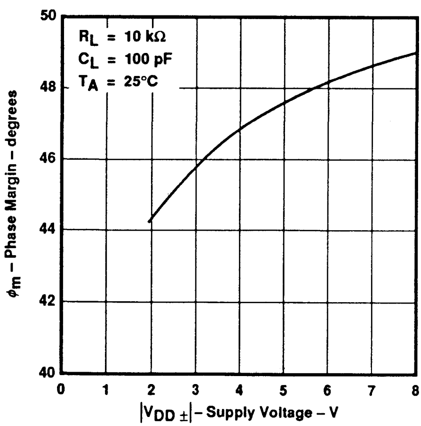


FIGURE 31

PHASE MARGIN
vs
LOAD CAPACITANCE

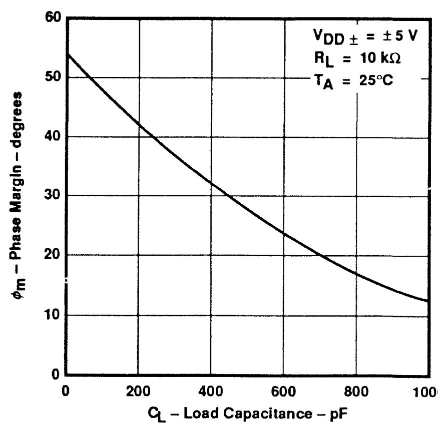


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

capacitor selection and placement

Leakage and dielectric absorption are the two important factors to consider when selecting external capacitors C_{XA} and C_{XB}. Both factors can cause system degradation negating the performance advantages realized by using the TLC2654.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guardbands around the capacitor connections on both sides of the printed circuit board are recommended to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input offset voltage, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2654 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin causes degradation in noise performance, a problem that is eliminated on the TLC2654.

internal/external clock

The TLC2654 has an internal clock that sets the chopping frequency to a nominal value of 10 kHz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 10-kHz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. This allows the TLC2654 to be driven directly by 5-V TTL and CMOS logic when operating in the single-supply configuration. If this 5-V level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2654, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2654 is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through the CLAMP pin.

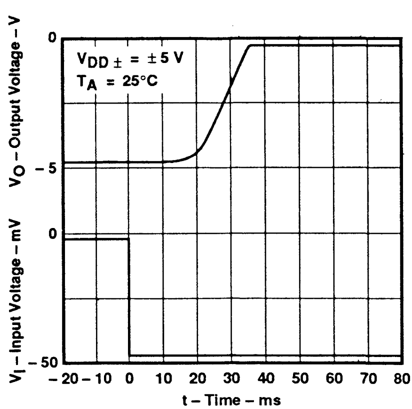


FIGURE 33. OVERLOAD RECOVERY

TYPICAL APPLICATION DATA

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2654 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 8), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the TLC2654, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-µV/°C typical of the TLC2654).

To help minimize thermoelectric effects, careful attention should be paid to componet selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latchup avoidance

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC2654 inputs and output are designed to withstand −100-mA surge currents without sustaining latchup; however, techniques to reduce the chance of latchup should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by using decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latchup occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2654 incorporates internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2654 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2654 on-chip control logic produces two dominant clock phases – a nulling phase and an amplifying phase. The term "chopper-stabilized" derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2654. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input

TYPICAL APPLICATION DATA

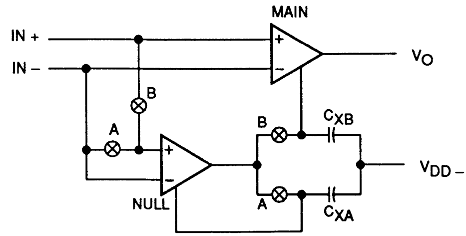


FIGURE 34. TLC2654 SIMPLIFIED BLOCK DIAGRAM

node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2654 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

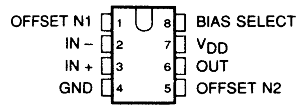
The TLC2654 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

The primary limitation on ac performance is the chopping frequency. As the input signal frequency approaches the chopper's clock frequency, intermodulation (or aliasing) errors result from the mixing of these frequencies. To avoid these error signals, the input frequency must be less than half the clock frequency. Most choppers available today limit the internal chopping frequency to less than 500 Hz in order to eliminate errors due to the charge imbalancing phenomenon mentioned previously. However, to avoid intermodulation errors on a 500 Hz chopper, the input signal frequency must be limited to less than 250 Hz. The TLC2654 removes this restriction on ac performance by using a 10-kHz internal clock frequency. This high chopping frequency allows amplification of input signals up to 5 kHz without errors due to intermodulation and greatly reduces low-frequency noise.

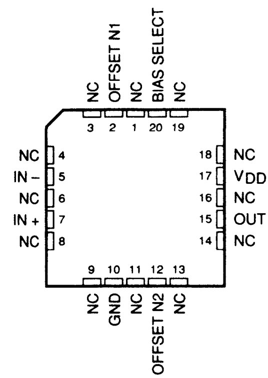
NOVEMBER 1987

- **Input Offset Voltage Drift Typically 0.1 μV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise . . . 25 nV √Hz Typically at f = 1 kHz (High-Bias Mode)**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC271 operational amplifier combines a wide range of input offset voltage grades with low offset voltage drift and high input impedance. In addition, the TLC271 offers a bias select mode which allows the user to select the best combination of power dissipation and AC performance for a particular application. These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	2 mV	TLC271BCD	TLC271BCP	TLC271BCJG	——
	5 mV	TLC271ACD	TLC271ACP	TLC271ACJG	——
	10 mV	TLC271CD	TLC271CP	TLC271CJG	——
– 40°C to 85°C	2 mV	TLC271BID	TLC271BIP	TLC271BIJG	——
	5 mV	TLC271AID	TLC271AIP	TLC271AIJG	——
	10 mV	TLC271ID	TLC271IP	TLC271IJG	——
– 55°C to 125°C	10 mV	——	——	TLC271MJG	TLC271MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC271CDR).

DEVICE FEATURES Typical at V_{DD} = 5 V, T_A = 25°C	BIAS-SELECT MODE			UNIT
	HIGH	MEDIUM	LOW	
P_D	3375	525	50	μW
SR	3.6	0.4	0.03	V/μs
V_n	25	32	68	nV/√Hz
B_1	1.7	0.5	0.09	MHz
A_{VD}	23	170	480	V/mV

TEXAS INSTRUMENTS

description (continued)

Using the bias select option, these cost-effective devices can be "programmed" to span a wide range of applications which previously required BiFET, NFET or bipolar technology. Three offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC271 (10mV) to the TLC271B (2mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and output are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC271 incorporates internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

bias select feature

The TLC271 offers a bias select feature which allows the user to select any one of three bias levels, depending on the level of performance desired. The trade-offs between bias levels involve AC performance and power dissipation (see Figure 1).

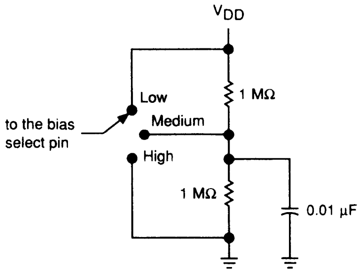
TYPICAL PARAMETER VALUES T_A = 25°C, V_{DD} = 5 V		MODE			UNITS
		HIGH-BIAS R_L = 10 kΩ	MEDIUM-BIAS R_L = 100 kΩ	LOW-BIAS R_L = 1 MΩ	
P_D	Power dissipation	3.4	0.5	0.05	mW
SR	Slew rate	3.6	0.4	0.03	V/μs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	1.7	0.5	0.09	MHz
ϕ_m	Phase margin	46°	40°	34°	
A_{VD}	Large-signal differential voltage amplification	23	170	480	V/mV

FIGURE 1. EFFECT OF BIAS SELECTION ON PERFORMANCE

bias selection

Bias selection is achieved by connecting the bias select pin to one of three voltage levels (see Figure 2). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated in Figure 2. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.

bias selection (continued)



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to V_{DD} − 1 V
HIGH	GND

FIGURE 2. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

high-bias mode

In the high-bias mode, the TLC271 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices, but at only a fraction of the power dissipation. Unity-gain bandwidth is typically greater than 1 MHz.

medium-bias mode

The TLC271 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices, but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

In the low-bias mode, the TLC271 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

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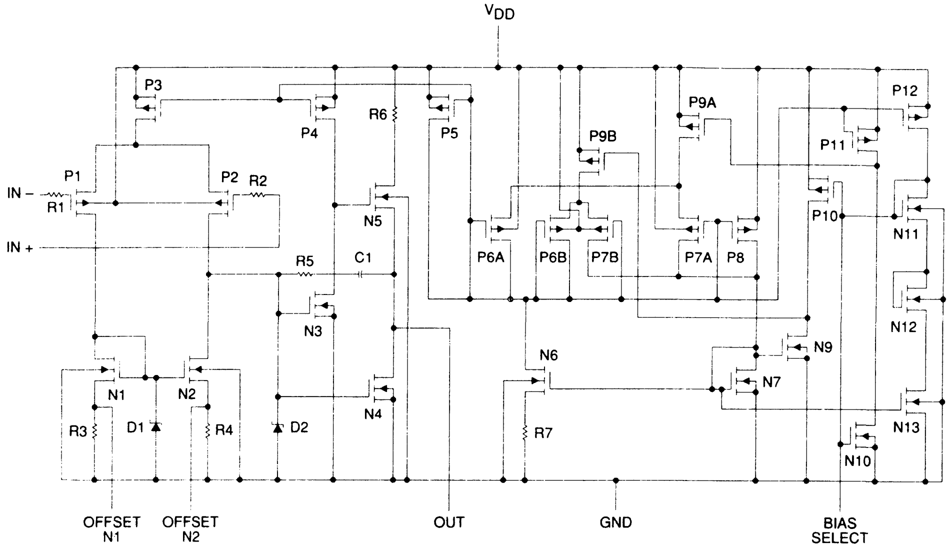
equivalent schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2)		18 V
Differential input voltage (see Note 3)		± V_{DD}
Input voltage range, V_I (any input)		– 0.3 V to V_{DD}
Input current, I_I		± 5 mA
Output current, I_O		± 30 mA
Duration of short-circuit current at (or below) 25°C (see Note 4)		Unlimited
Continuous total dissipation		See Dissipation Rating Table
Operating free-air temperature, T_A:	C-suffix types	0°C to 70°C
	I-suffix types	– 40°C to 85°C
	M-suffix types	– 55°C to 125°C
Storage temperature range		– 65°C to 150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package		300°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds: D and P package		260°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				70°C	3	3.8		7.8	8.4		
				0°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				70°C		0	50		0	50	
				0°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 7	25°C	5	23		10	36		V/mV
				70°C	4	20		7.5	32		
				0°C	4	27		7.5	42		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	80		65	85		dB
				70°C	60	85		60	88		
				0°C	60	84		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				70°C	60	96		60	96		
				0°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		675	1600		950	2000	μA
				70°C		575	1300		750	1700	
				0°C		775	1800		1125	2200	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.34	2		0.39	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				85°C	3	3.8		7.8	8.5		
				−40°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				85°C		0	50		0	50	
				−40°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 7	25°C	5	23		10	36		V/mV
				85°C	3.5	19		7	31		
				−40°C	3.5	32		7	46		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	80		65	85		dB
				85°C	60	86		60	88		
				−40°C	60	81		60	87		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				85°C	60	96		60	96		
				−40°C	60	92		60	92		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		675	1600		950	2000	μA
				85°C		525	1200		725	1600	
				−40°C		950	2200		1375	2500	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		M-SUFFIX TYPES V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		2.1			2.2		μV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
			125°C	3	3.8		7.8	8.4		
			−55°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			125°C		0	50		0	50	
			−55°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 7	25°C	5	23		10	36		V/mV
			125°C	3.5	16		7	27		
			−55°C	3.5	35		7	50		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C	65	80		65	85		dB
			125°C	60	84		60	86		
			−55°C	60	81		60	87		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
			125°C	60	97		60	97		
			−55°C	60	90		60	90		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current	No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		675	1600		950	2000	μA
			125°C		475	1100		625	1400	
			−55°C		1000	2500		1475	3000	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		3.6		V/μs
				70°C		3		
				0°C		3.9		
			V_{IPP} = 2.5 V	25°C		2.9		
				70°C		2.5		
				0°C		3.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		320		kHz
				70°C		260		
				0°C		340		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		1.7		MHz
				70°C		1.3		
				0°C		2		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		46°		
				70°C		43°		
				0°C		47°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				70°C		4.3		
				0°C		5.9		
			V_{IPP} = 5.5 V	25°C		4.6		
				70°C		3.8		
				0°C		5.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		200		kHz
				70°C		140		
				0°C		220		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		2.2		MHz
				70°C		1.8		
				0°C		2.5		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		49°		
				70°C		46°		
				0°C		50°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		3.6		V/μs
				85°C		2.8		
				−40°C		4.5		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
				−40°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		320		kHz
				85°C		250		
				−40°C		380		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		1.7		MHz
				85°C		1.2		
				−40°C		2.6		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		46°		
				85°C		43°		
				−40°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				85°C		4		
				−40°C		6.7		
			V_{IPP} = 5.5 V	25°C		4.6		
				85°C		3.5		
				−40°C		5.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		200		kHz
				85°C		130		
				−40°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		2.2		MHz
				85°C		1.7		
				−40°C		3.1		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		49°		
				85°C		46°		
				−40°C		52°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		3.6		V/μs
				125°C		2.3		
				− 55°C		4.7		
			V_{IPP} = 2.5 V	25°C		2.9		
				125°C		2		
				− 55°C		3.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		320		kHz
				125°C		230		
				− 55°C		400		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		1.7		MHz
				125°C		1.1		
				− 55°C		2.9		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		46°		
				125°C		41°		
				− 55°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				125°C		3.1		
				− 55°C		7.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				125°C		2.7		
				− 55°C		6.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 99		25°C		200		kHz
				125°C		110		
				− 55°C		280		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		2.2		MHz
				125°C		1.6		
				− 55°C		3.4		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		49°		
				125°C		44°		
				− 55°C		52°		

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

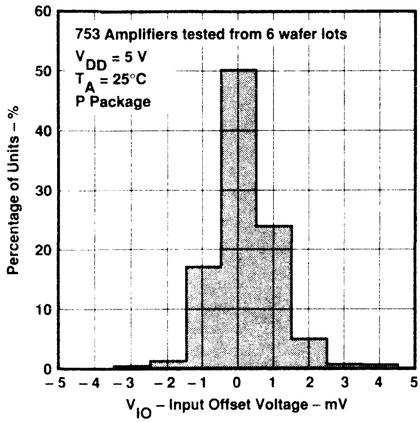


FIGURE 3

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

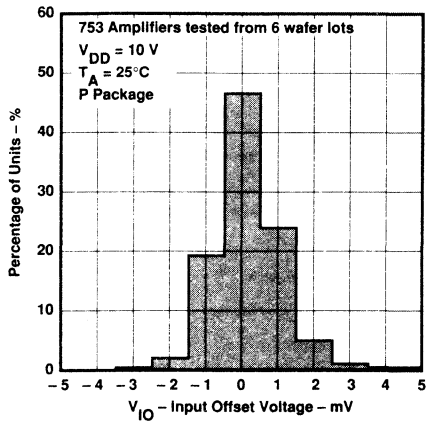


FIGURE 4

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

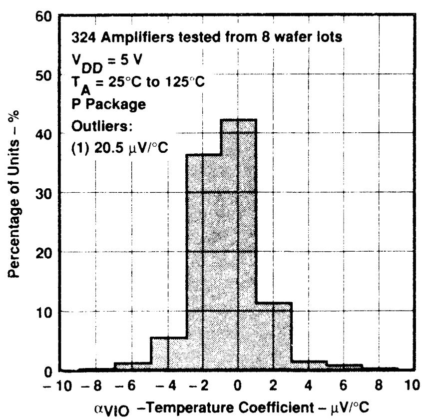


FIGURE 5

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

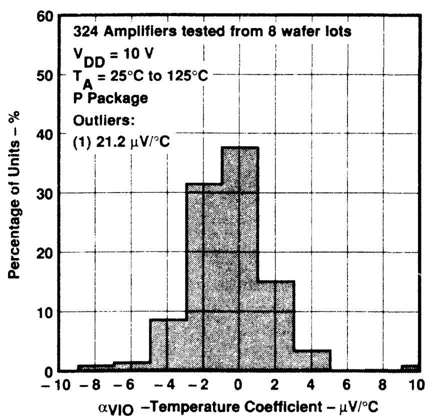


FIGURE 6

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

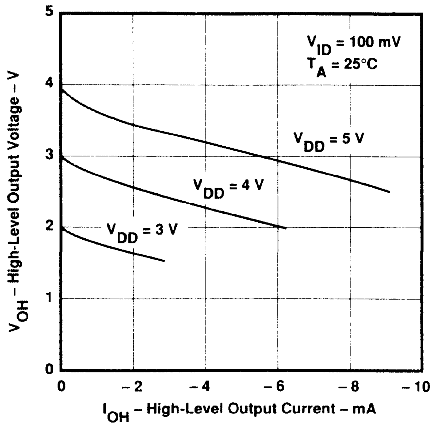


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

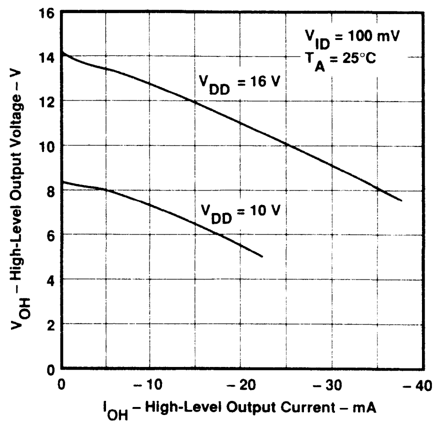


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

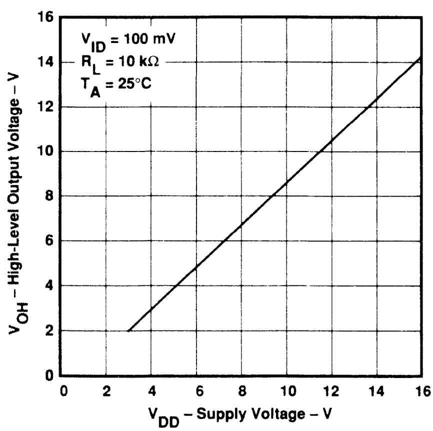


FIGURE 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

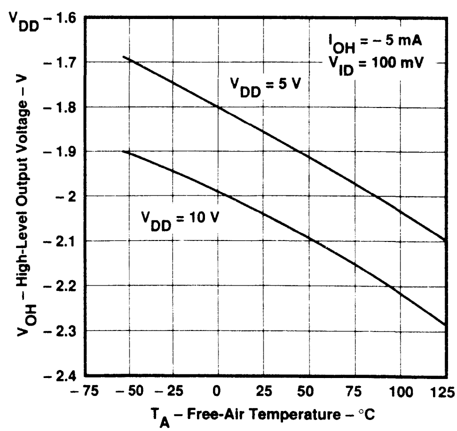


FIGURE10

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

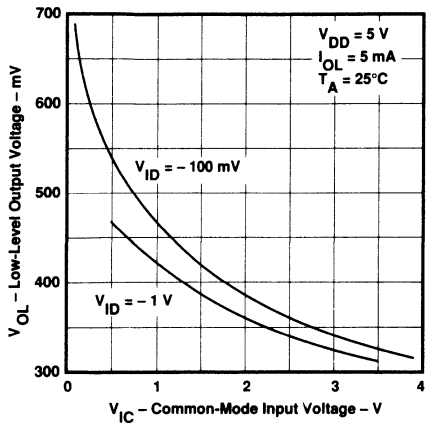


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

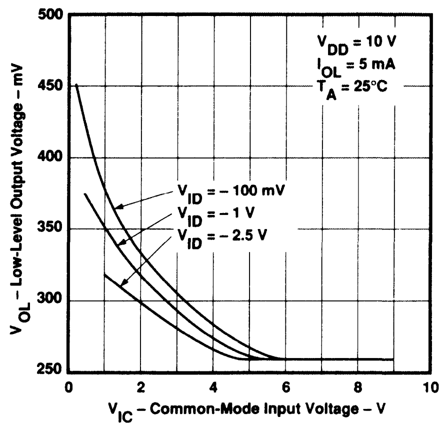


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

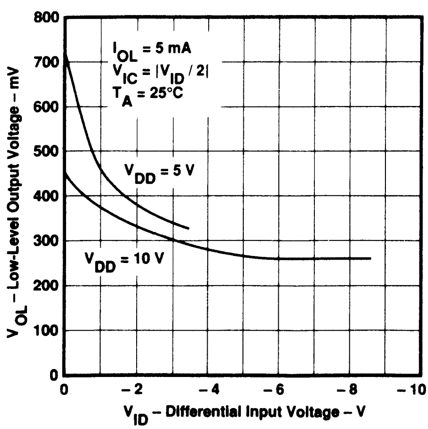


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

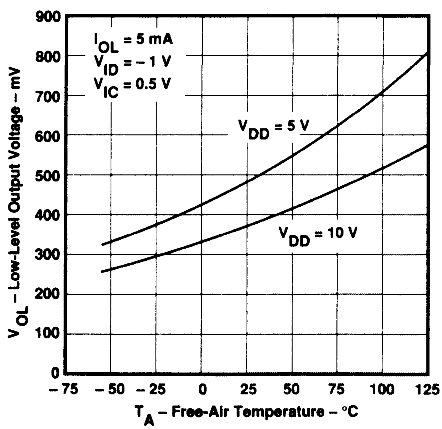


FIGURE 14

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

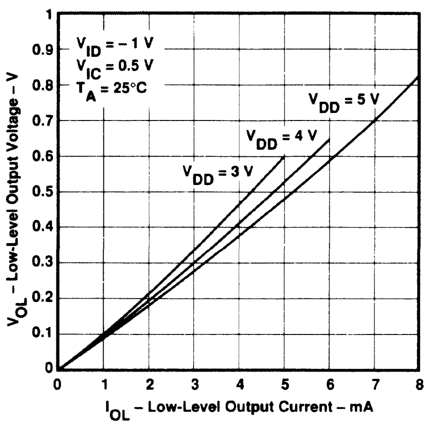


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

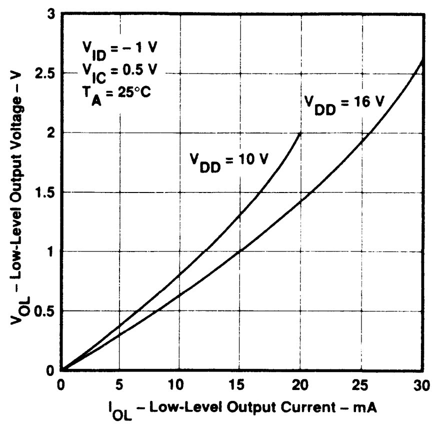


FIGURE 16

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

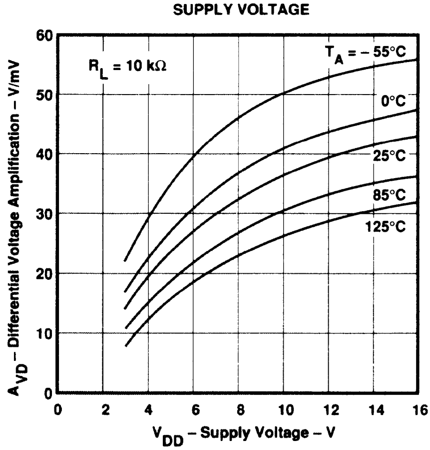


FIGURE 17

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

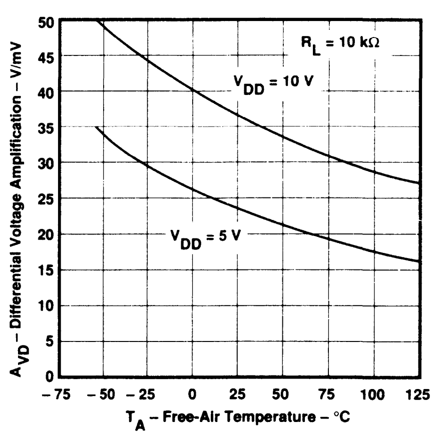


FIGURE 18

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

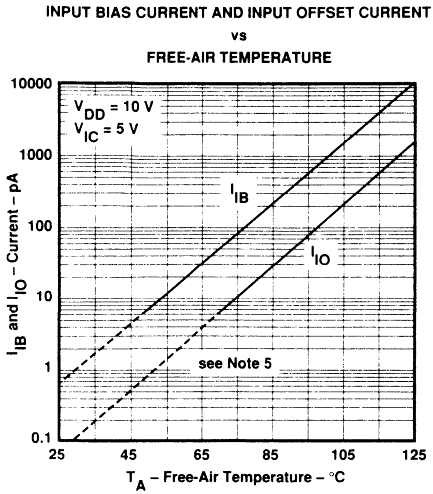


FIGURE 19

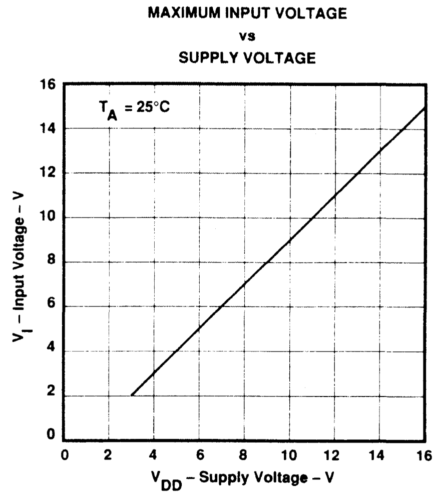


FIGURE 20

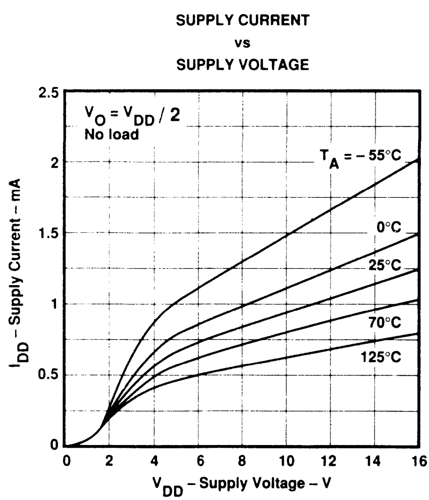


FIGURE 21

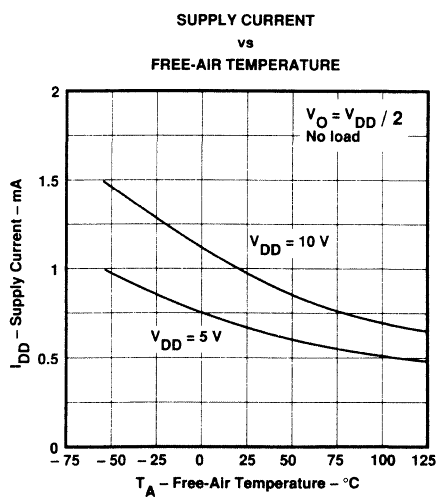


FIGURE 22

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

3 Operational Amplifiers

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

SLEW RATE
vs
SUPPLY VOLTAGE

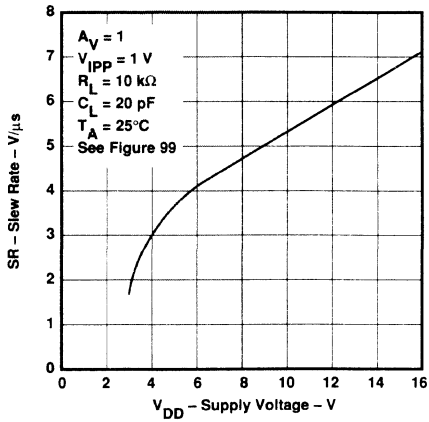


FIGURE 23

SLEW RATE
vs
FREE-AIR TEMPERATURE

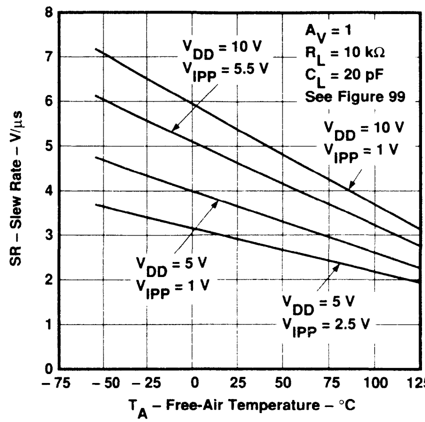


FIGURE 24

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

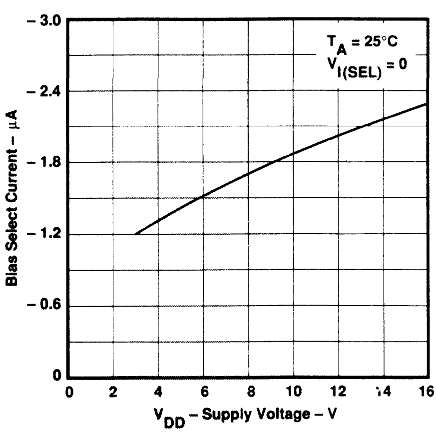


FIGURE 25

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

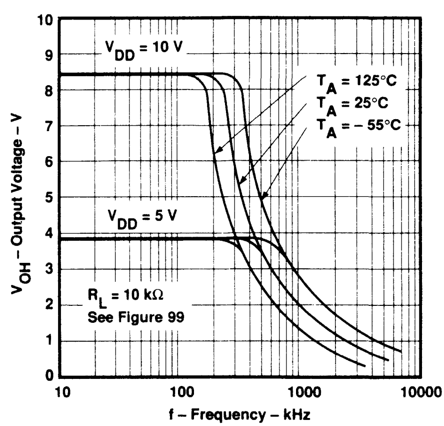


FIGURE 26

3 Operational Amplifiers

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

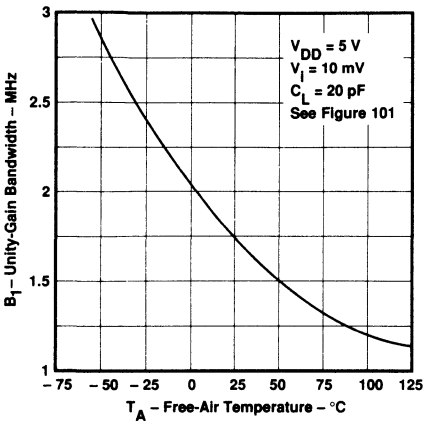


FIGURE 27

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

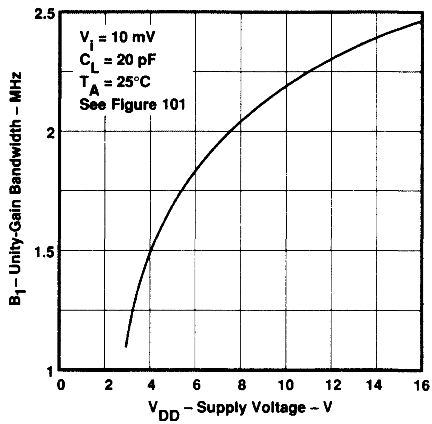


FIGURE 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

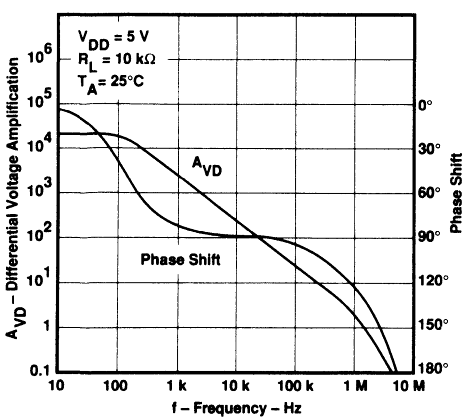


FIGURE 29

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

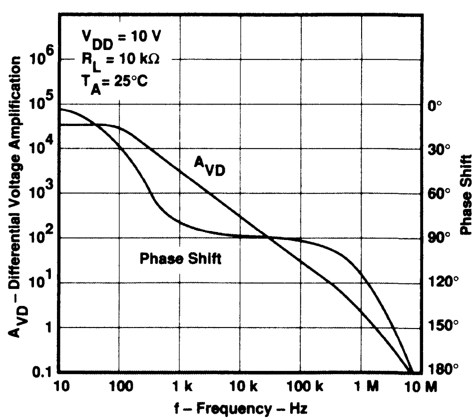


FIGURE 30

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

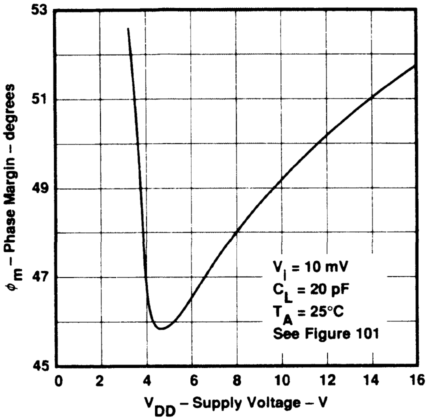


FIGURE 31

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

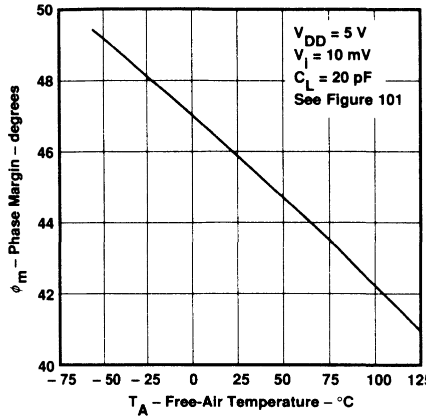


FIGURE 32

PHASE MARGIN
vs
CAPACITIVE LOAD

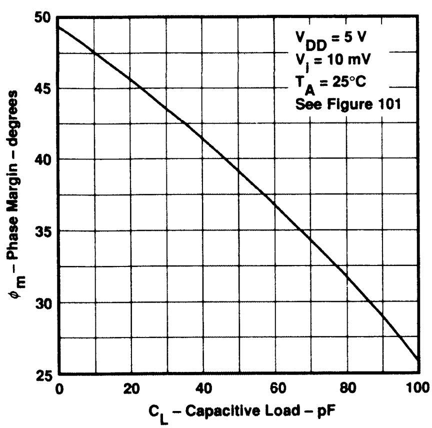


FIGURE 33

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

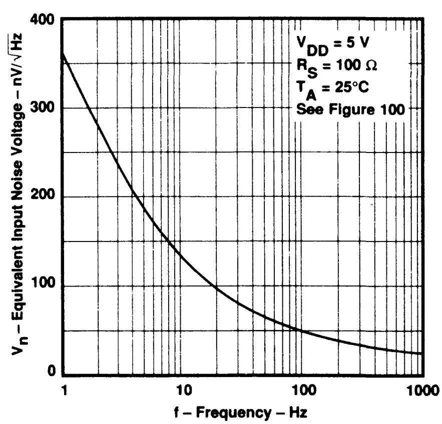


FIGURE 34

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C- SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.25	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	− 0.2 to 4	− 0.3 to 4.2		− 0.2 to 9	− 0.3 to 9.2		V
				Full range	− 0.2 to 3.5			− 0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				70°C	3	4		7.8	8.7		
				0°C	3	3.9		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				70°C		0	50		0	50	
				0°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 7	25°C	25	170		25	275		V/mV
				70°C	15	140		15	230		
				0°C	15	200		15	320		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	91		65	94		dB
				70°C	60	92		60	94		
				0°C	60	91		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				70°C	60	94		60	94		
				0°C	60	92		60	92		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}/2$	25°C		− 130			− 160		nA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		105	280		143	300	µA
				70°C		85	220		110	280	
				0°C		125	320		173	400	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.25	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	− 0.2 to 4	− 0.3 to 4.2		− 0.2 to 9	− 0.3 to 9.2		V
				Full range	− 0.2 to 3.5			− 0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				85°C	3	4		7.8	8.7		
				− 40°C	3	3.9		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				85°C		0	50		0	50	
				− 40°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 7	25°C	25	170		25	275		V/mV
				85°C	15	130		15	220		
				− 40°C	15	270		15	390		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	91		65	94		dB
				85°C	60	90		60	94		
				− 40°C	60	90		60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				85°C	60	94		60	94		
				− 40°C	60	91		60	91		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}/2$	25°C		− 130			− 160		nA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		105	280		143	300	µA
				85°C		80	200		103	260	
				− 40°C		158	400		225	450	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		M-SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.7			2.1		µV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
			125°C	3	4		7.8	3.8		
			−55°C	3	3.9		7.8	8.6		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			125°C		0	50		0	50	
			−55°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 100 kΩ, See Note 7	25°C	25	170		25	275		V/mV
			125°C	15	120		15	190		
			−55°C	15	290		15	420		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C	65	91		65	94		dB
			125°C	60	91		60	93		
			−55°C	60	89		60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
			125°C	60	94		60	94		
			−55°C	60	91		60	91		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)} = V_{DD}/2$	25°C		−130			−160		nA
I_{DD}	Supply current	No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		105	280		143	300	µA
			125°C		70	180		90	240	
			−55°C		170	440		245	500	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.43		V/μs
				70°C		0.36		
				0°C		0.46		
			V_{IPP} = 2.5 V	25°C		0.40		
				70°C		0.34		
				0°C		0.43		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		55		kHz
				70°C		50		
				0°C		60		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		525		kHz
				70°C		400		
				0°C		600		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		40°		
				70°C		39°		
				0°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.62		V/μs
				70°C		0.51		
				0°C		0.67		
			V_{IPP} = 5.5 V	25°C		0.56		
				70°C		0.46		
				0°C		0.61		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		35		kHz
				70°C		30		
				0°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		635		kHz
				70°C		510		
				0°C		710		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		43°		
				70°C		42°		
				0°C		44°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.43		V/μs
				85°C		0.35		
				− 40°C		0.51		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
				− 40°C		0.48		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		55		kHz
				85°C		45		
				− 40°C		75		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		525		kHz
				85°C		370		
				− 40°C		770		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		40°		
				85°C		38°		
				− 40°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.62		V/μs
				85°C		0.47		
				− 40°C		0.77		
			V_{IPP} = 5.5 V	25°C		0.56		
				85°C		0.44		
				− 40°C		0.70		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		35		kHz
				85°C		25		
				− 40°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		635		kHz
				85°C		480		
				− 40°C		880		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		43°		
				85°C		41°		
				− 40°C		46°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.43		V/μs
				125°C		0.29		
				− 55°C		0.54		
			V_{IPP} = 2.5 V	25°C		0.40		
				125°C		0.28		
				− 55°C		0.50		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		55		kHz
				125°C		40		
				− 55°C		80		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		525		kHz
				125°C		330		
				− 55°C		850		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		40°		
				125°C		36°		
				− 55°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.62		V/μs
				125°C		0.38		
				− 55°C		0.81		
			V_{IPP} = 5.5 V	25°C		0.56		
				125°C		0.35		
				− 55°C		0.73		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 99		25°C		35		kHz
				125°C		20		
				− 55°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		635		kHz
				125°C		440		
				− 55°C		960		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		43°		
				125°C		39°		
				− 55°C		47°		

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

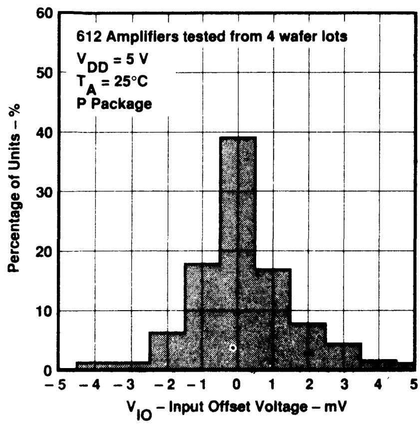


FIGURE 35

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

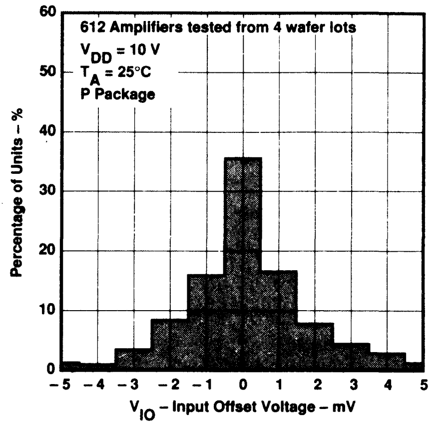


FIGURE 36

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

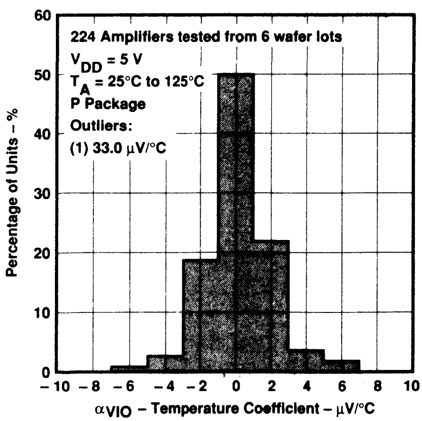


FIGURE37

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

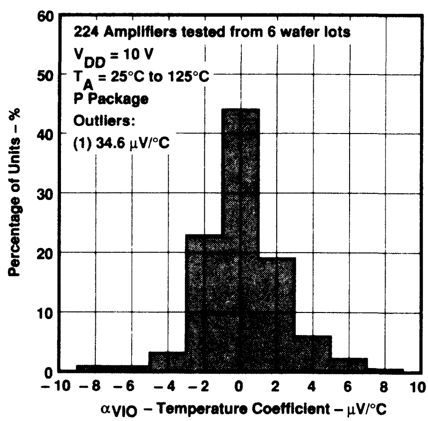


FIGURE 38

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

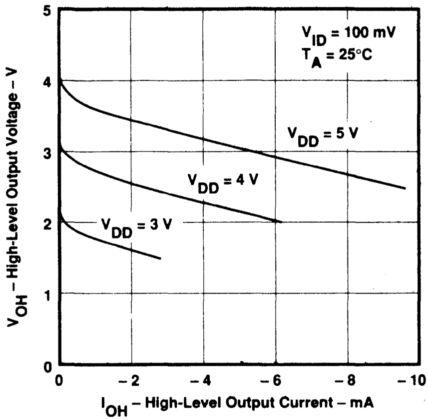


FIGURE 39

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

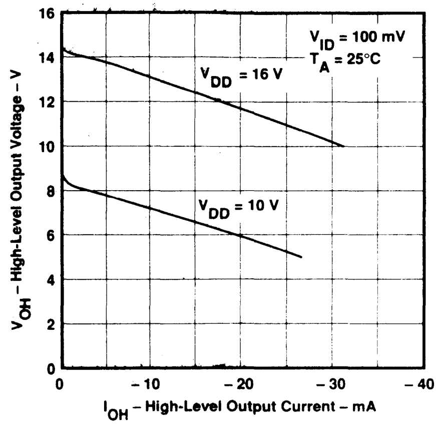


FIGURE 40

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

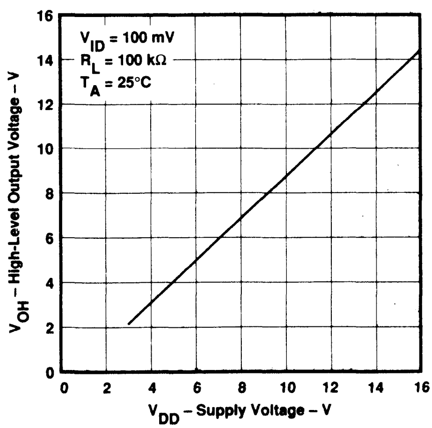


FIGURE 41

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

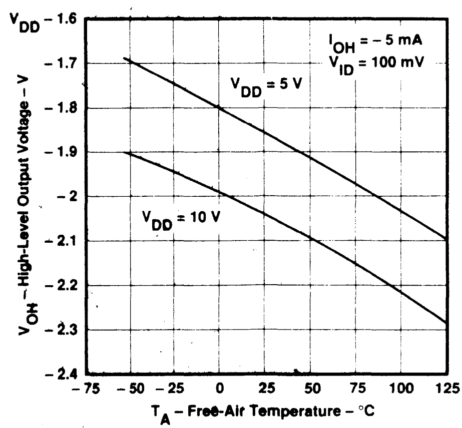


FIGURE 42

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Operational Amplifiers

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

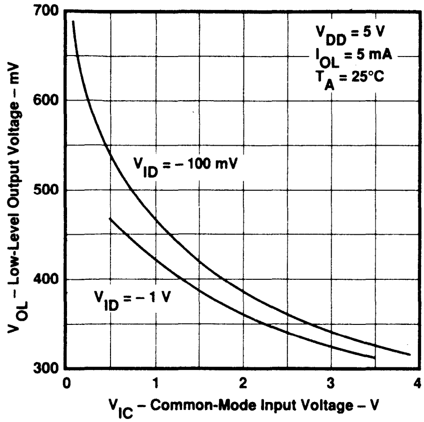

FIGURE 43

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

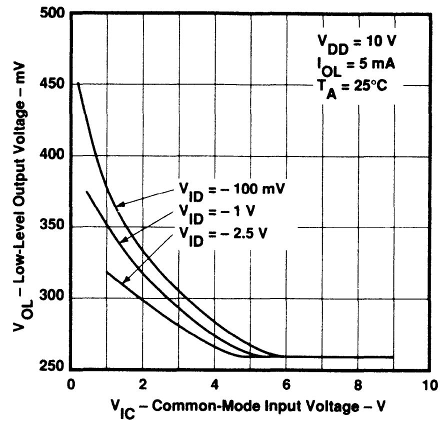

FIGURE 44

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

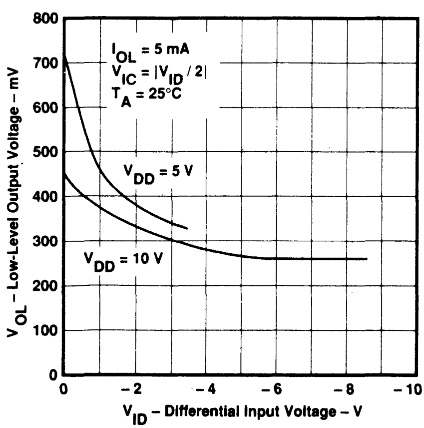

FIGURE 45

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

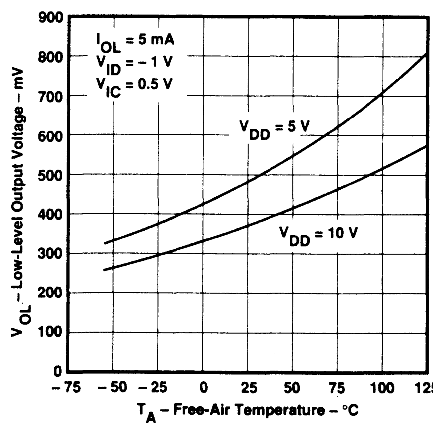

FIGURE 46

3 Operational Amplifiers

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

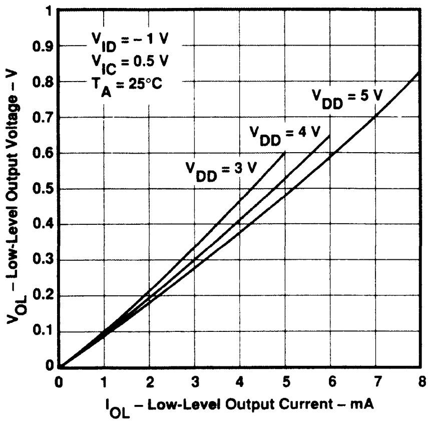

FIGURE 47

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

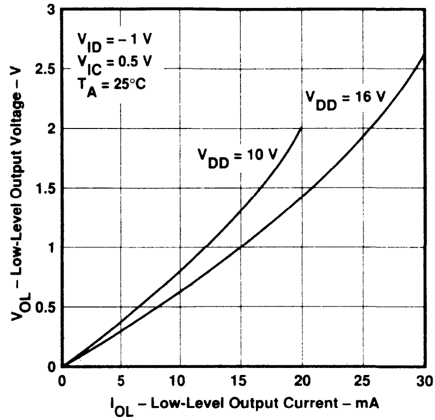

FIGURE 48

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

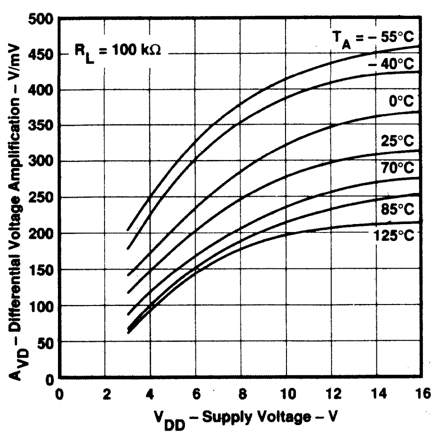

FIGURE 49

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

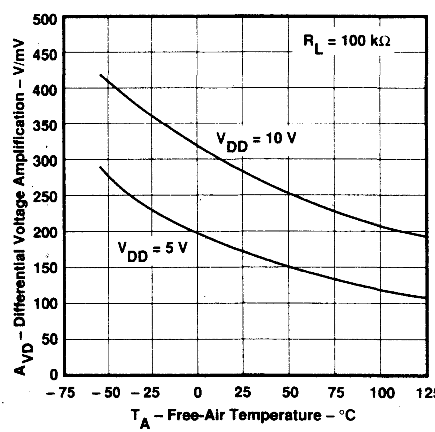

FIGURE 50

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

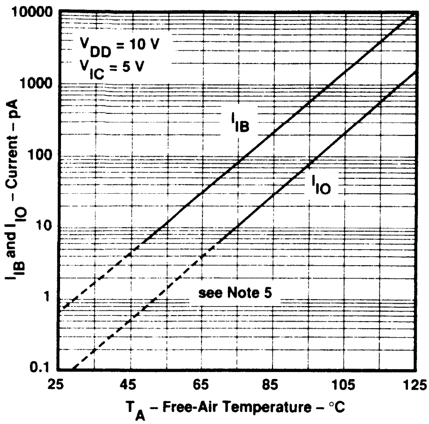

FIGURE 51

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

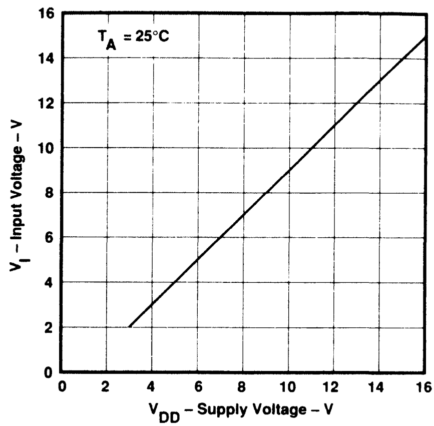

FIGURE 52

SUPPLY CURRENT vs SUPPLY VOLTAGE

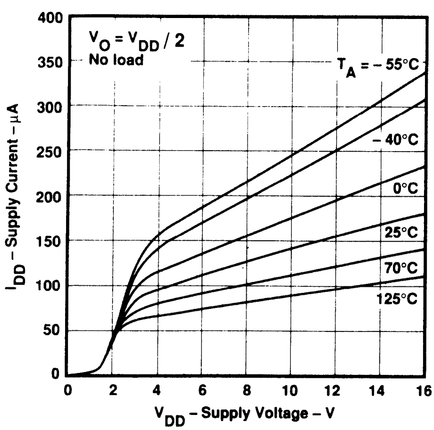

FIGURE 53

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

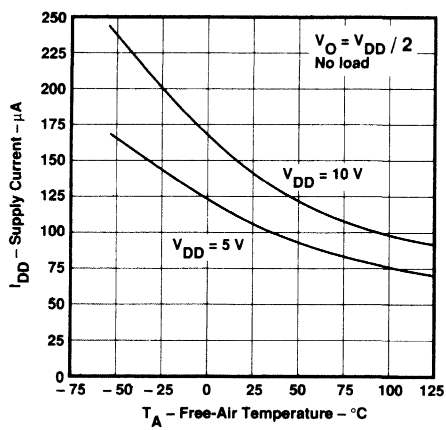

FIGURE 54

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

SLEW RATE
vs
SUPPLY VOLTAGE

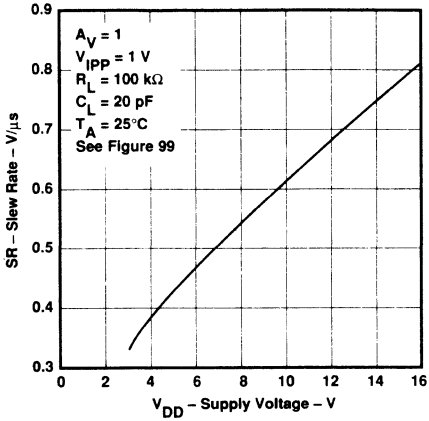

FIGURE 55

SLEW RATE
vs
FREE-AIR TEMPERATURE

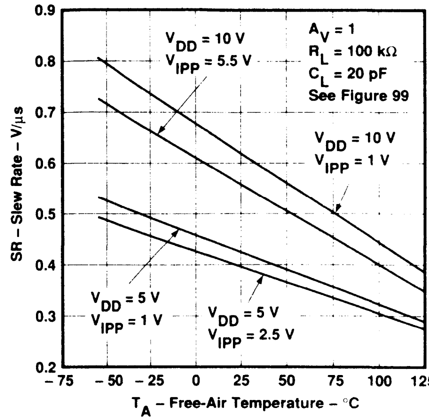

FIGURE56

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

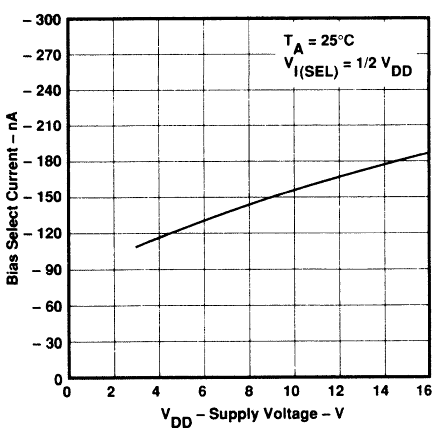

FIGURE 57

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

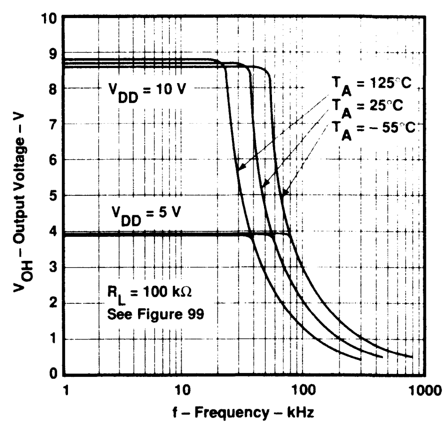

FIGURE 58

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Operational Amplifiers

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

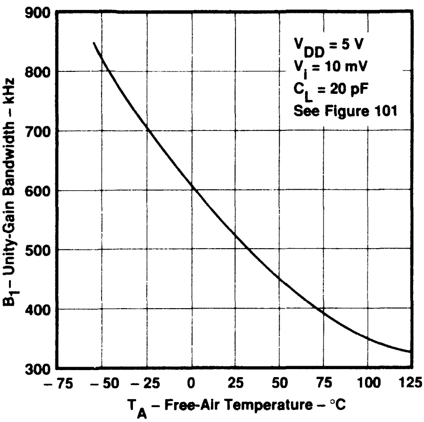

FIGURE 59

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

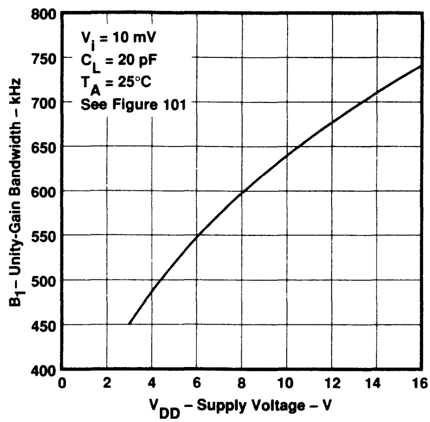

FIGURE 60

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

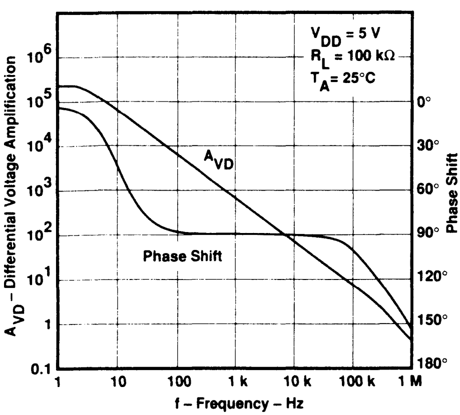

FIGURE 61

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

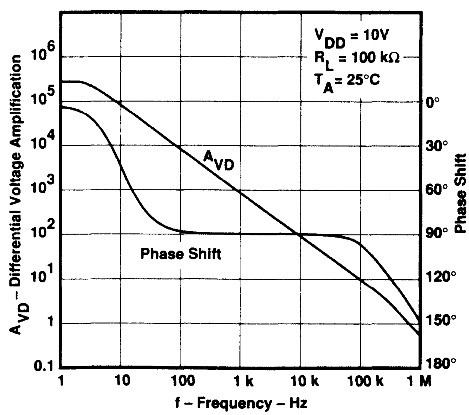

FIGURE 62

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

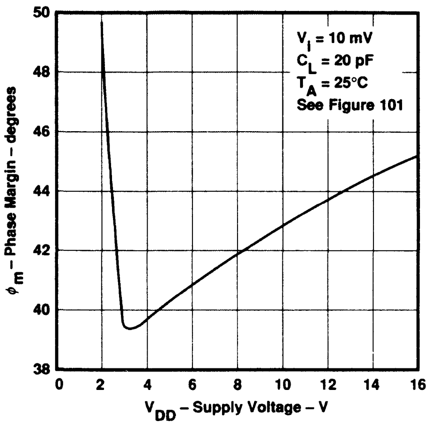

FIGURE 63

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

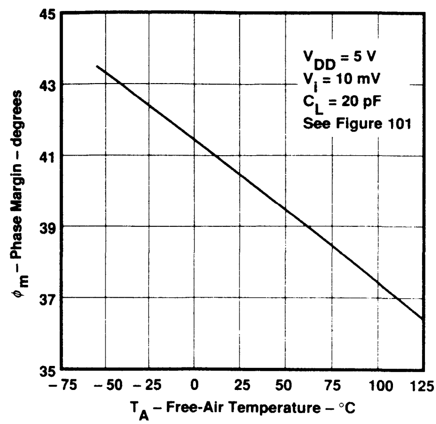

FIGURE 64

PHASE MARGIN
vs
CAPACITIVE LOAD

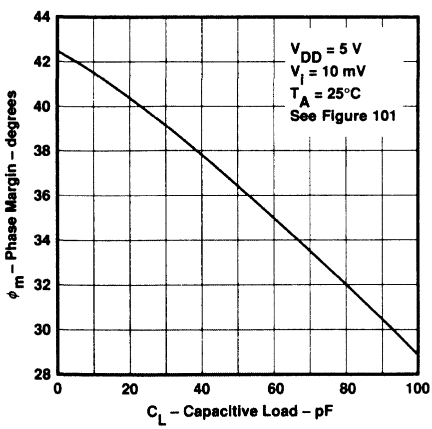

FIGURE 65

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

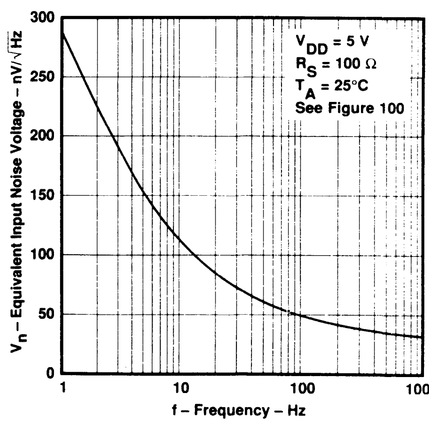

FIGURE 66

Operational Amplifiers 3

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				70°C	3	4.2		7.8	8.9		
				0°C	3	4.1		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				70°C		0	50		0	50	
				0°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 7	25°C	50	480		50	800		V/mV
				70°C	50	380		50	660		
				0°C	50	700		50	1100		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	94		65	97		dB
				70°C	60	95		60	97		
				0°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				70°C	60	98		60	98		
				0°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		10	17		14	23	µA
				70°C		8	14		11	20	
				0°C		12	21		18	33	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				85°C	3	4.2		7.8	8.9		
				−40°C	3	4.1		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				85°C		0	50		0	50	
				−40°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 7	25°C	50	480		50	800		V/mV
				85°C	50	330		50	585		
				−40°C	50	900		50	1550		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$	25°C	65	94		65	97		dB
				85°C	60	95		60	98		
				−40°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				85°C	60	98		60	98		
				−40°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		10	17		14	23	μA
				85°C		7	13		10	18	
				−40°C		16	27		25	43	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		M- SUFFIX TYPES V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	− 0.3 to 4.2		0 to 9	− 0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			125°C	3	4.2		7.8	9		
			− 55°C	3	4.1		7.8	8.8		
V_{OL}	Low-level output voltage	V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			125°C		0	50		0	50	
			− 55°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 7	25°C	50	480		50	800		V/mV
			125°C	25	200		25	380		
			− 55°C	25	950		25	1750		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C	65	94		65	97		dB
			125°C	60	85		60	91		
			− 55°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
			125°C	60	98		60	98		
			− 55°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current	No load, $V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		10	17		14	23	μA
			125°C		7	12		9	15	
			− 55°C		17	30		28	48	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.03		V/μs
				70°C		0.03		
				0°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				70°C		0.02		
				0°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		5		kHz
				70°C		4.5		
				0°C		6		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		85		kHz
				70°C		65		
				0°C		100		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		34°		
				70°C		30°		
				0°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.05		V/μs
				70°C		0.04		
				0°C		0.05		
			V_{IPP} = 5.5 V	25°C		0.04		
				70°C		0.04		
				0°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		1		kHz
				70°C		0.9		
				0°C		1.3		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		110		kHz
				70°C		90		
				0°C		125		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		38°		
				70°C		34°		
				0°C		40°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.03		V/µs
				85°C		0.03		
				−40°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
				−40°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1MΩ, See Figure 99		25°C		5		kHz
				85°C		4		
				−40°C		7		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		85		kHz
				85°C		55		
				−40°C		130		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		34°		
				85°C		28°		
				−40°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.05		V/µs
				85°C		0.03		
				−40°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				85°C		0.03		
				−40°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		1		kHz
				85°C		0.8		
				−40°C		1.4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		110		kHz
				85°C		80		
				−40°C		155		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		38°		
				85°C		32°		
				−40°C		42°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.03		V/μs
				125°C		0.02		
				−55°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				125°C		0.02		
				−55°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		5		kHz
				125°C		3		
				−55°C		8		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		85		kHz
				125°C		45		
				−55°C		140		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		34°		
				125°C		25°		
				−55°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		0.05		V/μs
				125°C		0.03		
				−55°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				125°C		0.03		
				−55°C		0.06		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 100		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 99		25°C		1		kHz
				125°C		0.7		
				−55°C		1.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		110		kHz
				125°C		70		
				−55°C		165		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 101		25°C		38°		
				125°C		29°		
				−55°C		43°		

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

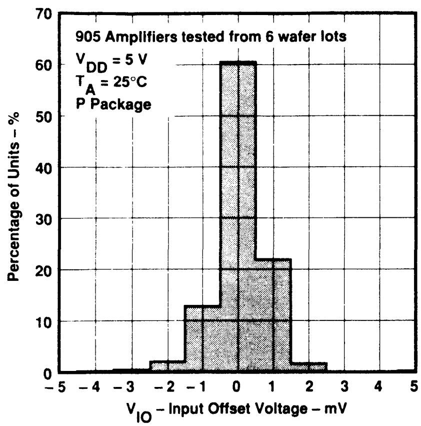

FIGURE 67

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

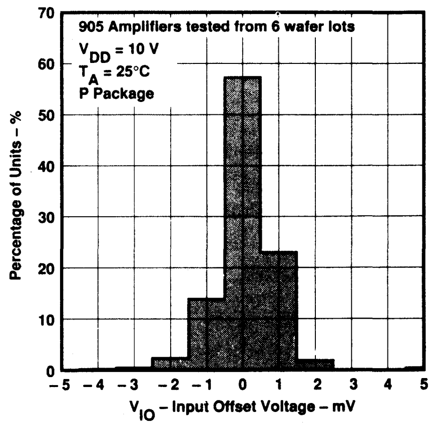

FIGURE 68

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

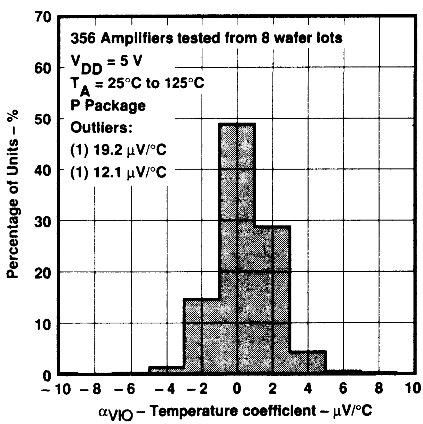

FIGURE 69

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

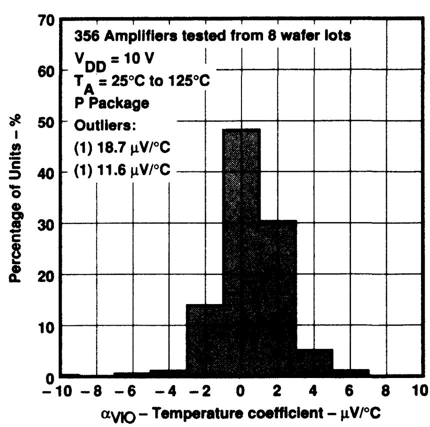

FIGURE 70

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

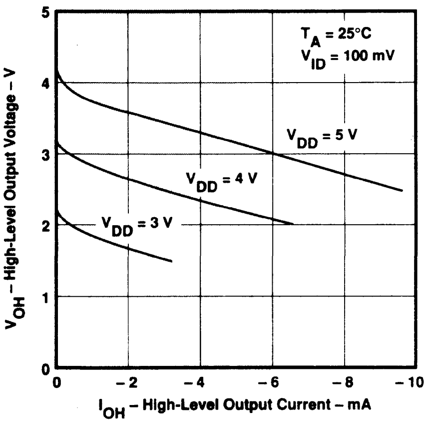

FIGURE 71

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

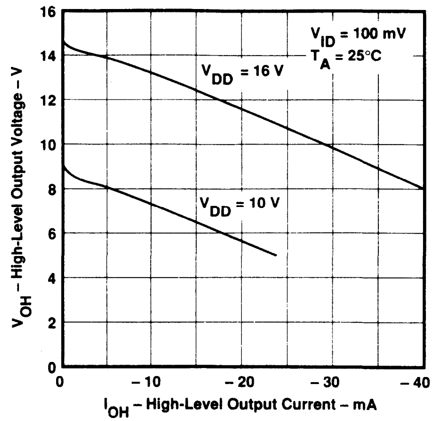

FIGURE 72

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

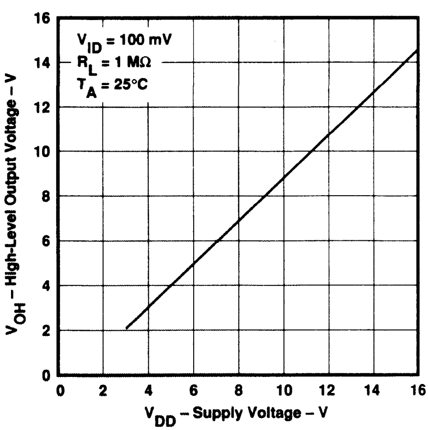

FIGURE 73

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

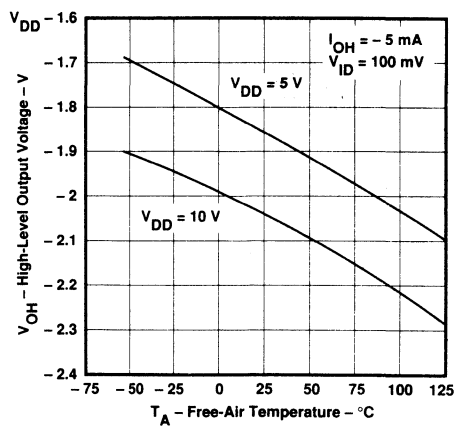

FIGURE 74

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TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

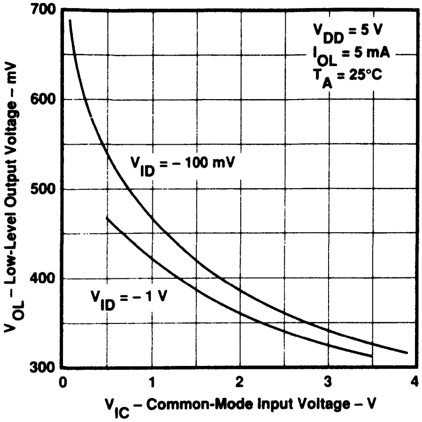

FIGURE 75

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

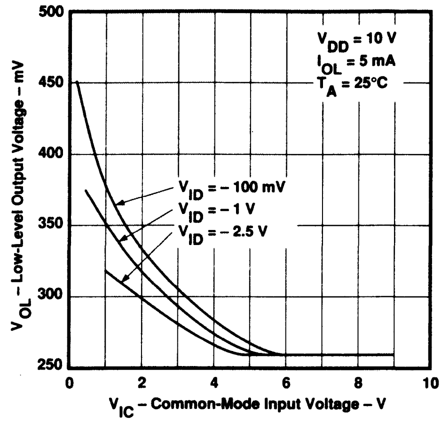

FIGURE 76

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

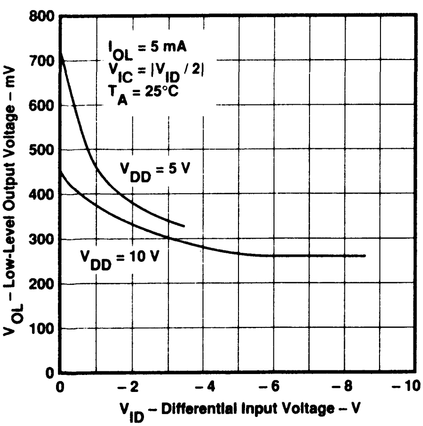

FIGURE 77

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

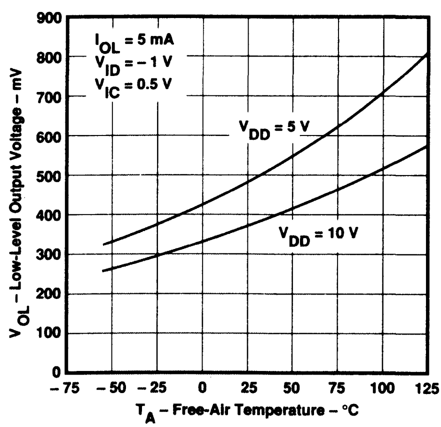

FIGURE 78

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

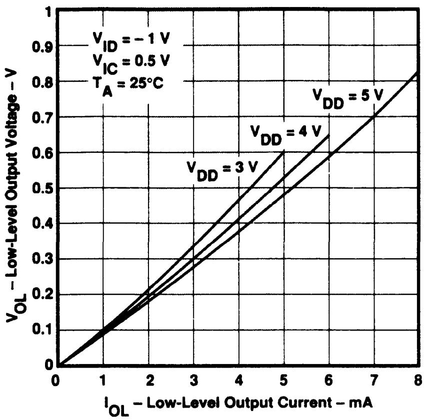

FIGURE 79

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

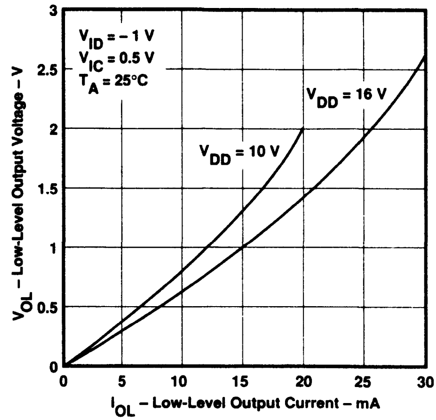

FIGURE 80

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

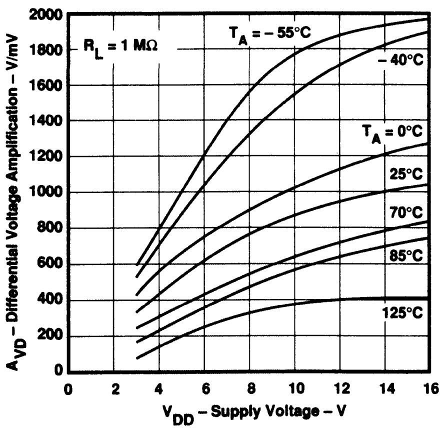

FIGURE 81

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

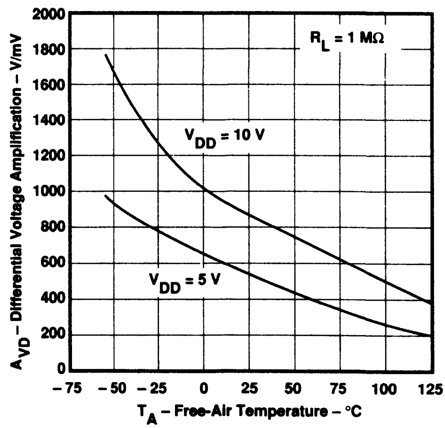

FIGURE 82

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

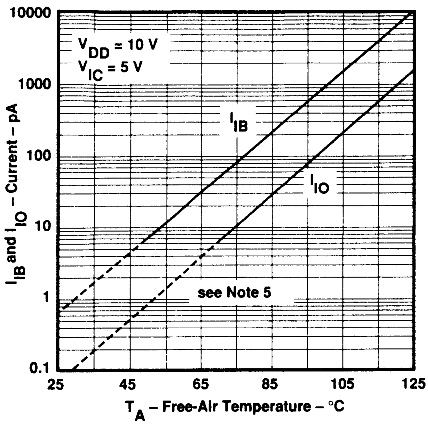

FIGURE 83

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

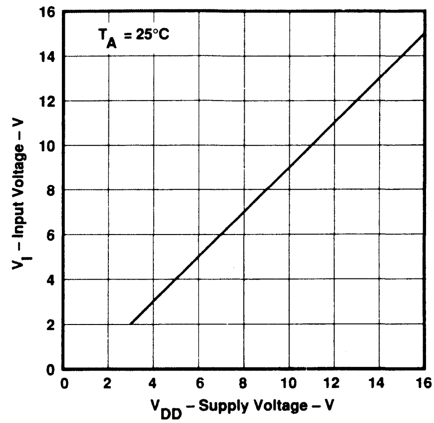

FIGURE 84

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

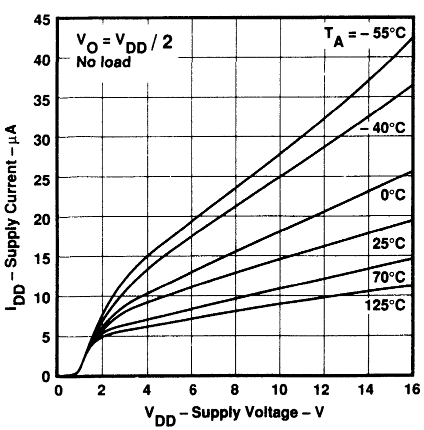

FIGURE 85

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

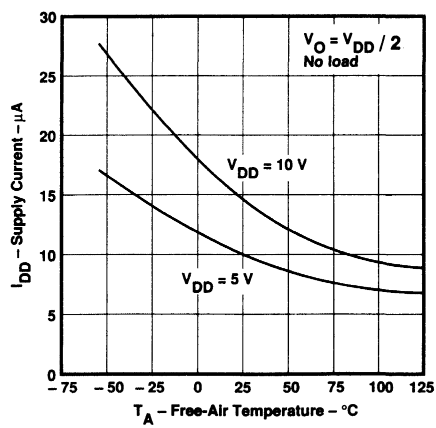

FIGURE 86

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

SLEW RATE
vs
SUPPLY VOLTAGE

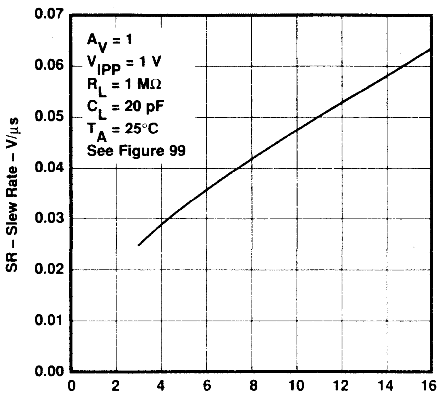

FIGURE 87

SLEW RATE
vs
FREE-AIR TEMPERATURE

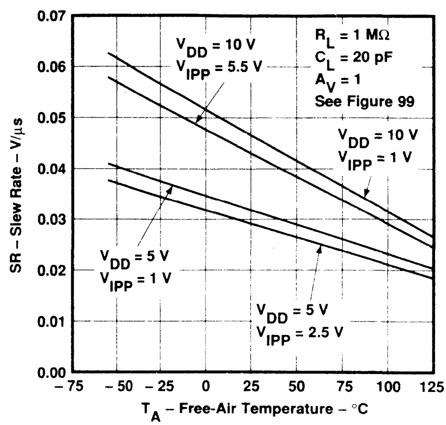

FIGURE 88

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

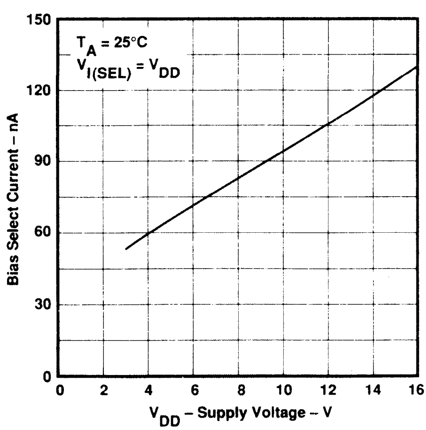

FIGURE 89

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

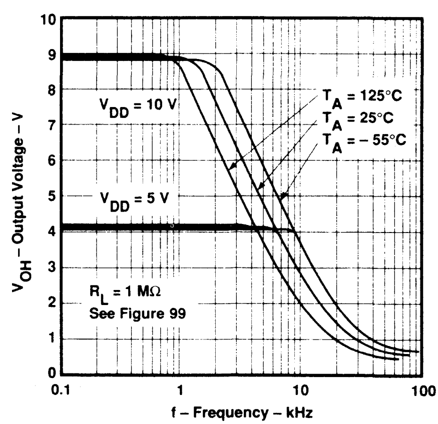

FIGURE 90

3
Operational Amplifiers

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

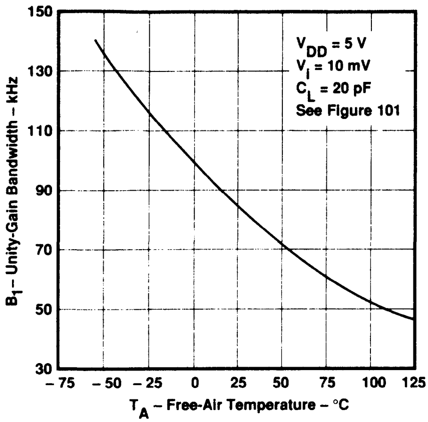

FIGURE 91

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

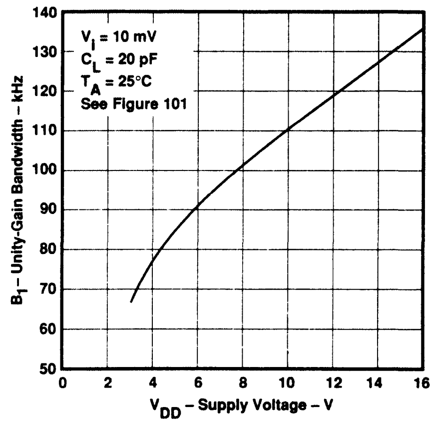

FIGURE 92

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

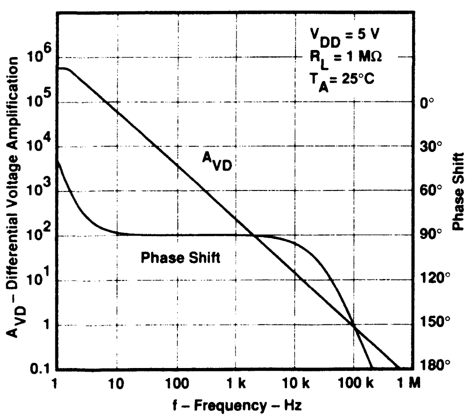

FIGURE 93

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

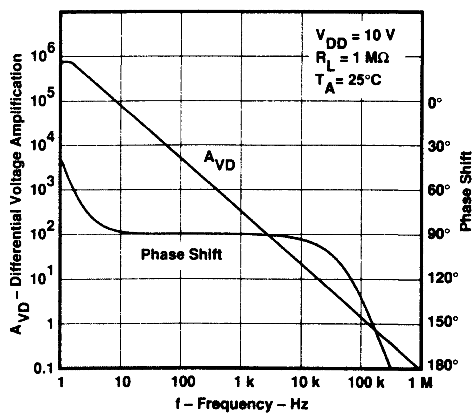

FIGURE 94

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TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

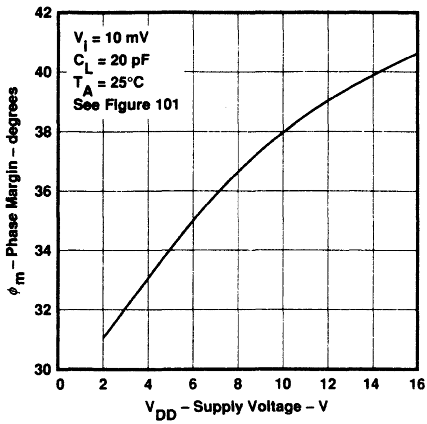


FIGURE 95

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

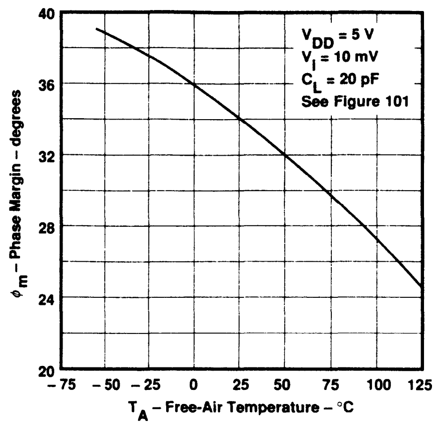


FIGURE 96

PHASE MARGIN
vs
CAPACITIVE LOAD

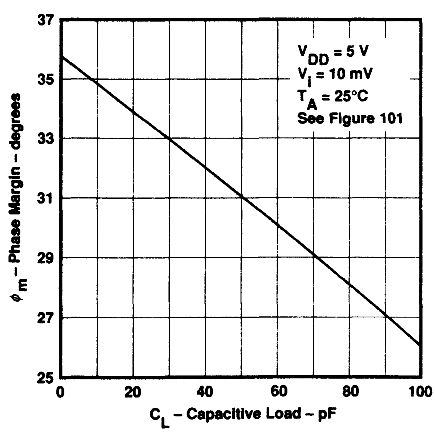


FIGURE 97

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

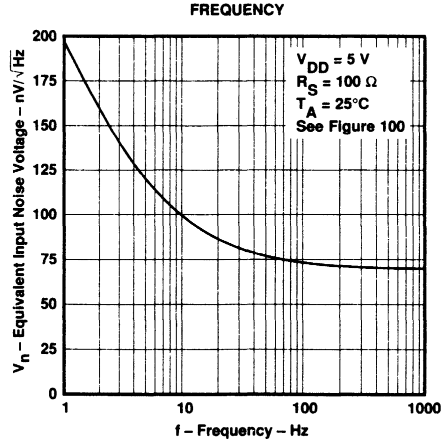


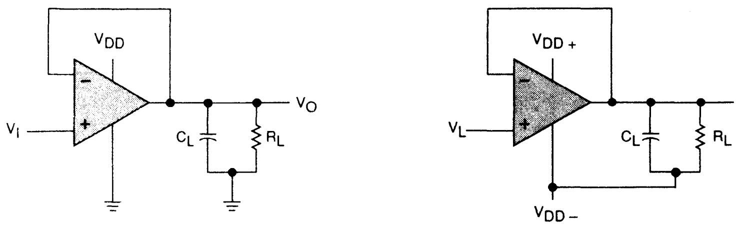
FIGURE 98

3
Operational Amplifiers

PARAMETER MEASUREMENT INFORMATION

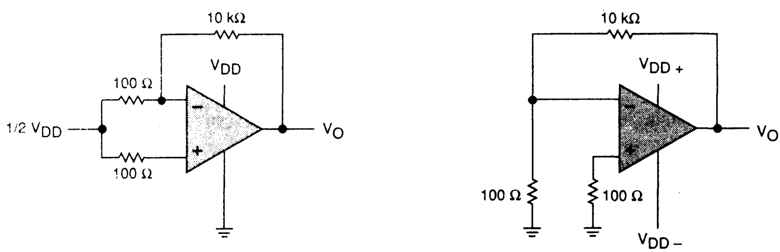
single-supply versus split-supply test circuits

Because the TLC271 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



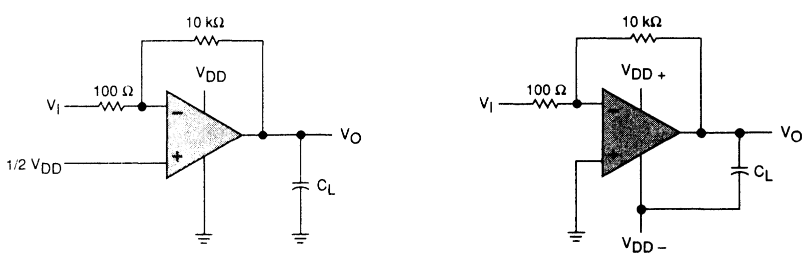
(a) Single-Supply (b) Split-Supply

FIGURE 99. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 100. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 101. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC271 op amp, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 102). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

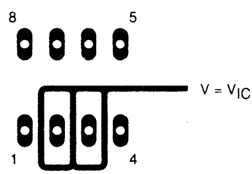


FIGURE 102. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally

PARAMETER MEASUREMENT INFORMATION

measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 99. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 103). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

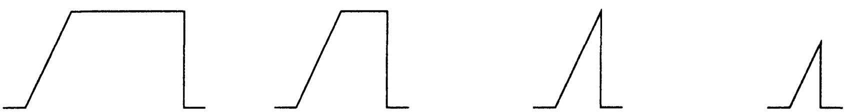


FIGURE 103. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLC271 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 104). The low input bias current consumption of the TLC271 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

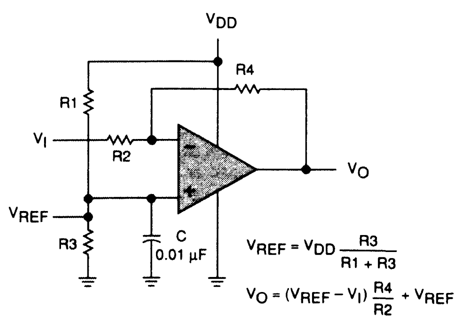
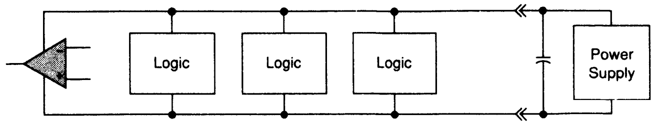


FIGURE 104. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

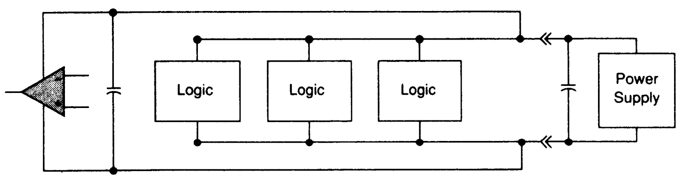
TYPICAL APPLICATION DATA

The TLC271 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 105); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails

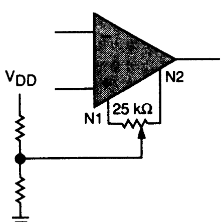


(b) Separate Bypassed Supply Rails (preferred)

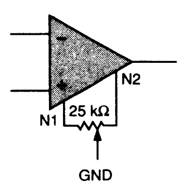
FIGURE 105. COMMON VERSUS SEPARATE SUPPLY RAILS

input offset voltage nulling

The TLC271 offers external input offset null control. Nulling of the input offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 106. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range will allow the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.



(a) Single-Supply



(b) Split-Supply

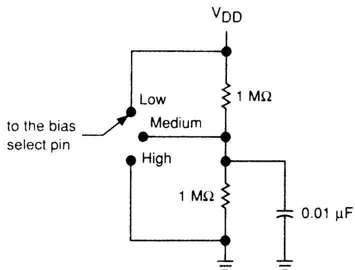
FIGURE 106. INPUT OFFSET VOLTAGE NULL CIRCUIT

Operational Amplifiers 3

TYPICAL APPLICATION DATA

bias selection

Bias selection is achieved by connecting the bias select pin to one of the three voltage levels (see Figure 107). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to V_{DD} − 1 V
HIGH	GND

FIGURE 107. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

input characteristics

The TLC271 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} − 1 V at T_A = 25°C and at V_{DD} − 1.5 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC271 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

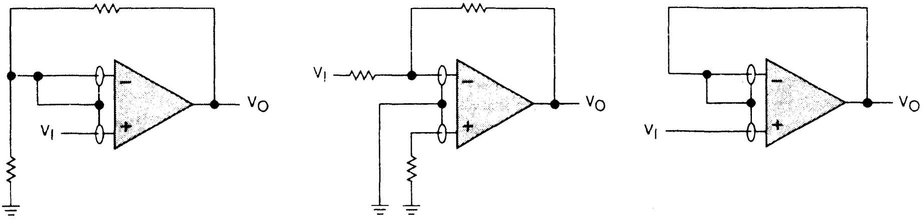
Because of the extremely high input impedance and resulting low bias current requirements, the TLC271 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 102 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 108).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC271 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

TYPICAL APPLICATION DATA



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity Gain Amplifier

Figure 108. GUARD RING SCHEMES

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 109). The value of this capacitor is optimized empirically.

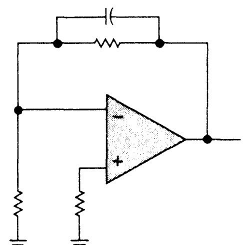


FIGURE 109. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC271 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC271 inputs and output were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

output characteristics

The output stage of the TLC271 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC271 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures below). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.

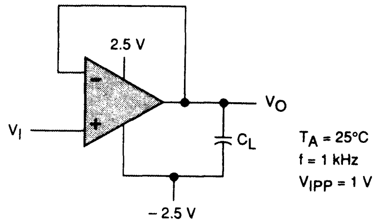
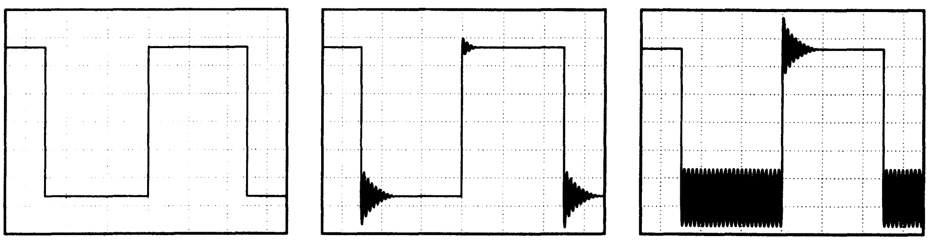
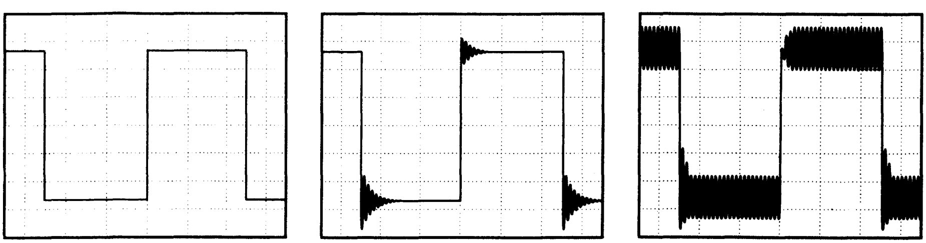


FIGURE 110. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS



(a) C_L = 20 pF, R_L = no load (a) C_L = 130 pF, R_L = no load (a) C_L = 150 pF, R_L = no load

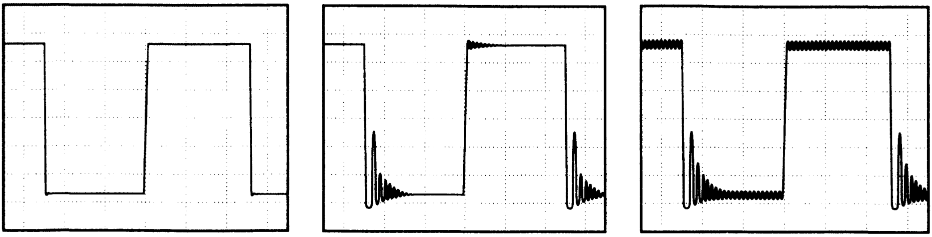
FIGURE 111. EFFECT OF CAPACITIVE LOADS IN HIGH-BIAS MODE



(a) C_L = 20 pF, R_L = no load (a) C_L = 170 pF, R_L = no load (a) C_L = 190 pF, R_L = no load

FIGURE 112. EFFECT OF CAPACITIVE LOADS IN MEDIUM-BIAS MODE

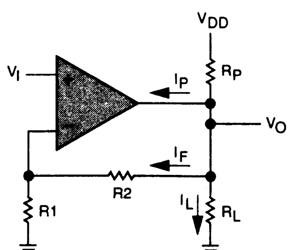
TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = no load (a) C_L = 260 pF, R_L = no load (a) C_L = 310 pF, R_L = no load

FIGURE 113. EFFECT OF CAPACITIVE LOADS IN LOW-BIAS MODE

Although the TLC271 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor (R_P) connected from the output to the positive supply rail (see Figure 114). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

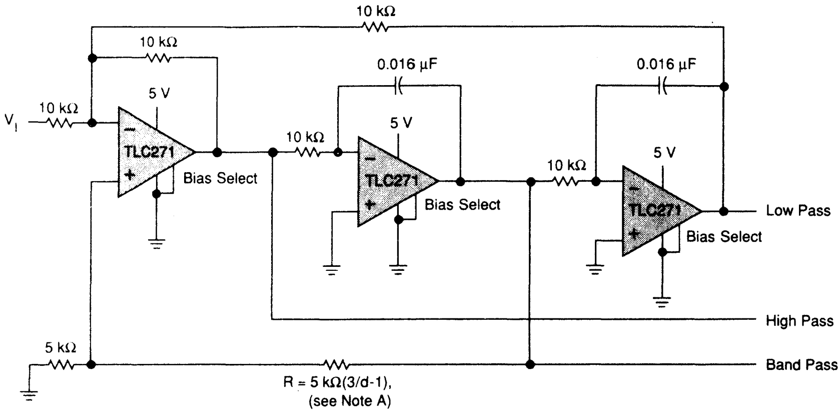


$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pull-up curent required by the op amp (typically 500 μA)

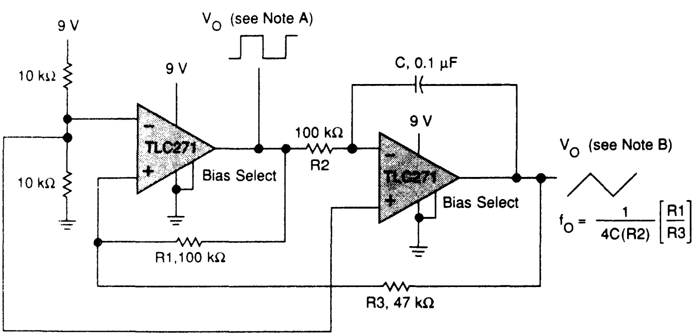
FIGURE 114. RESISTIVE PULL-UP TO INCREASE V_{OH}

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

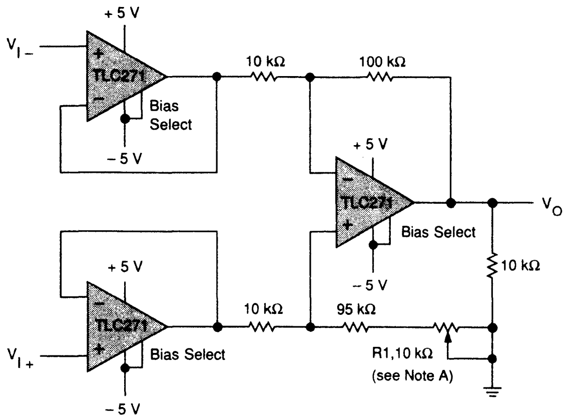
FIGURE 115. STATE VARIABLE FILTER



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

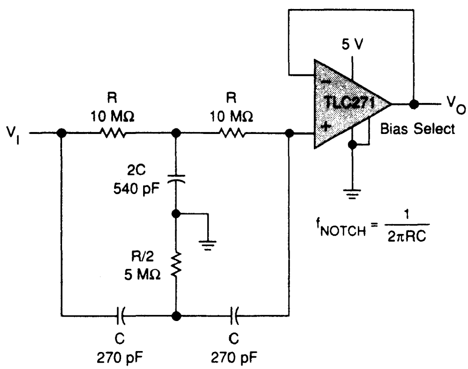
FIGURE 116. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTE A: CMRR Adjustment (must be noninductive).

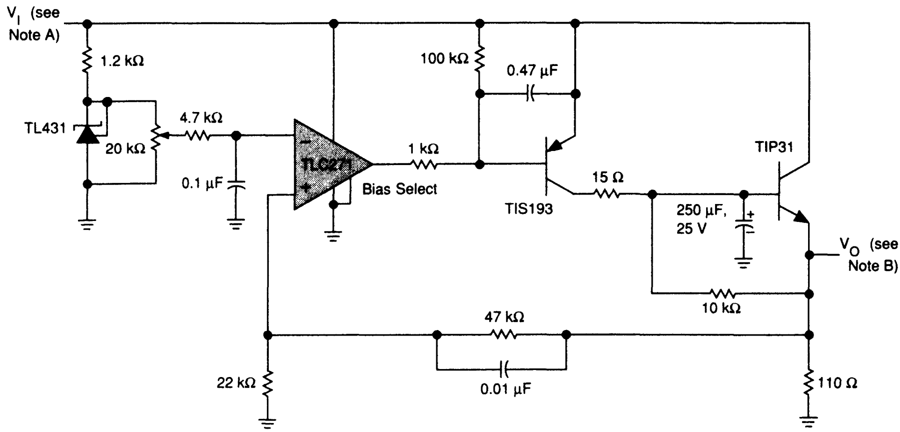
FIGURE 117. LOW-POWER INSTRUMENTATION AMPLIFIER



$$f_{NOTCH} = \frac{1}{2\pi RC}$$

FIGURE 118. SINGLE-SUPPLY TWIN-T NOTCH FILTER

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

FIGURE 119. LOGIC ARRAY POWER SUPPLY

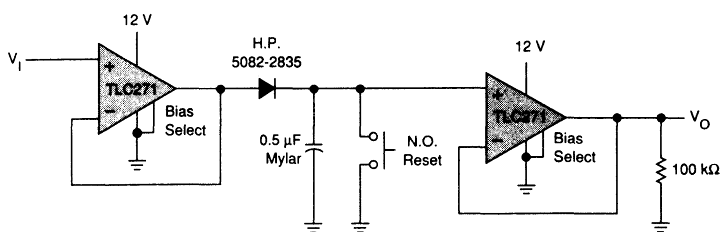
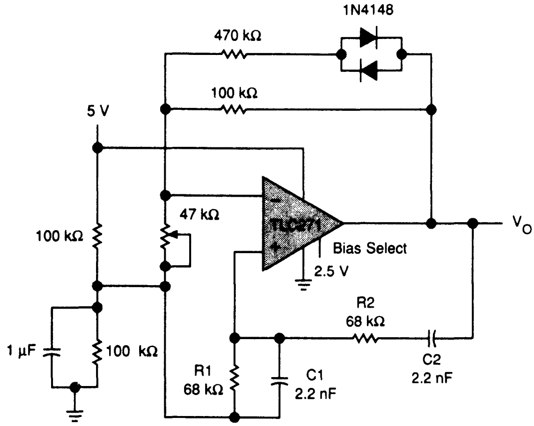


FIGURE 120. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 121. WIEN OSCILLATOR

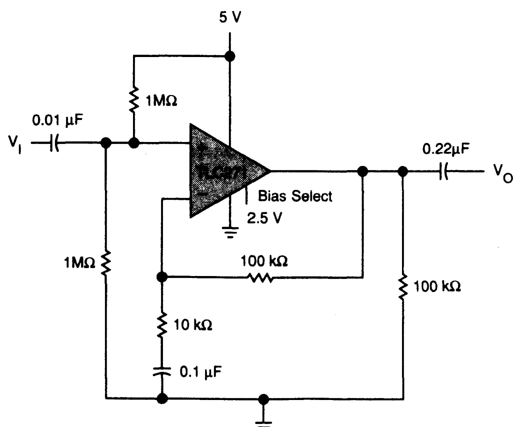
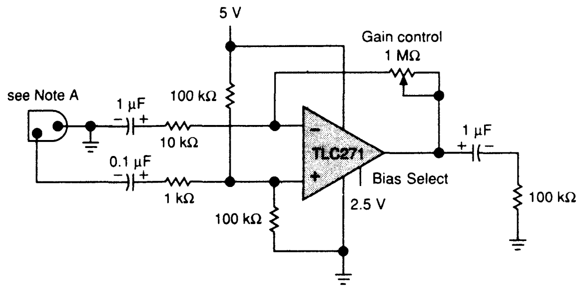


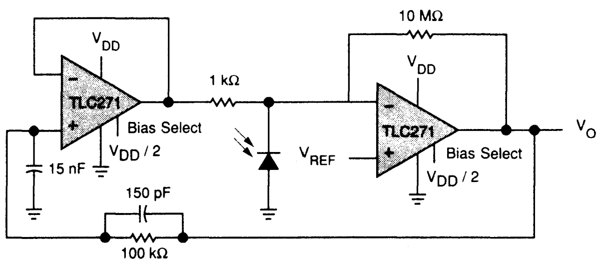
FIGURE 122. SINGLE-SUPPLY A.C. AMPLIFIER

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



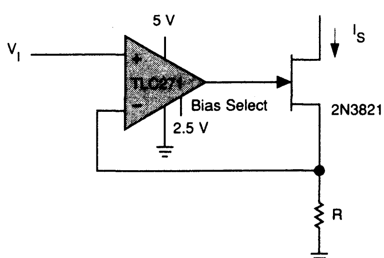
NOTE A: Low to medium impedance dynamic mike

FIGURE 123. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 124. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

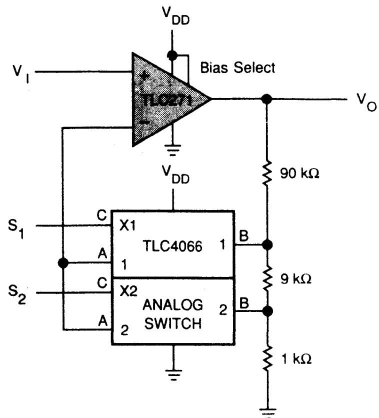


NOTES: V_I = 0 V TO 3 V
$I_S = \frac{V_I}{R}$

FIGURE 125. PRECISION LOW-CURRENT SINK

3 Operational Amplifiers

TYPICAL APPLICATION DATA (LOW-BIAS MODE)



Select:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12V

FIGURE 126. AMPLIFIER WITH DIGITAL GAIN SELECTION

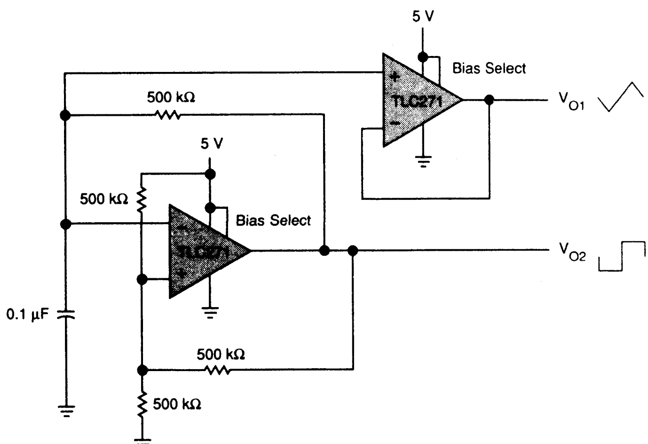
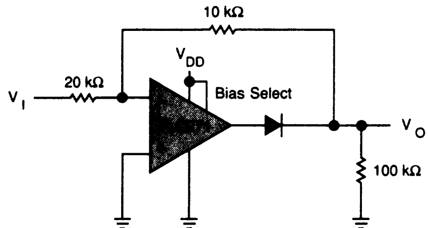


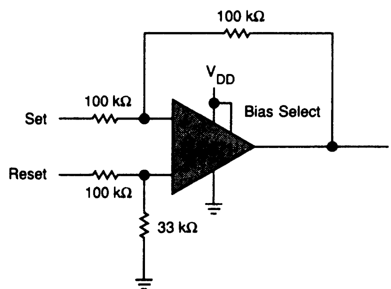
FIGURE 127. MULTIVIBRATOR

TYPICAL APPLICATION DATA (LOW-BIAS MODE)



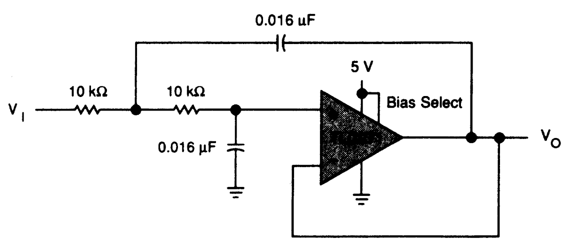
NOTE: V_{DD} = 5 V to 16V

FIGURE 128. FULL WAVE RECTIFIER



NOTE: V_{DD} = 5 V to 16V

FIGURE 129. SET / RESET FLIP-FLOP



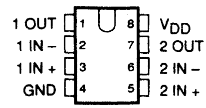
NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 130. TWO-POLE LOW-PASS BUTTERWORTH FILTER

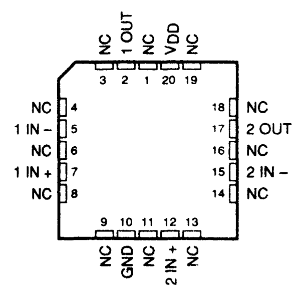
OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC277 . . . 500 µV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically 0.1 µV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise . . . 25 nV/√Hz Typically at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

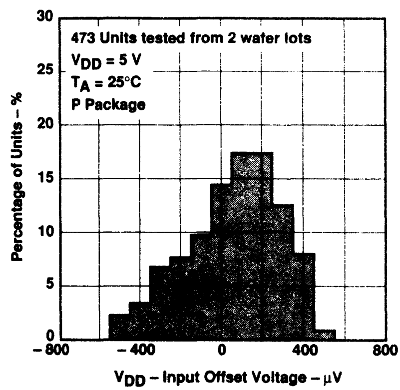
description

The TLC272 and TLC277 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	500 µV	TLC277CD	TLC277CP	TLC277CJG	——
	2 mV	TLC272BCD	TLC272BCP	TLC272BCJG	——
	5 mV	TLC272ACD	TLC272ACP	TLC272ACJG	——
	10 mV	TLC272CD	TLC272CP	TLC272CJG	——
– 40°C to 85°C	500 µV	TLC277ID	TLC277IP	TLC277IJG	——
	2 mV	TLC272BID	TLC272BIP	TLC272BIJG	——
	5 mV	TLC272AID	TLC272AIP	TLC272AIJG	——
	10 mV	TLC272ID	TLC272IP	TLC272IJG	——
– 55°C to 125°C	500 µV	——	——	TLC277MJG	TLC277MFK
	10 mV	——	——	TLC272MJG	TLC272MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC277CDR).

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



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TEXAS INSTRUMENTS

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single supply operation making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

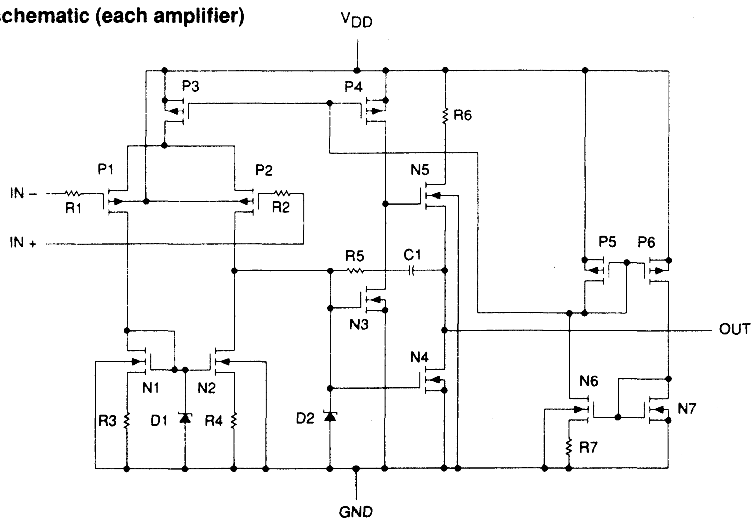
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC272 and TLC277 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... -0.3 V to V_{DD}
Input current, I_I .... ±5 mA
Output current, I_O (each output) .... ±30 mA
Total current into V_{DD} terminal .... 45 mA
Total current out of ground terminal .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types .... 0°C to 70°C
I-suffix types .... −40°C to 85°C
M-suffix types .... −55°C to 125°C
Storage temperature range .... −65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package .... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX TYPES			I-SUFFIX TYPES			C-SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC272AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC272BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		230	2000	µV
				Full range			3000	
		TLC277C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				70°C	3	3.8		
				0°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				70°C	4	20		
				0°C	4	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				70°C	60	85		
				0°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		
				0°C	60	94		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		1.4	3.2	mA
				70°C		1.2	2.6	
				0°C		1.6	3.6	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC272AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC272BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		290	2000	µV
				Full range			3000	µV
		TLC277C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	µV
				Full range			1900	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				70°C	7.8	8.4		V
				0°C	7.8	8.5		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				70°C	7.5	32		V/mV
				0°C	7.5	42		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				70°C	60	88		dB
				0°C	60	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		dB
				0°C	60	94		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1.9	4	mA
				70°C		1.5	3.4	mA
				0°C		2.3	4.4	mA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	mV
		TLC272AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	mV
				Full range			7	mV
		TLC272BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		230	2000	μV
				Full range			3500	μV
		TLC277I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	μV
				Full range			2000	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				85°C	3	3.8		V
				−40°C	3	3.8		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	mV
				−40°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				85°C	3.5	19		V/mV
				−40°C	3.5	32		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				85°C	60	86		dB
				−40°C	60	81		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		dB
				−40°C	60	92		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		1.4	3.2	mA
				85°C		1.1	2.4	mA
				−40°C		1.9	4.4	mA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

TEXAS INSTRUMENTS

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC272AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC272BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		290	2000	μV
				Full range			3500	
		TLC277I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				85°C	7.8	8.5		
				−40°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				85°C	7	31		
				−40°C	7	46		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				85°C	60	88		
				−40°C	60	87		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		
				−40°C	60	92		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1.9	4	mA
				85°C		1.5	3.2	
				−40°C		2.8	5	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC277M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		200	500	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				125°C	3	3.8		
				−55°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				125°C	3.5	16		
				−55°C	3.5	35		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				125°C	60	84		
				−55°C	60	81		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		
				−55°C	60	90		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		1.4	3.2	mA
				125°C		1	2.2	
				−55°C		2	5	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

3 Operational Amplifiers

TEXAS INSTRUMENTS

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC277M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		250	800	µV
				Full range			4300	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				125°C	7.8	8.4		V
				−55°C	7.8	8.5		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	mV
				−55°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				125°C	7	27		V/mV
				−55°C	7	50		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				125°C	60	86		dB
				−55°C	60	87		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		dB
				−55°C	60	90		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1.9	4	mA
				125°C		1.3	2.8	mA
				−55°C		3	6	mA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				70°C		3		
				0°C		3.9		
			V_{IPP} = 2.5 V	25°C		2.9		
				70°C		2.5		
				0°C		3.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				70°C		260		
				0°C		340		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				70°C		1.3		
				0°C		2		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				70°C		43°		
				0°C		47°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				70°C		4.3		
				0°C		5.9		
			V_{IPP} = 5.5 V	25°C		4.6		
				70°C		3.8		
				0°C		5.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				70°C		140		
				0°C		220		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				70°C		1.8		
				0°C		2.5		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				70°C		46°		
				0°C		50°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/µs
				85°C		2.8		
				− 40°C		4.5		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
				− 40°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				85°C		250		
				− 40°C		380		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				85°C		1.2		
				− 40°C		2.6		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				85°C		43°		
				− 40°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/µs
				85°C		4		
				− 40°C		6.7		
			V_{IPP} = 5.5 V	25°C		4.6		
				85°C		3.5		
				− 40°C		5.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				85°C		130		
				− 40°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				85°C		1.7		
				− 40°C		3.1		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				85°C		46°		
				− 40°C		52°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				125°C		2.3		
				− 55°C		4.7		
			V_{IPP} = 2.5 V	25°C		2.9		
				125°C		2		
				− 55°C		3.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				125°C		230		
				− 55°C		400		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				125°C		1.1		
				− 55°C		2.9		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				125°C		41°		
				− 55°C		49°		

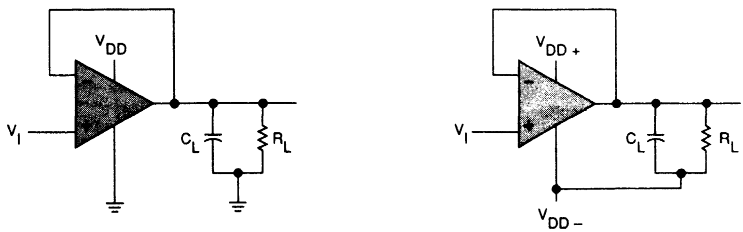
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				125°C		3.1		
				− 55°C		7.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				125°C		2.7		
				− 55°C		6.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				125°C		110		
				− 55°C		280		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				125°C		1.6		
				− 55°C		3.4		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				125°C		44°		
				− 55°C		52°		

PARAMETER MEASUREMENT INFORMATION

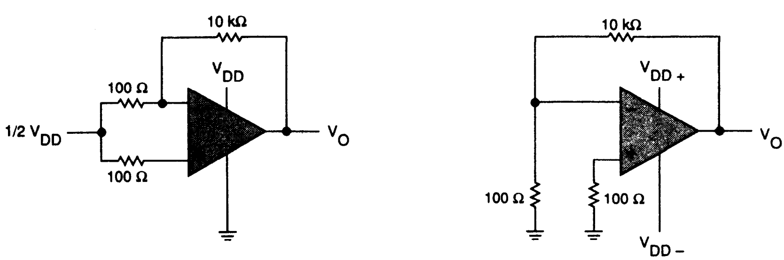
single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

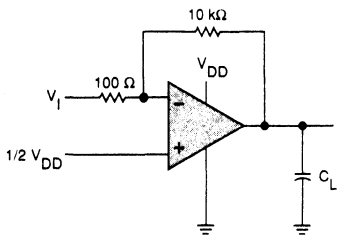
FIGURE 1. UNITY-GAIN AMPLIFIER



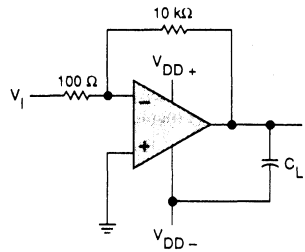
(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply



(b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

Input bias current

Because of the high input impedance of the TLC272 and TLC277 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

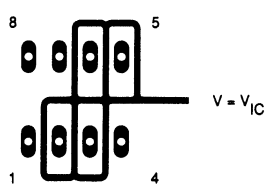


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (P AND JG DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

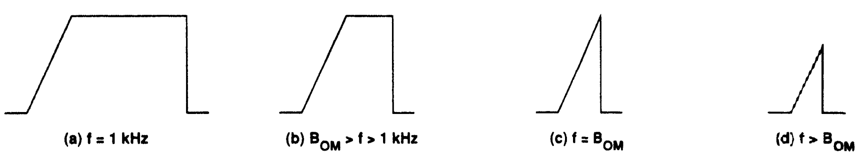


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

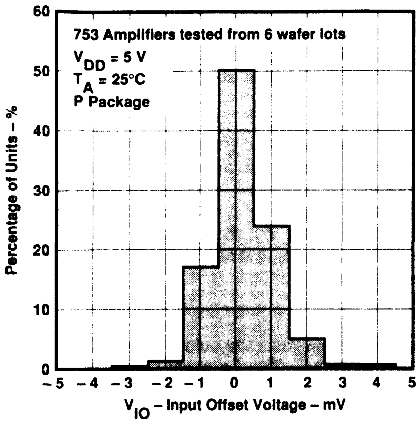


FIGURE 6

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

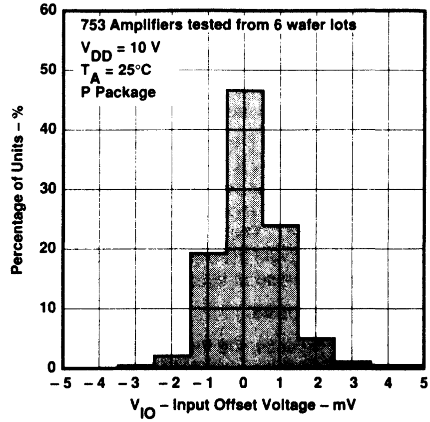


FIGURE 7

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

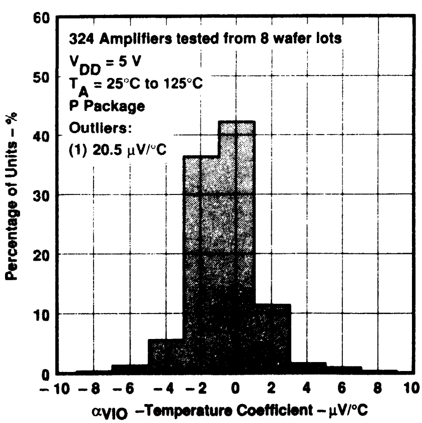


FIGURE 8

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

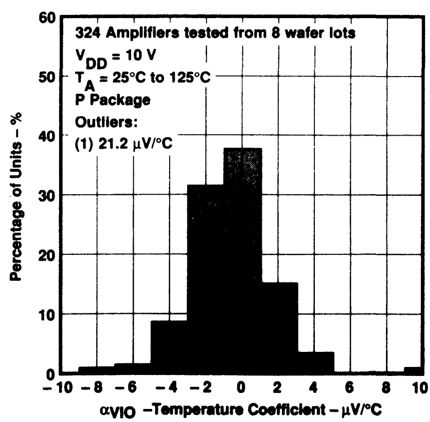


FIGURE 9

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

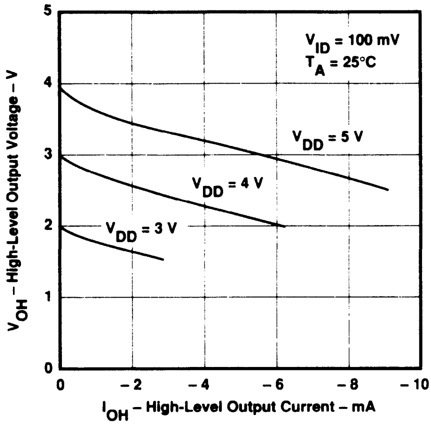


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

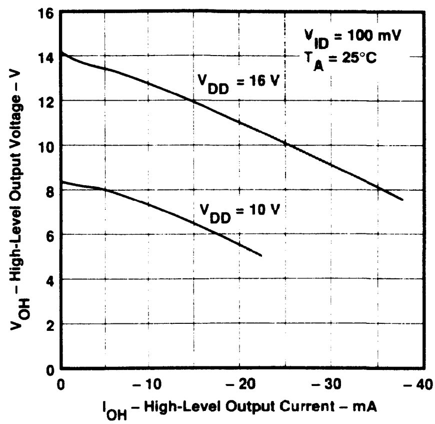


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

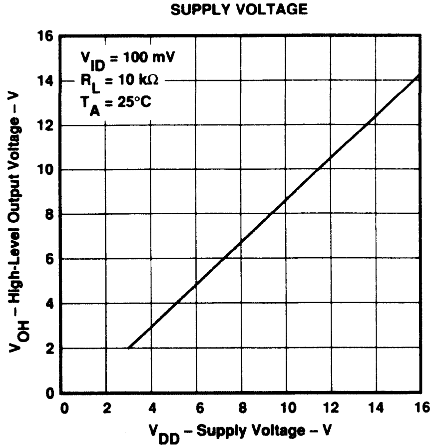


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

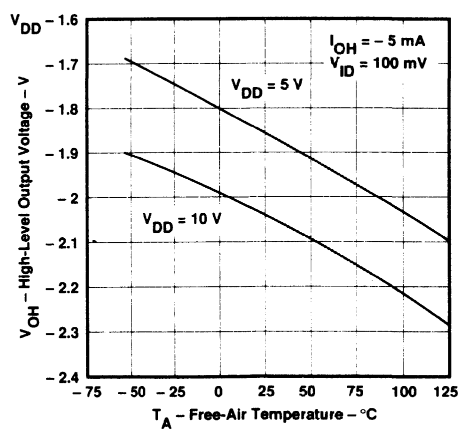


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

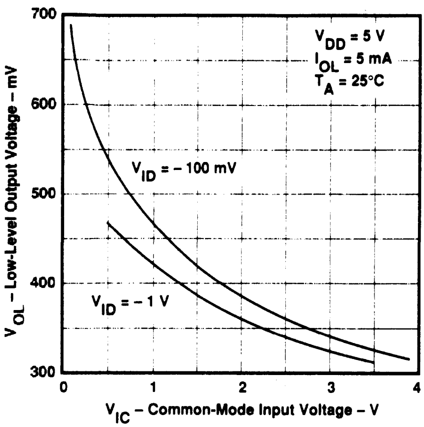


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

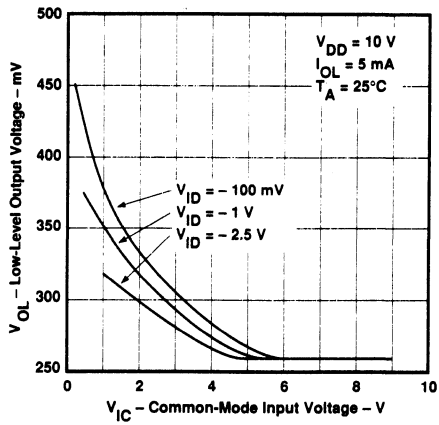


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

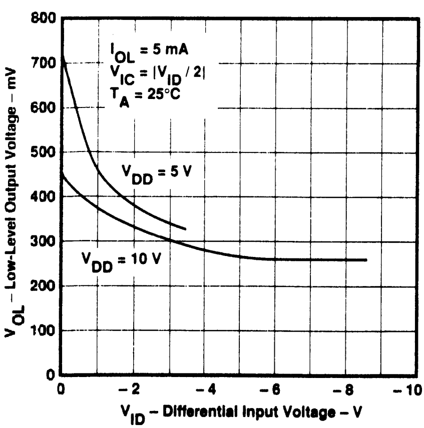


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

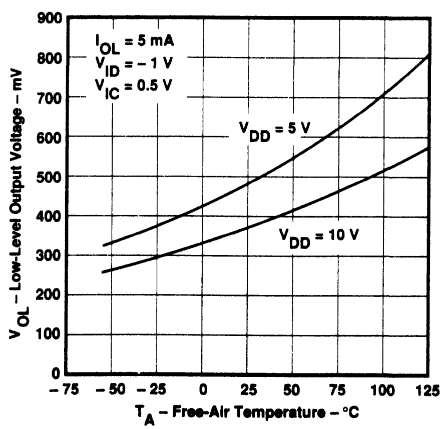


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

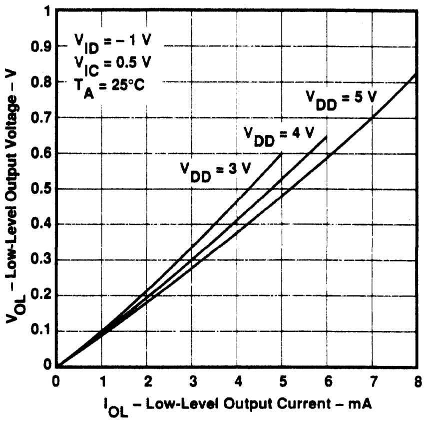


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

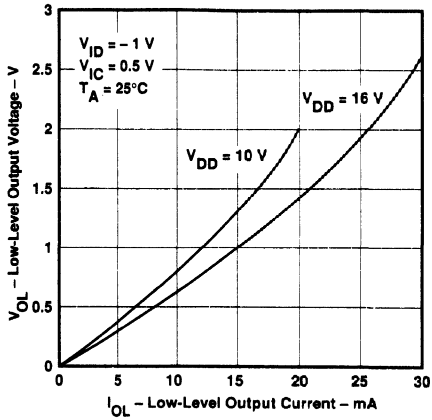


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

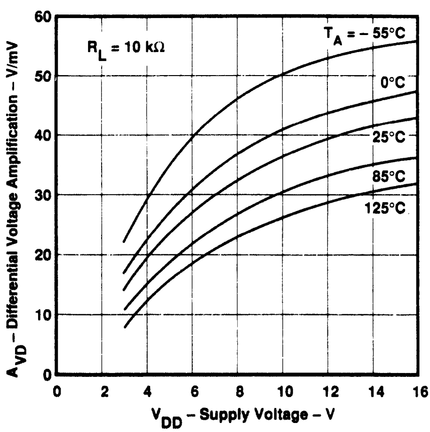


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

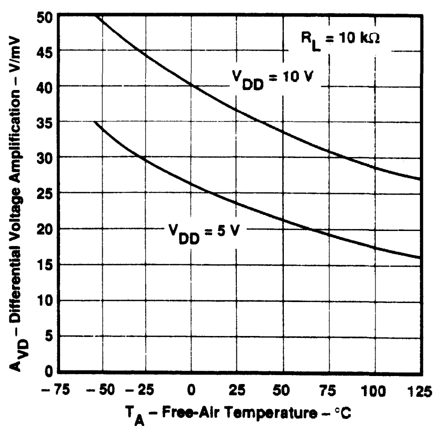


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

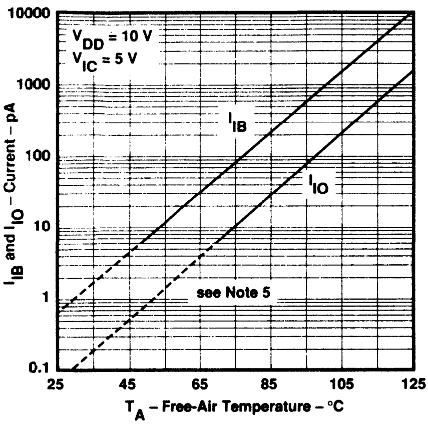


FIGURE 22

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

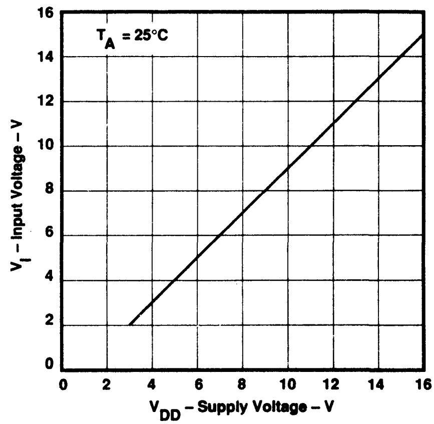


FIGURE 23

SUPPLY CURRENT vs SUPPLY VOLTAGE

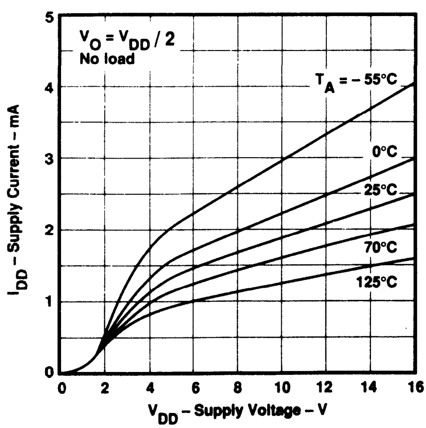


FIGURE 24

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

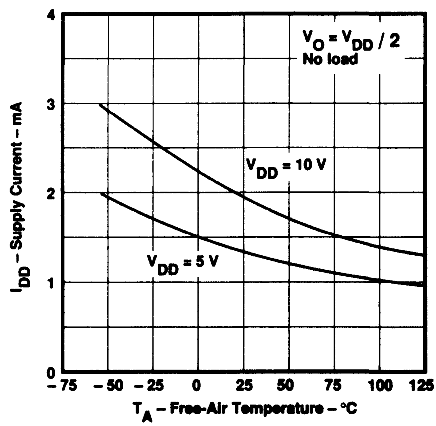


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

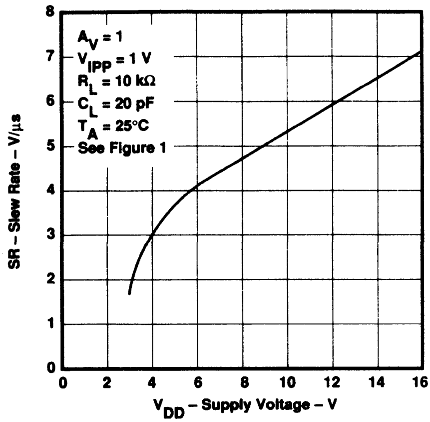


FIGURE 26

SLEW RATE vs FREE-AIR TEMPERATURE

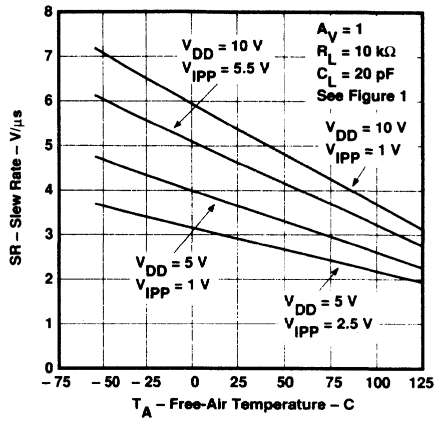


FIGURE 27

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

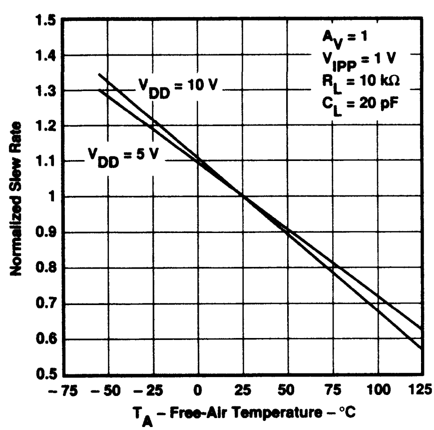


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

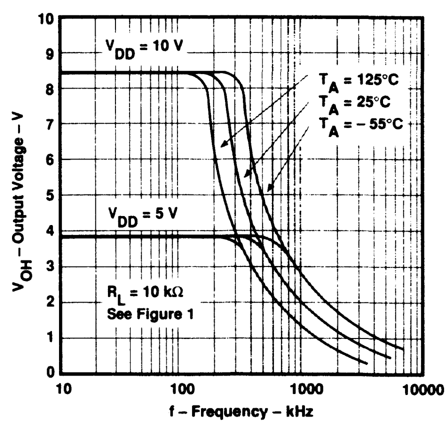


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

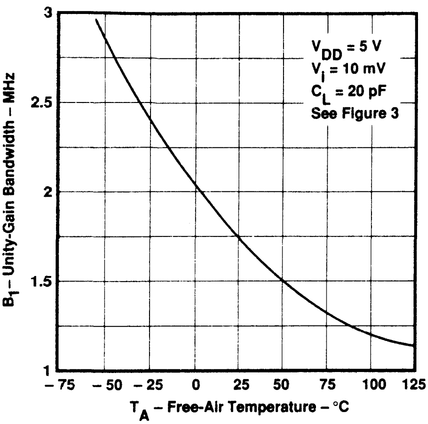


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

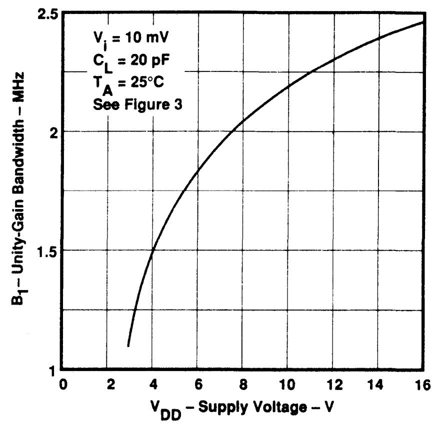


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

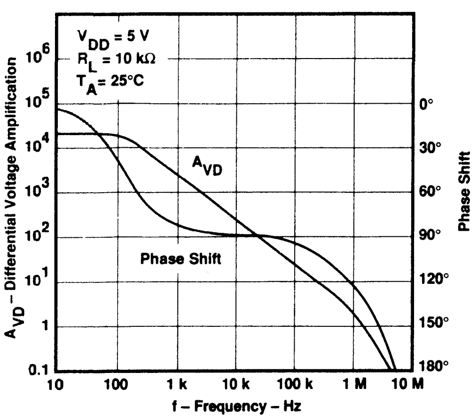


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

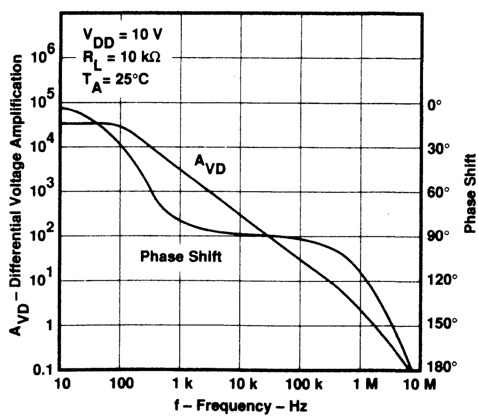


FIGURE 33

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

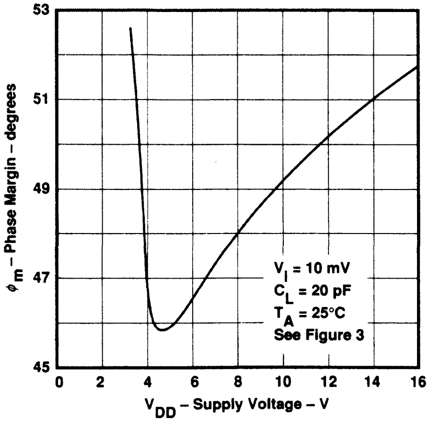


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

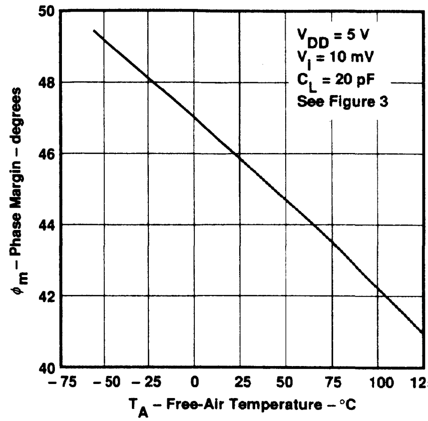


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

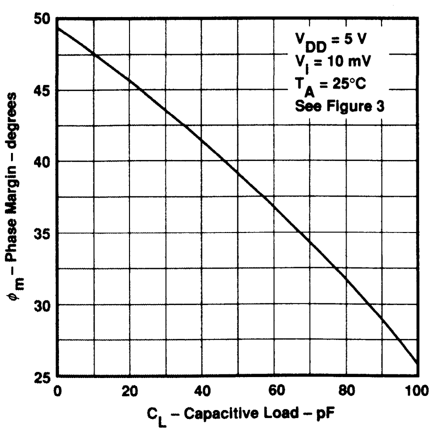


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

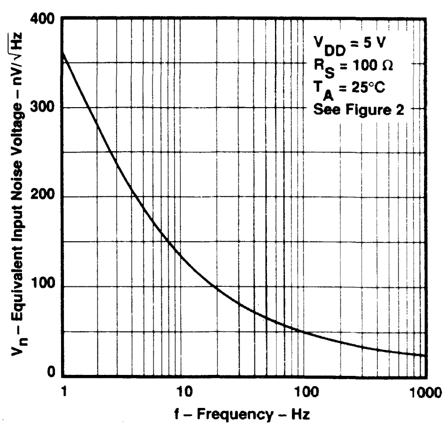


FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC272 and TLC277 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

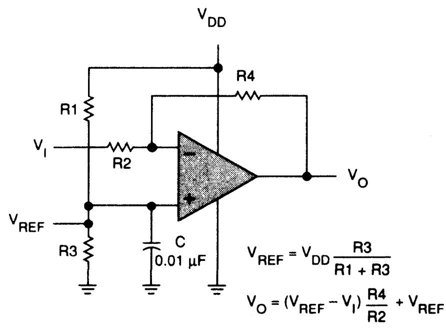
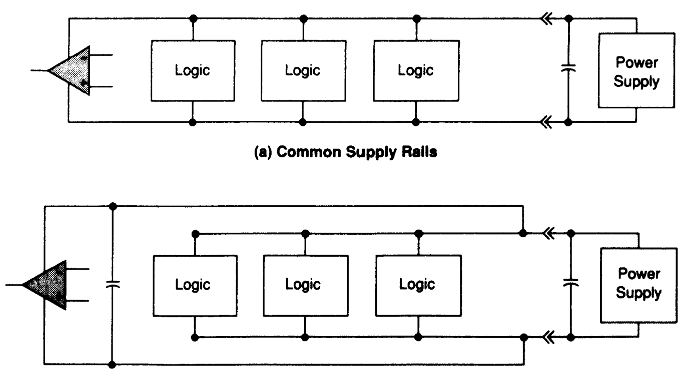


FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails

(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TEXAS INSTRUMENTS

TYPICAL APPLICATION DATA

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

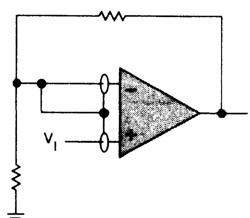
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

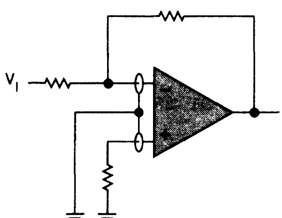
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

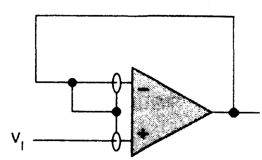
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.

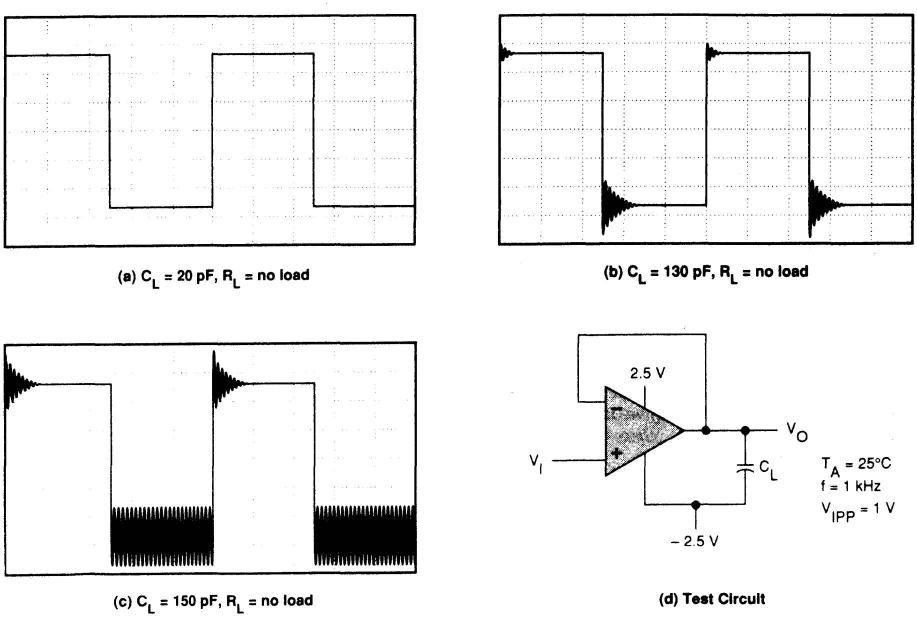


FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R6 acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

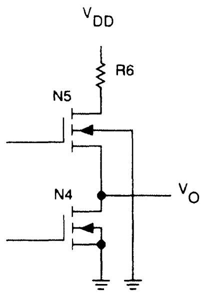


FIGURE 42. TLC272 / TLC277 OUTPUT STAGE

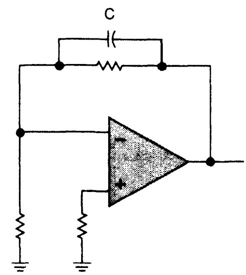


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

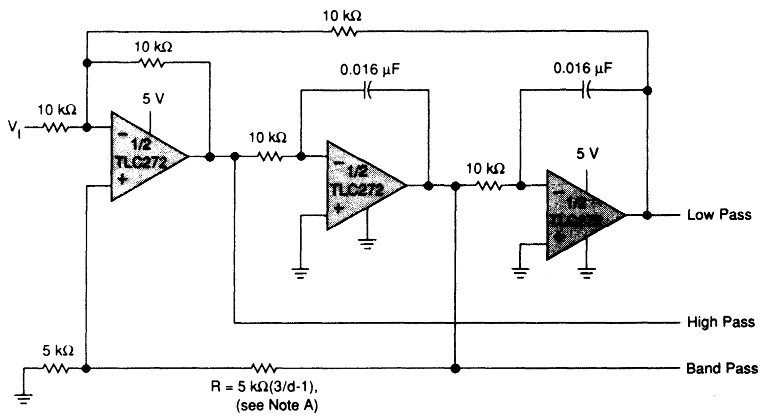
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

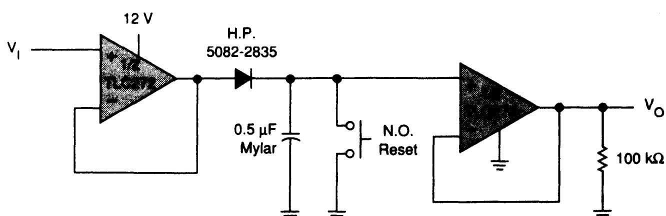
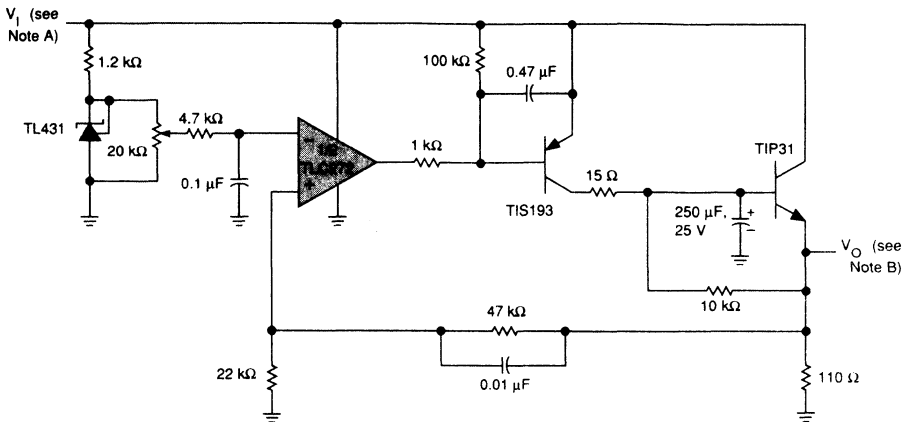


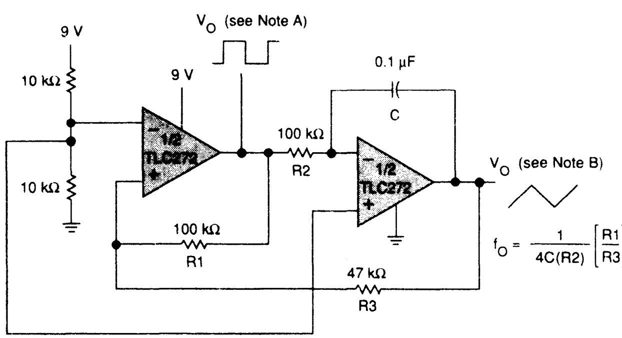
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

FIGURE 46. LOGIC ARRAY POWER SUPPLY

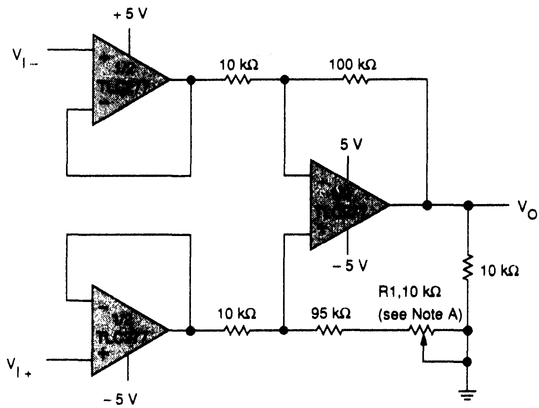


$$f_O = \frac{1}{4C(R2)} \left[\frac{R1}{R3}\right]$$

NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR Adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

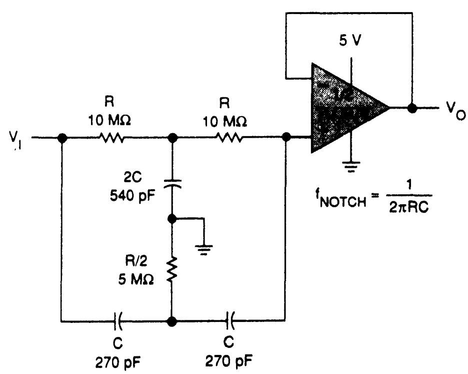
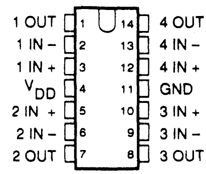


FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

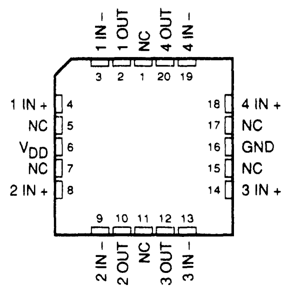
SEPTEMBER 1987

- **Trimmed Offset Voltage:**
  TLC279 . . . 900 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically 0.1 μV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise . . . 25 nV/√Hz Typically at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

N AND J DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

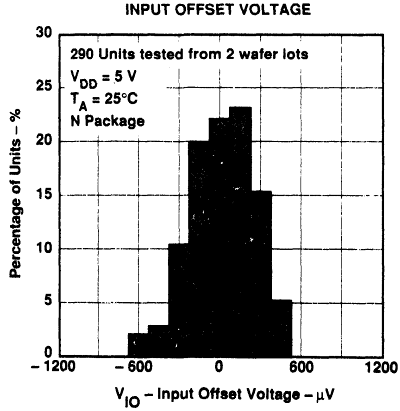
description

The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	900 μV	TLC279CD	TLC279CN	TLC279CJ	—
	2 mV	TLC274BCD	TLC274BCN	TLC274BCJ	—
	5 mV	TLC274ACD	TLC274ACN	TLC274ACJ	—
	10 mV	TLC274CD	TLC274CN	TLC274CJ	—
– 40°C to 85°C	900 μV	TLC279ID	TLC279IN	TLC279IJ	—
	2 mV	TLC274BID	TLC274BIN	TLC274BIJ	—
	5 mV	TLC274AID	TLC274AIN	TLC274AIJ	—
	10 mV	TLC274ID	TLC274IN	TLC274IJ	—
– 55°C to 125°C	900 μV	—	—	TLC279MJ	TLC279MFK
	10 mV	—	—	TLC274MJ	TLC274MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC279CDR).

DISTRIBUTION OF TLC279
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

TEXAS INSTRUMENTS

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC274 (10 mV) to the high-precision TLC279 (900 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are avaliable on LinCMOS operational amplifiers, without the power penalities of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single supply operation making them ideally suited for remote and inaccessable battery-powered applications. The common-mode input voltage range includes the negative rail.

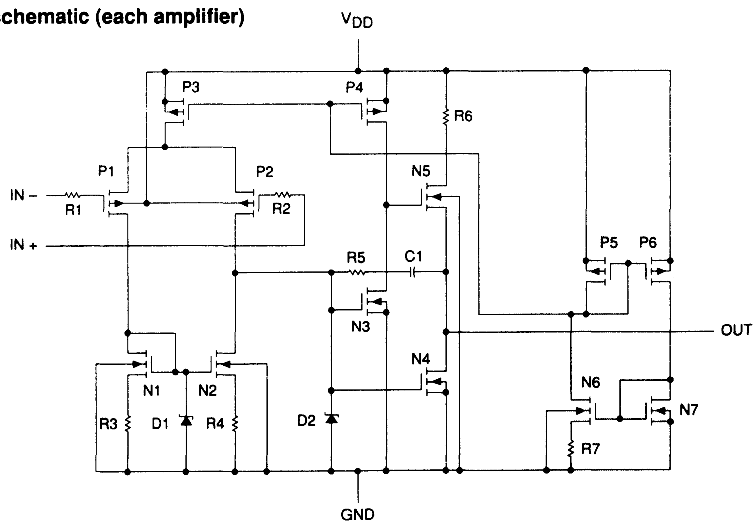
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC274 and TLC279 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... -0.3 V to V_{DD}
Input current, I_I .... ± 5 mA
Output current, I_O (each output) .... ± 30 mA
Total current into V_{DD} terminal .... 45 mA
Total current out of ground terminal .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types .... 0°C to 70°C
I-suffix types .... – 40°C to 85°C
M-suffix types .... – 55°C to 125°C
Storage temperature range .... – 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package .... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I- suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
J (M- suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M-SUFFIX TYPES			I-SUFFIX TYPES			C-SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	– 0.2		3.5	– 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	– 0.2		8.5	– 0.2		8.5	V
Input voltage, V_I	V_{DD} = 5 V	0		3.5	– 0.2		3.5	– 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	– 0.2		8.5	– 0.2		8.5	V
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC274AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC274BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		340	2000	µV
				Full range			3000	µV
		TLC279C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	µV
				Full range			1500	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	− 0.2 to 4	− 0.3 to 4.2		V
				Full range	− 0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				70°C	3	3.8		V
				0°C	3	3.8		V
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				70°C	4	20		V/mV
				0°C	4	27		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				70°C	60	85		dB
				0°C	60	84		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		dB
				0°C	60	94		dB
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		2.7	6.4	mA
				70°C		2.3	5.2	mA
				0°C		3.1	7.2	mA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC274AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC274BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		390	2000	µV
				Full range			3000	
		TLC279C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				70°C	7.8	8.4		
				0°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				70°C	7.5	32		
				0°C	7.5	42		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				70°C	60	88		
				0°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				70°C	60	96		
				0°C	60	94		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		3.8	8	mA
				70°C		3	6.8	
				0°C		4.5	8.8	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC274AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	
				Full range			7	
		TLC274BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		340	2000	μV
				Full range			3500	
		TLC279I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				85°C	3	3.8		
				−40°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				85°C	3.5	19		
				−40°C	3.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				85°C	60	86		
				−40°C	60	81		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		
				−40°C	60	92		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		2.7	6.4	mA
				85°C		2.1	4.8	
				−40°C		3.8	8.8	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

TEXAS INSTRUMENTS

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			13	mV
		TLC274AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.9	5	mV
				Full range			7	mV
		TLC274BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		390	2000	µV
				Full range			3500	µV
		TLC279I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	µV
				Full range			2900	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				85°C	7.8	8.5		V
				−40°C	7.8	8.5		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	mV
				−40°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				85°C	7	31		V/mV
				−40°C	7	46		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				85°C	60	88		dB
				−40°C	60	87		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				85°C	60	96		dB
				−40°C	60	92		dB
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		3.8	8	mA
				85°C		2.9	6.4	mA
				−40°C		5.5	10	mA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC279M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		320	900	µV
				Full range			3750	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 4	−0.3 to 4.2		V
				Full range	0.0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		V
				125°C	3	3.8		
				−55°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	23		V/mV
				125°C	3.5	16		
				−55°C	3.5	35		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	80		dB
				125°C	60	84		
				−55°C	60	81		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		
				−55°C	60	90		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		2.7	6.4	mA
				125°C		1.9	4.4	
				−55°C		4	10	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC279M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		370	1200	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.2		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 9	− 0.3 to 9.2		V
				Full range	0.0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	8	8.5		V
				125°C	7.8	8.4		
				− 55°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 10 kΩ	25°C	10	36		V/mV
				125°C	7	27		
				− 55°C	7	50		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	85		dB
				125°C	60	86		
				− 55°C	60	87		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		dB
				125°C	60	97		
				− 55°C	60	90		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		3.8	8	mA
				125°C		2.5	5.6	
				− 55°C		5.9	12	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

3

Operational Amplifiers

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			C- SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/µs
				70°C		3		
				0°C		3.9		
			V_{IPP} = 2.5 V	25°C		2.9		
				70°C		2.5		
				0°C		3.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				70°C		260		
				0°C		340		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				70°C		1.3		
				0°C		2		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				70°C		43°		
				0°C		47°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			C- SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/µs
				70°C		4.3		
				0°C		5.9		
			V_{IPP} = 5.5 V	25°C		4.6		
				70°C		3.8		
				0°C		5.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				70°C		140		
				0°C		220		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				70°C		1.8		
				0°C		2.5		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				70°C		46°		
				0°C		50°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				85°C		2.8		
				−40°C		4.5		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
				−40°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				85°C		250		
				−40°C		380		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				85°C		1.2		
				−40°C		2.6		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				85°C		43°		
				−40°C		49°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				85°C		4		
				−40°C		6.7		
			V_{IPP} = 5.5 V	25°C		4.6		
				85°C		3.5		
				−40°C		5.8		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				85°C		130		
				−40°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				85°C		1.7		
				−40°C		3.1		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				85°C		46°		
				−40°C		52°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/µs
				125°C		2.3		
				− 55°C		4.7		
			V_{IPP} = 2.5 V	25°C		2.9		
				125°C		2		
				− 55°C		3.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		320		kHz
				125°C		230		
				− 55°C		400		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		1.7		MHz
				125°C		1.1		
				− 55°C		2.9		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		46°		
				125°C		41°		
				− 55°C		49°		

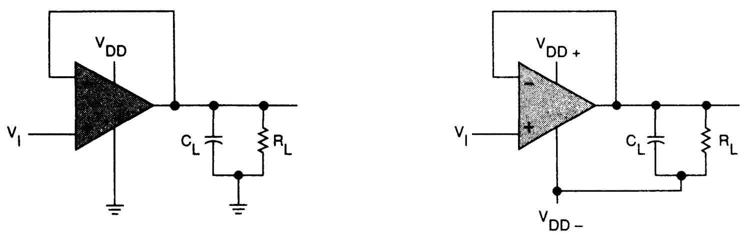
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/µs
				125°C		3.1		
				− 55°C		7.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				125°C		2.7		
				− 55°C		6.1		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 1		25°C		200		kHz
				125°C		110		
				− 55°C		280		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		2.2		MHz
				125°C		1.6		
				− 55°C		3.4		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		49°		
				125°C		44°		
				− 55°C		52°		

PARAMETER MEASUREMENT INFORMATION

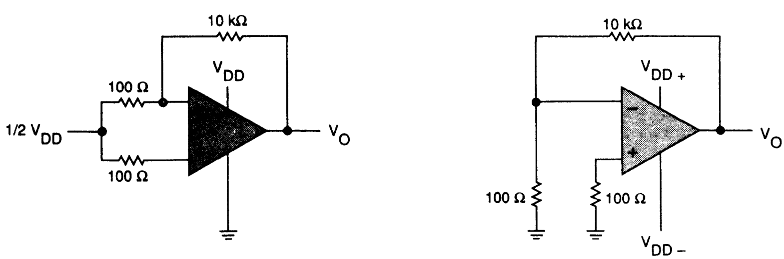
single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

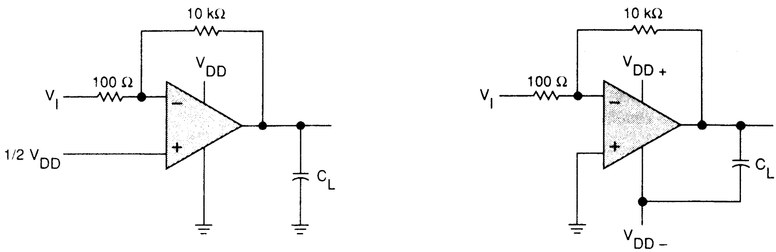
FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC274 and TLC279 op amps, attempts to measure the input bias current can result in erroneous readings. The typical bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. This can be achieved by using a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket. This can be achieved by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

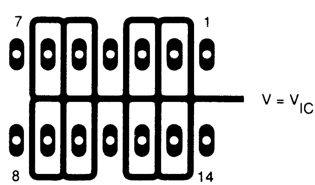


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(N AND J DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

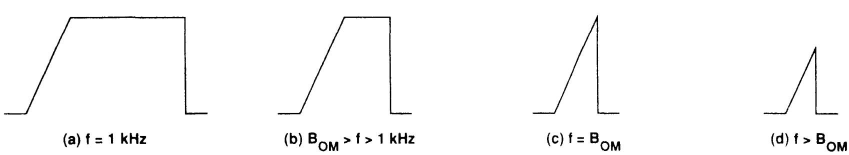


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

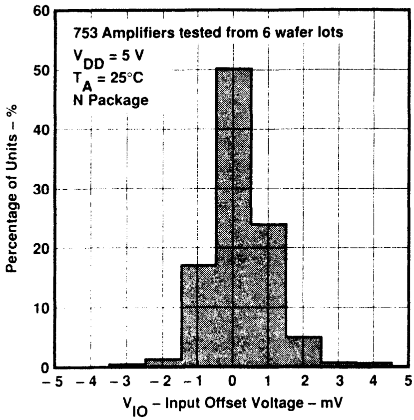


FIGURE 6

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

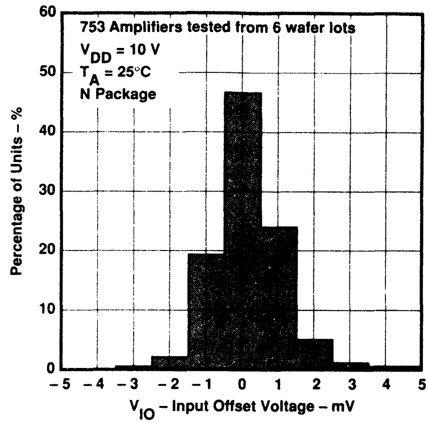


FIGURE 7

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

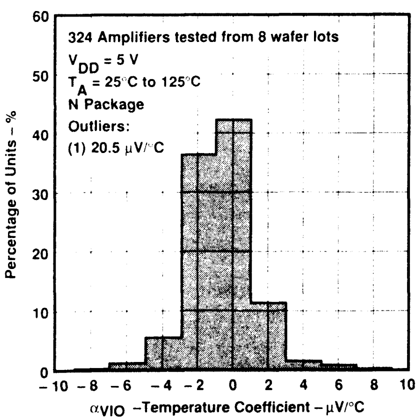


FIGURE 8

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

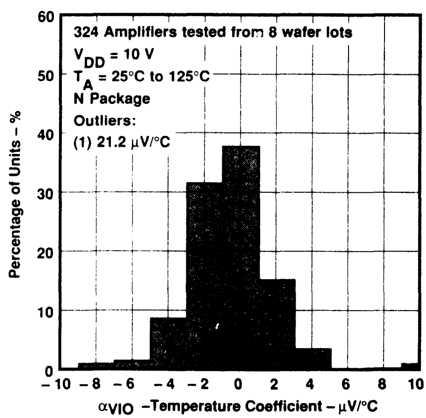


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

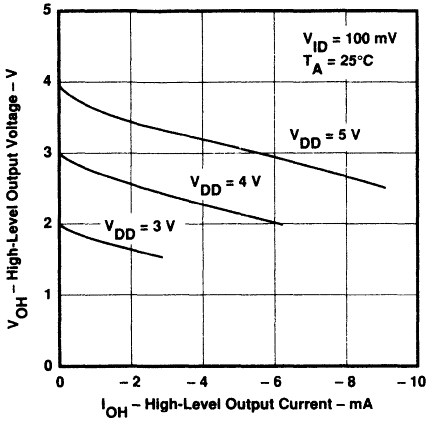


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

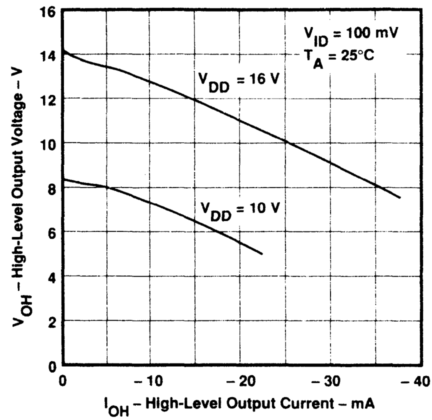


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

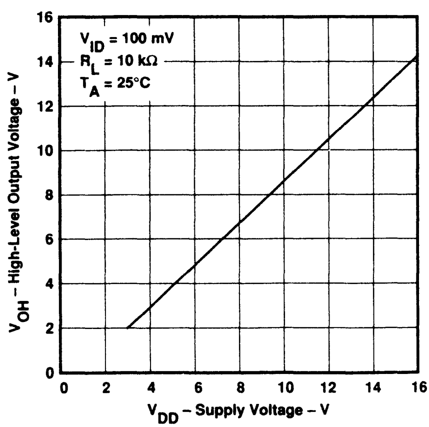


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

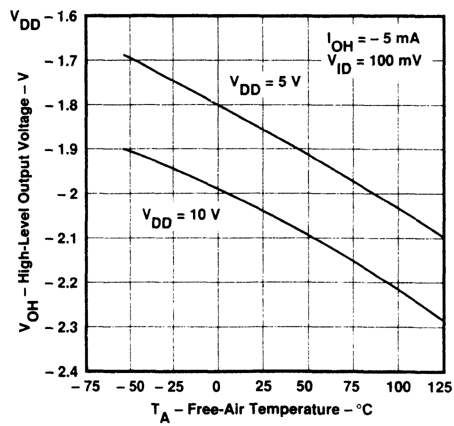


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

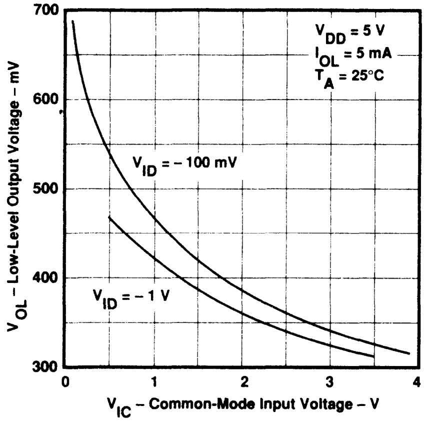


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

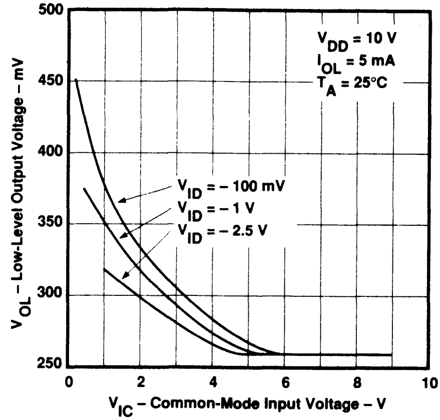


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

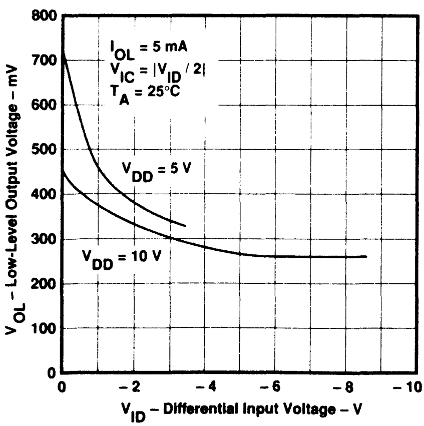


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

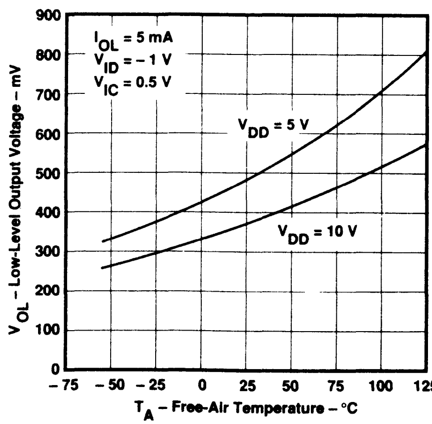


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

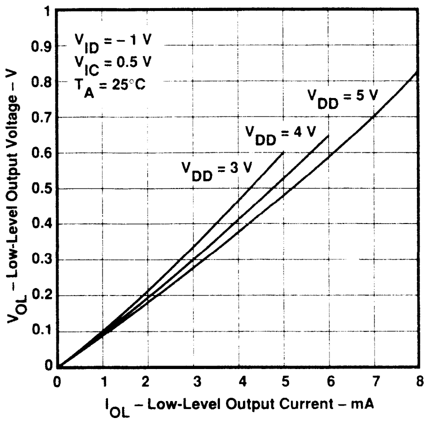


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

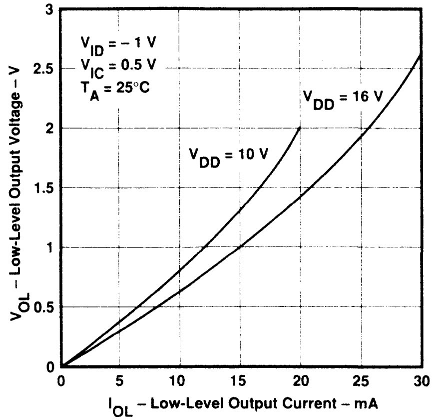


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

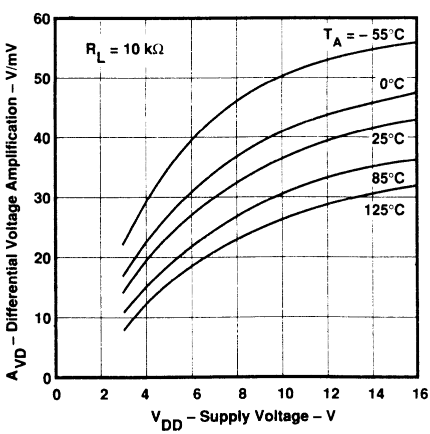


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

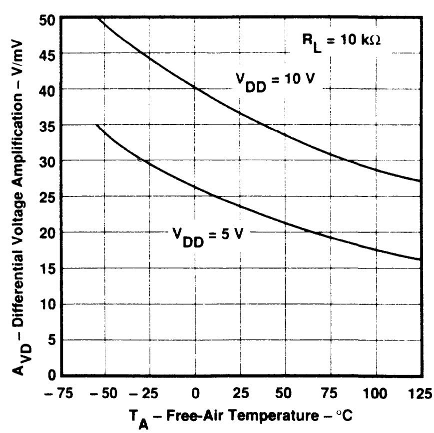


FIGURE 21

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

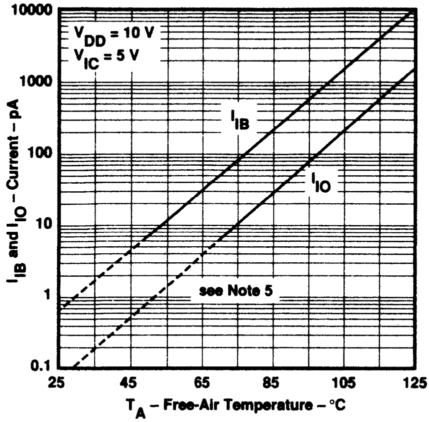


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

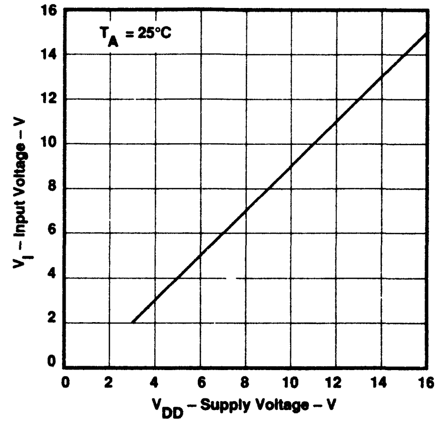


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

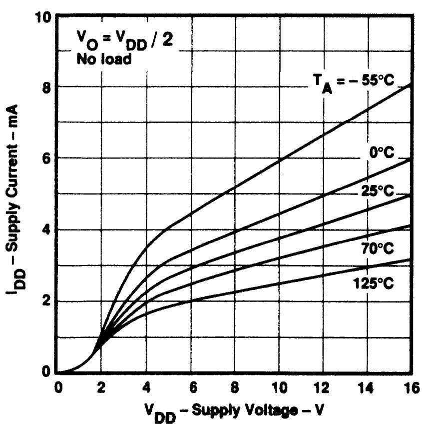


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

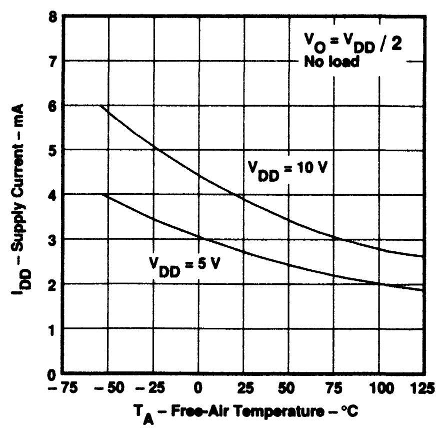


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

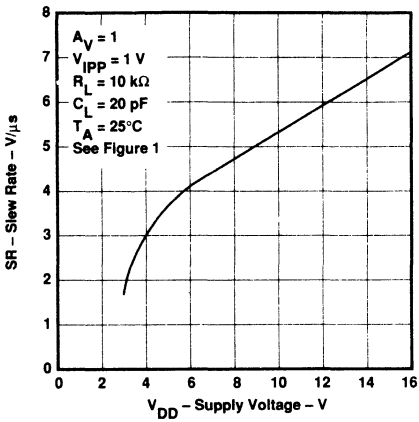


FIGURE 26

SLEW RATE vs FREE-AIR TEMPERATURE

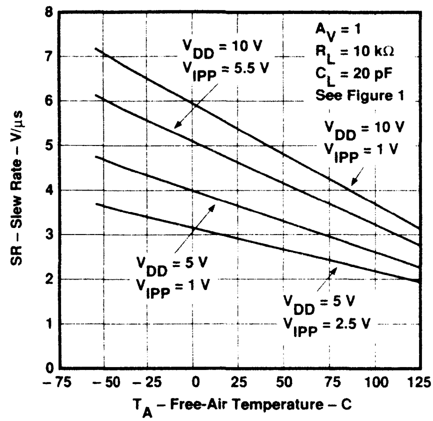


FIGURE 27

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

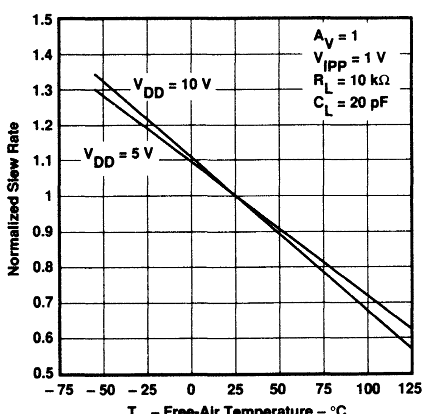


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

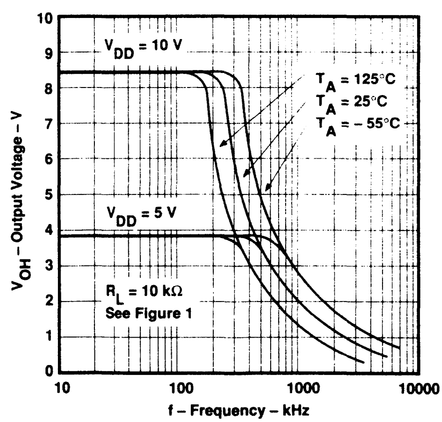


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

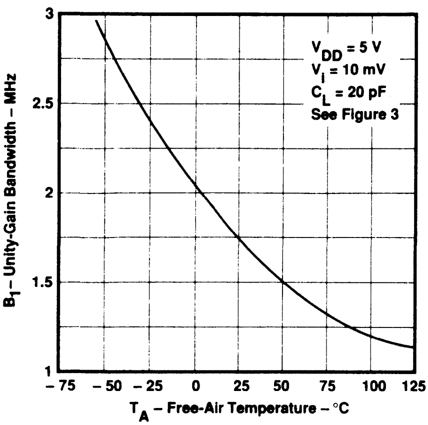


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

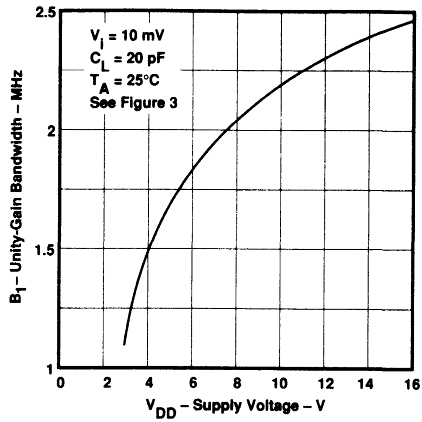


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

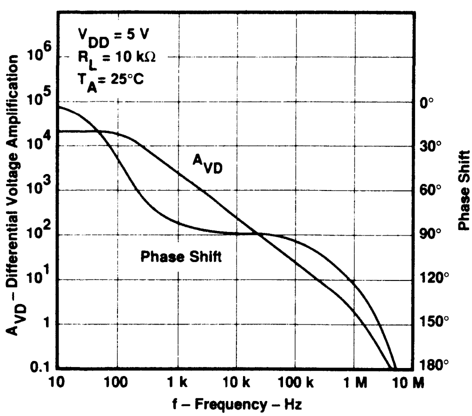


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

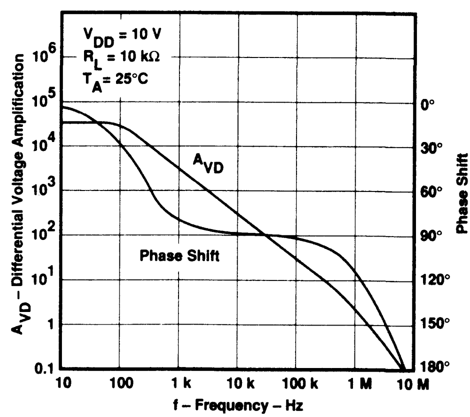


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

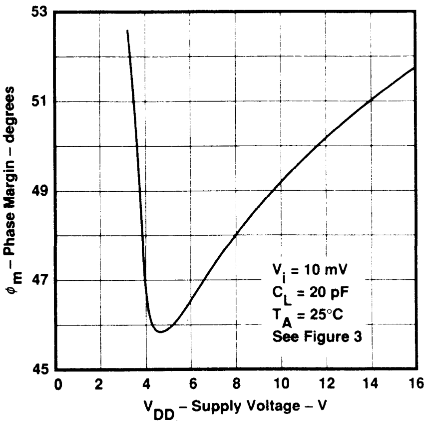


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

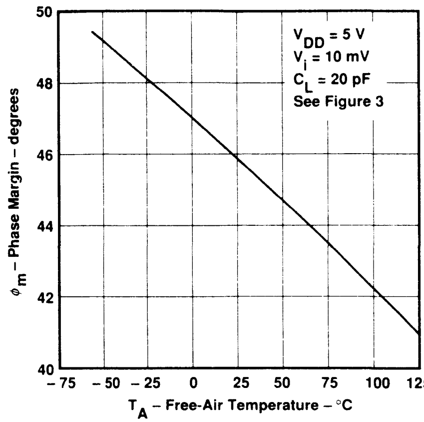


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

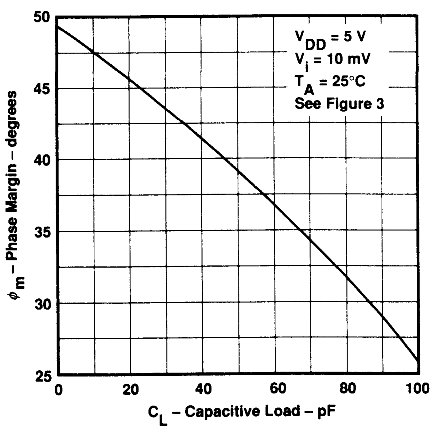


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

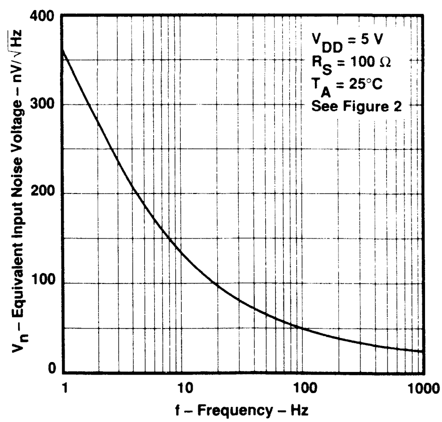


FIGURE 37

3

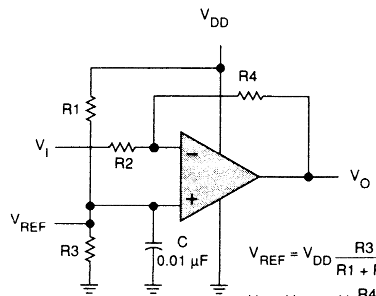
Operational Amplifiers

TYPICAL APPLICATION DATA

single-supply operation

While the TLC274 and TLC279 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.



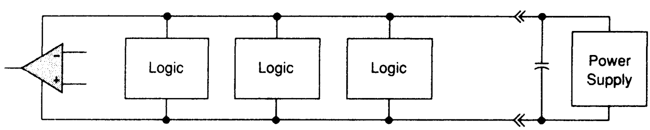
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = V_{REF} - V_I\frac{R4}{R2}$$

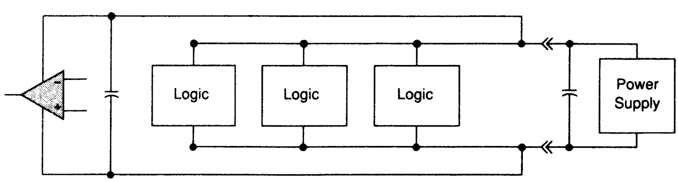
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-$ 1 V at T_A = 25°C and at $V_{DD}-$ 1.5 V at all other temperatures.

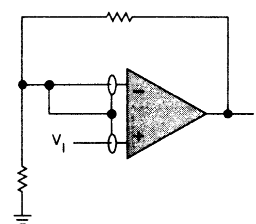
The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

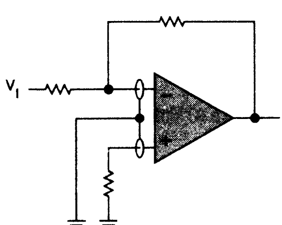
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

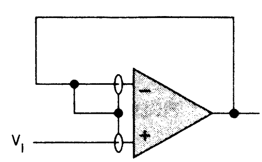
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

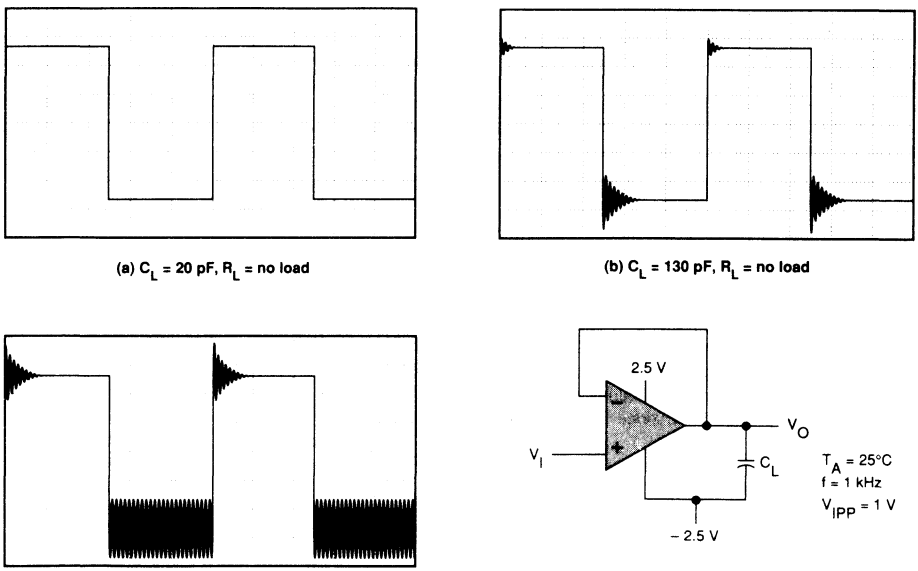
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

output characteristics

The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



(a) C_L = 20 pF, R_L = no load

(b) C_L = 130 pF, R_L = no load

(c) C_L = 150 pF, R_L = no load

(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R6 acts as a drain load to N4 and the gain of the opamp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

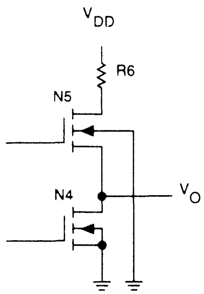


FIGURE 42. TLC274 / TLC279 OUTPUT STAGE

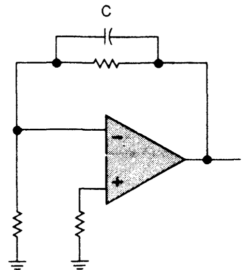


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequsite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capactive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

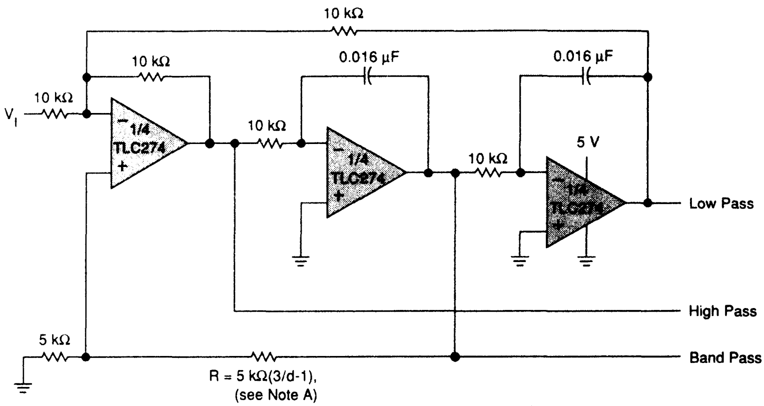
The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages at or below 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as is possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

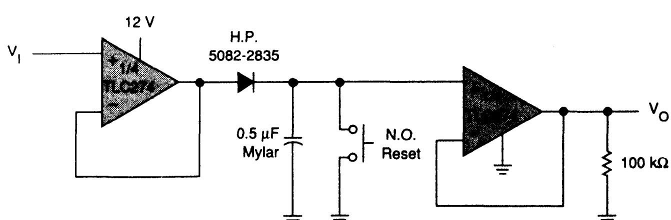
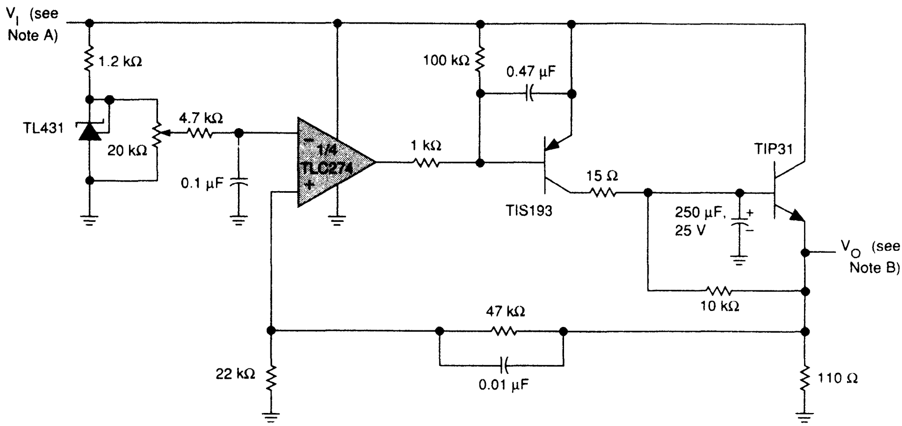


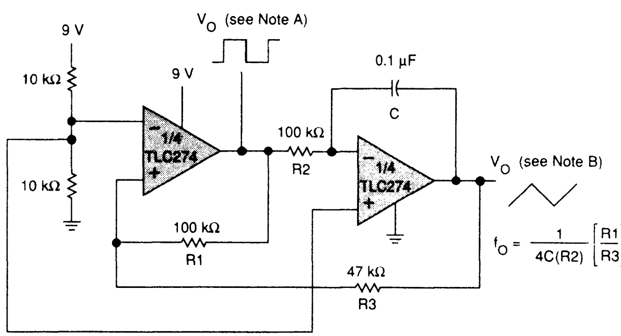
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

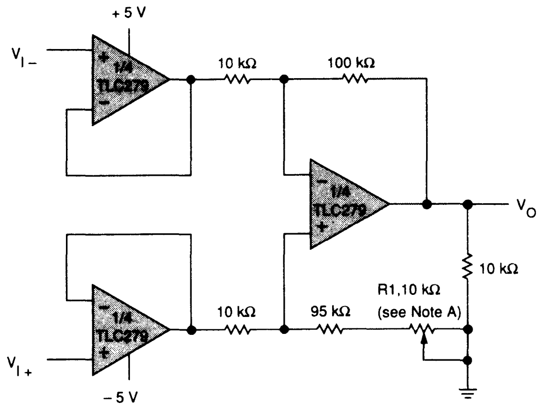
FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR Adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

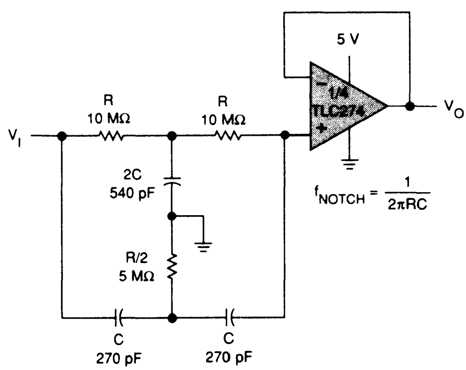
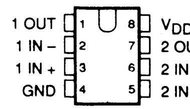


FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

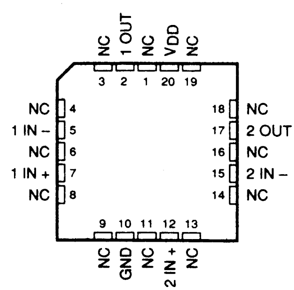
OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC27L7 . . . 500 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically 0.1 μV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Ultra-Low Power . . . 95 μW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-In Latchup Immunity**

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)

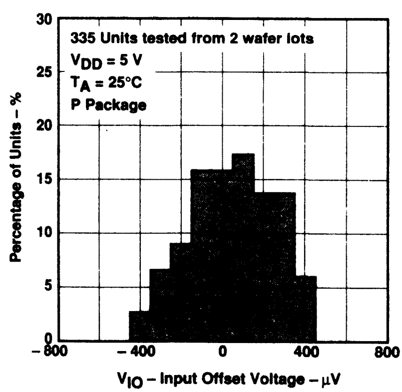


NC – No internal connection

description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

DISTRIBUTION OF TLC27L7
INPUT OFFSET VOLTAGE



T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	500 μV	TLC27L7CD	TLC27L7CP	TLC27L7CJG	——
	2 mV	TLC27L2BCD	TLC27L2BCP	TLC27L2BCJG	——
	5 mV	TLC27L2ACD	TLC27L2ACP	TLC27L2ACJG	——
	10 mV	TLC27L2CD	TLC27L2CP	TLC27L2CJG	——
– 40°C to 85°C	500 μV	TLC27L7ID	TLC27L7IP	TLC27L7IJG	——
	2 mV	TLC27L2BID	TLC27L2BIP	TLC27L2BIJG	——
	5 mV	TLC27L2AID	TLC27L2AIP	TLC27L2AIJG	——
	10 mV	TLC27L2ID	TLC27L2IP	TLC27L2IJG	——
– 55°C to 125°C	500 μV	——	——	TLC27L7MJG	TLC27L7MFK
	10 mV	——	——	TLC27L2MJG	TLC27L2MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27L7CDR).

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications . Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single supply operation and ultra-low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

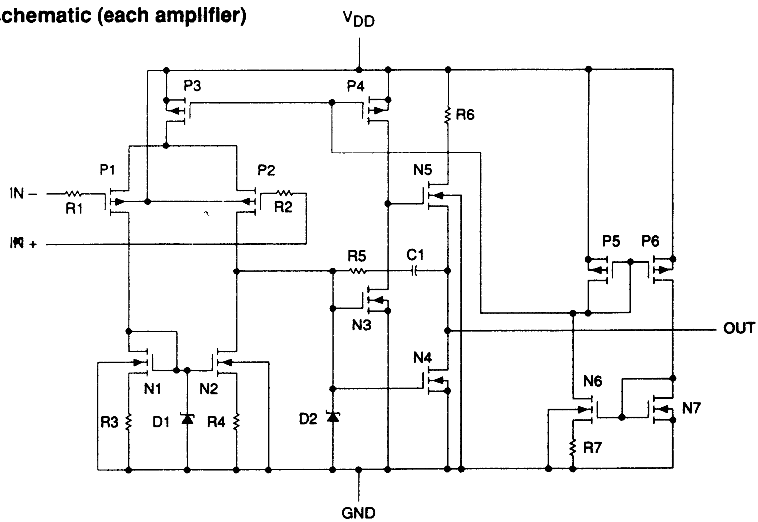
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC27L2 and TLC27L7 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... -0.3 V to V_{DD}
Input current, I_I .... ± 5 mA
Output current, I_O (each output) .... ± 30 mA
Total current into V_{DD} terminal .... 45 mA
Total current out of ground terminal .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types .... 0°C to 70°C
I-suffix types .... − 40°C to 85°C
M-suffix types .... − 55°C to 125°C
Storage temperature range .... − 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package .... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		204	2000	µV
				Full range			3000	µV
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	µV
				Full range			1500	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				70°C	3	4.2		V
				0°C	3	4.1		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				70°C	50	380		V/mV
				0°C	50	700		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	95		dB
				0°C	60	95		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		dB
				0°C	60	97		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		19	34	µA
				70°C		15	28	µA
				0°C		24	42	µA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27L2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27L2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	2000	µV
				Full range			3000	µV
		TLC27L7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	µV
				Full range			1900	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				70°C	7.8	8.9		V
				0°C	7.8	8.9		V
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				70°C	50	660		V/mV
				0°C	50	1100		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				70°C	60	97		dB
				0°C	60	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		dB
				0°C	60	97		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		29	46	µA
				70°C		22	40	µA
				0°C		36	66	µA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		204	2000	µV
				Full range			3500	
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				85°C	3	4.2		
				−40°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				85°C	50	330		
				−40°C	50	900		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	95		
				−40°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		
				−40°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		19	34	µA
				85°C		15	26	
				−40°C		31	54	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	mV
		TLC27L2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	mV
				Full range			7	mV
		TLC27L2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		235	2000	μV
				Full range			3500	μV
		TLC27L7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	μV
				Full range			2900	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	− 0.2 to 9	− 0.3 to 9.2		V
				Full range	− 0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				85°C	7.8	8.9		V
				− 40°C	7.8	8.9		V
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	mV
				− 40°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				85°C	50	585		V/mV
				− 40°C	50	1550		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				85°C	60	98		dB
				− 40°C	60	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		dB
				− 40°C	60	97		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		29	46	μA
				85°C		20	36	μA
				− 40°C		49	86	μA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		170	500	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				125°C	3	4.2		
				−55°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				125°C	25	200		
				−55°C	25	950		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	85		
				−55°C	60	95		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				−55°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		19	34	µA
				125°C		14	24	
				−55°C		35	60	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

3 Operational Amplifiers

TEXAS INSTRUMENTS

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		190	800	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	− 0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				125°C	7.8	9		
				− 55°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				125°C	25	380		
				− 55°C	25	1750		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				125°C	60	91		
				− 55°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				− 55°C	60	97		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		29	46	μA
				125°C		18	30	
				− 55°C		56	96	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/µs
				70°C		0.03		
				0°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				70°C		0.02		
				0°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				70°C		4.5		
				0°C		6		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				70°C		65		
				0°C		100		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				70°C		30°		
				0°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/µs
				70°C		0.04		
				0°C		0.05		
			V_{IPP} = 5.5 V	25°C		0.04		
				70°C		0.04		
				0°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				70°C		0.9		
				0°C		1.3		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				70°C		90		
				0°C		125		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				70°C		34°		
				0°C		40°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
				−40°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
				−40°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				85°C		4		
				−40°C		7		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				85°C		55		
				−40°C		130		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				85°C		28°		
				−40°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				85°C		0.03		
				−40°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				85°C		0.03		
				−40°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				85°C		0.8		
				−40°C		1.4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				85°C		80		
				−40°C		155		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				85°C		32°		
				−40°C		42°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				125°C		0.02		
				− 55°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				125°C		0.02		
				− 55°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				125°C		3		
				− 55°C		8		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				125°C		45		
				− 55°C		140		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				125°C		25°		
				− 55°C		39°		

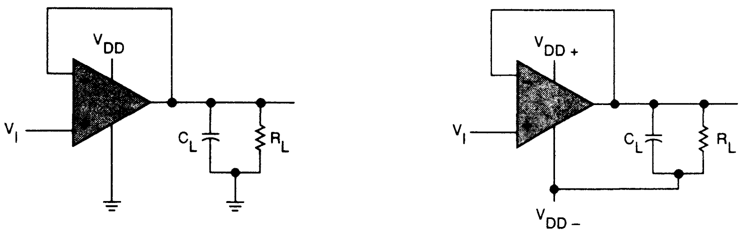
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				125°C		0.03		
				− 55°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				125°C		0.03		
				− 55°C		0.06		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				125°C		0.7		
				− 55°C		1.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				125°C		70		
				− 55°C		165		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				125°C		29°		
				− 55°C		43°		

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

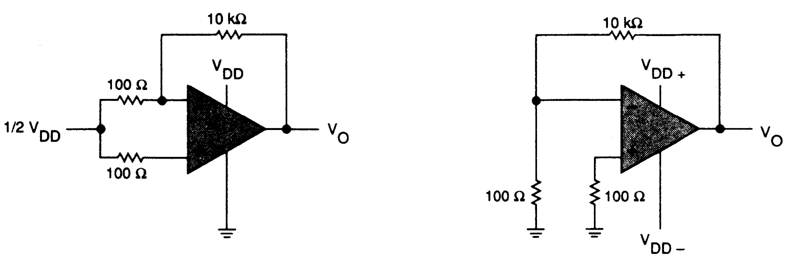
Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply

(b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply

(b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

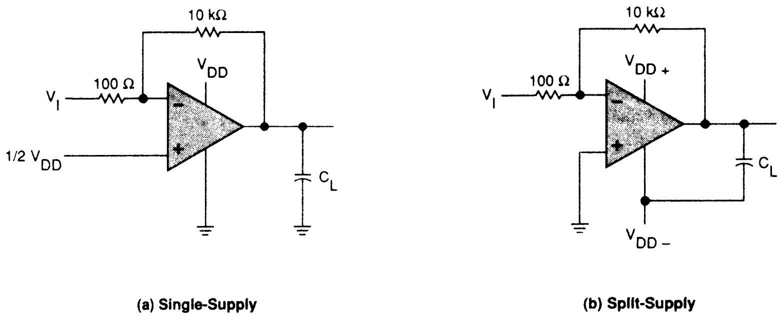


FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

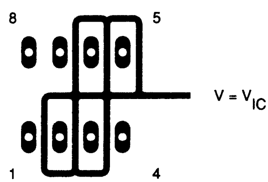


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(JG AND P DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

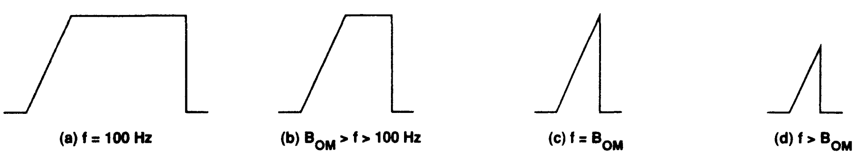


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

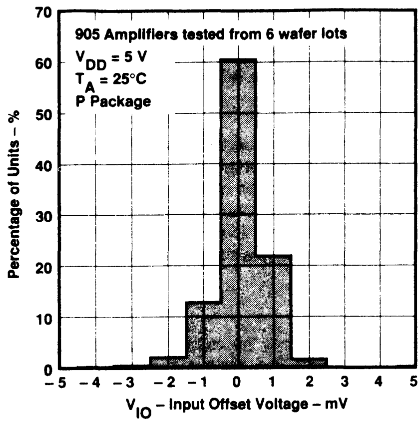


FIGURE 6

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

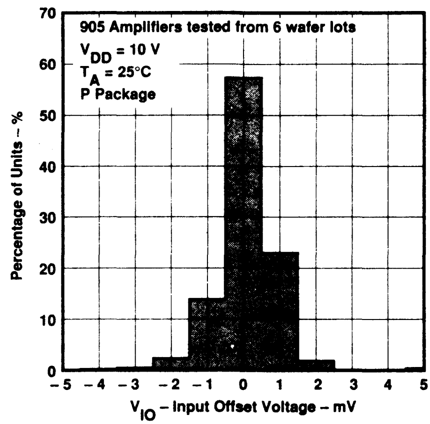


FIGURE 7

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

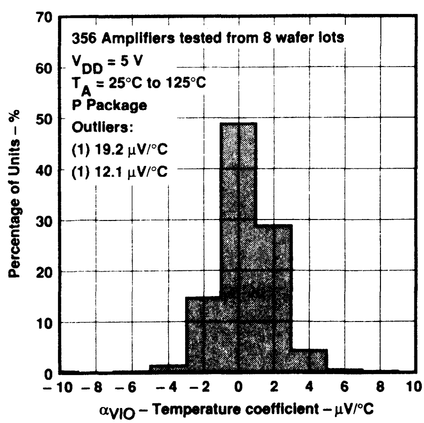


FIGURE 8

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

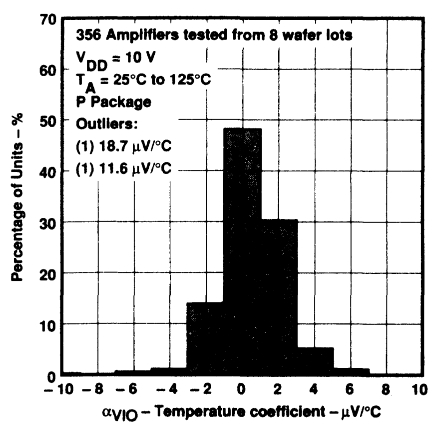


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

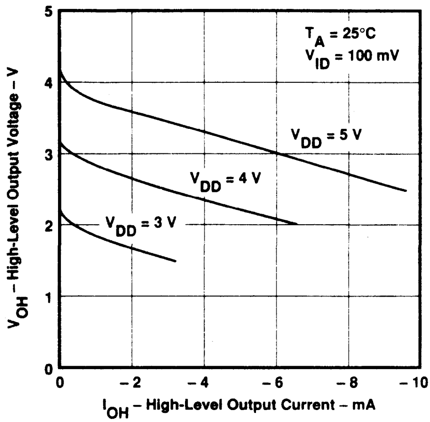


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

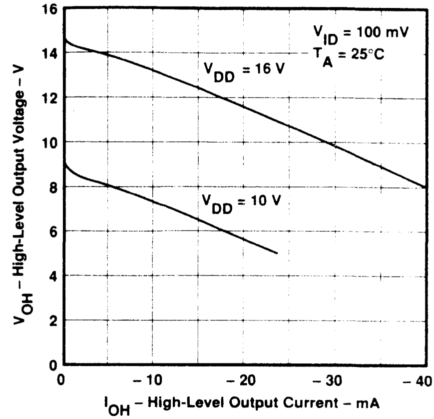


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

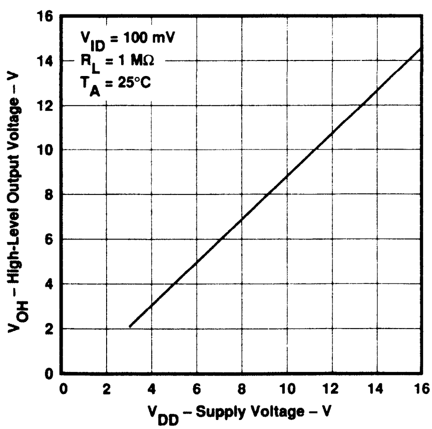


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

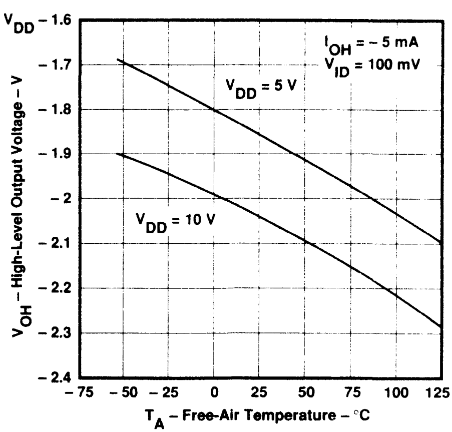


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

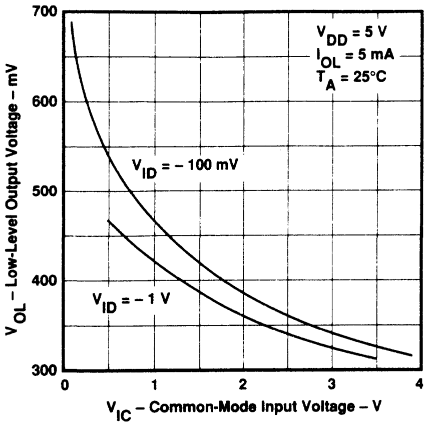


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

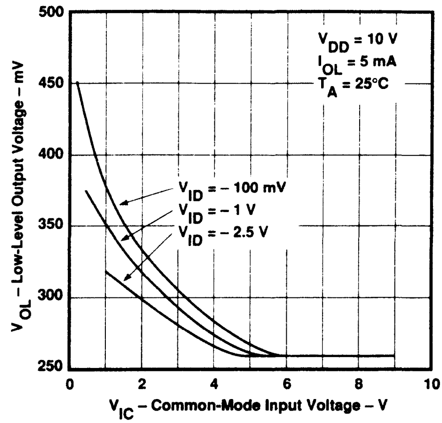


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

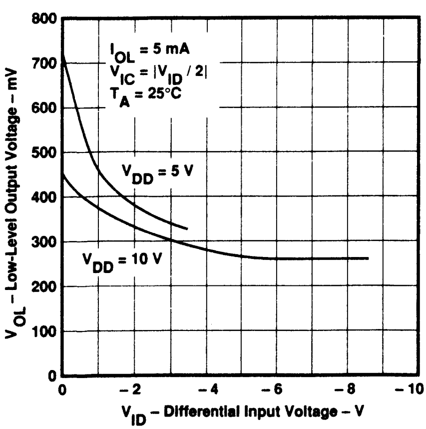


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

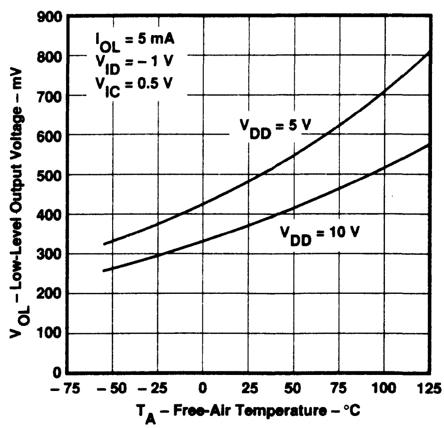


FIGURE 17

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

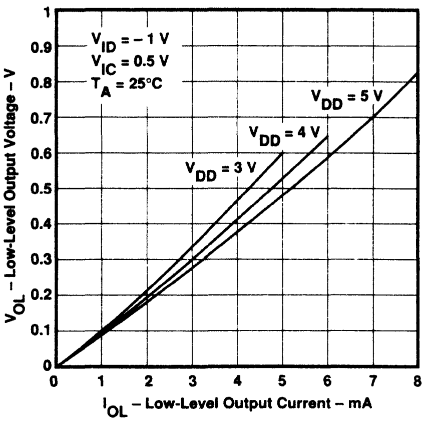


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

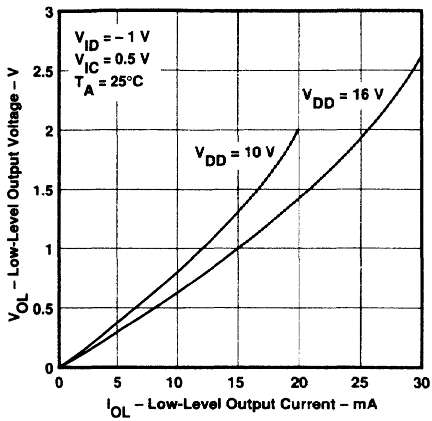


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

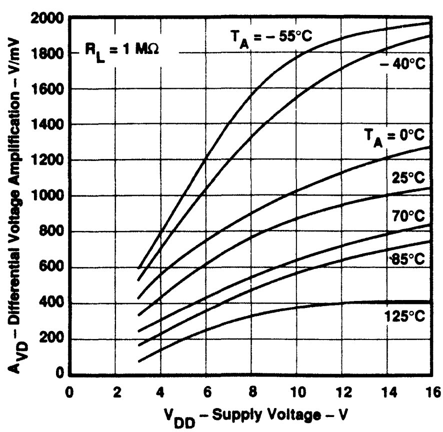


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

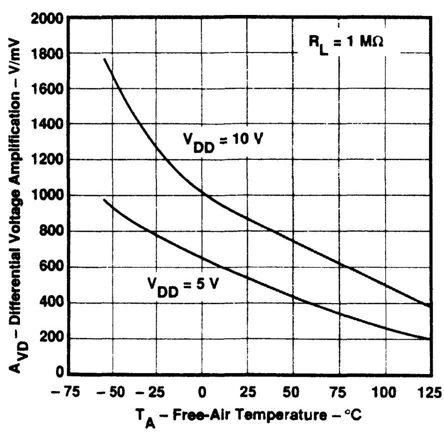


FIGURE 21

3
Operational Amplifiers

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

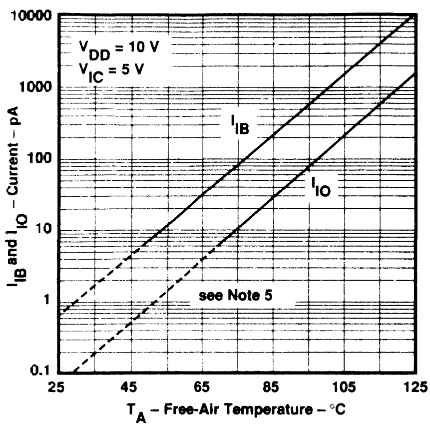


FIGURE 22

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

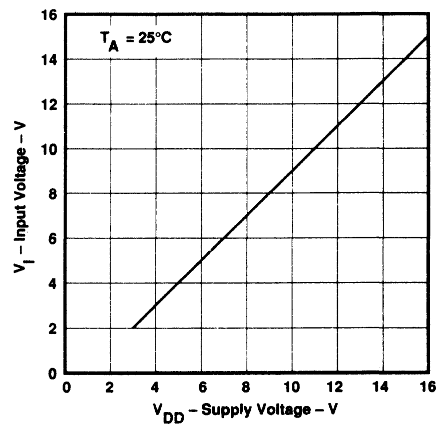


FIGURE 23

SUPPLY CURRENT vs SUPPLY VOLTAGE

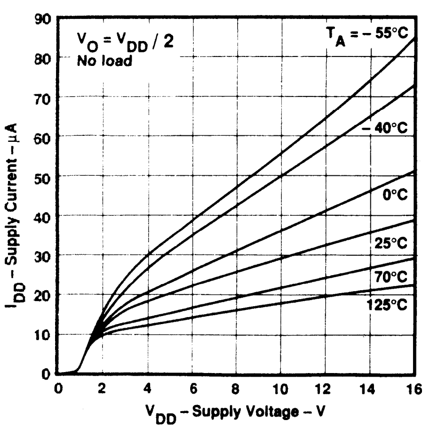


FIGURE 24

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

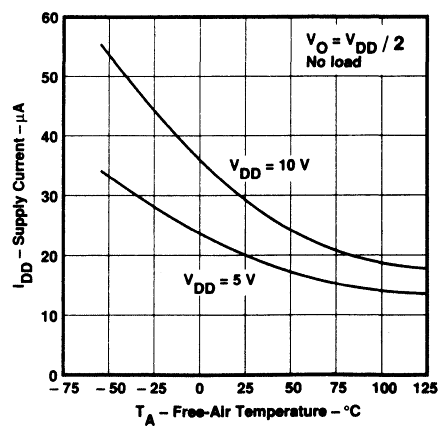


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

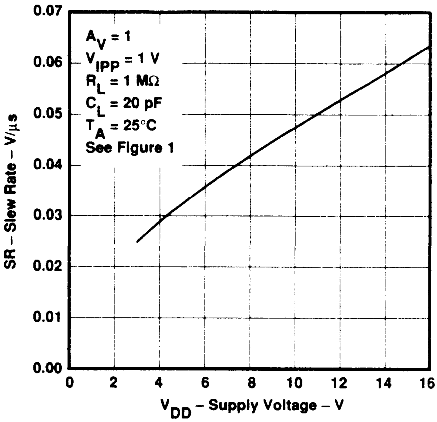


FIGURE 26

SLEW RATE vs FREE-AIR TEMPERATURE

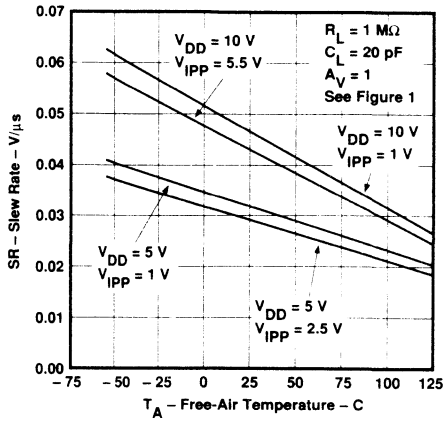


FIGURE 27

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

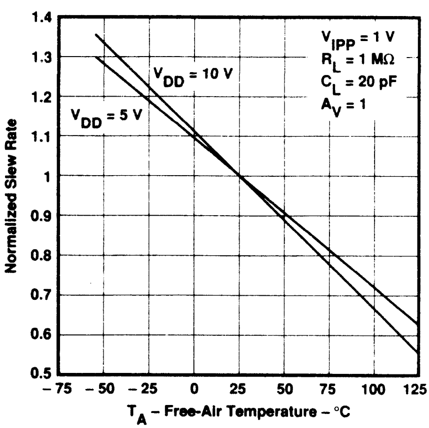


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

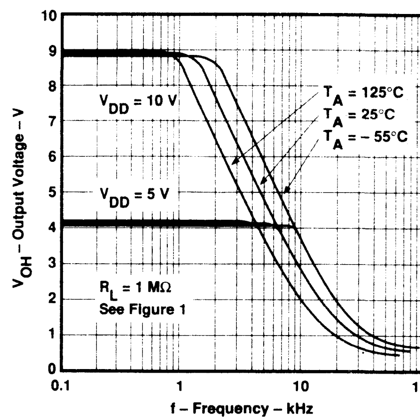


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

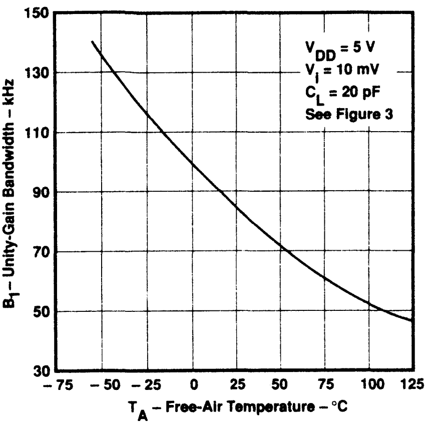


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

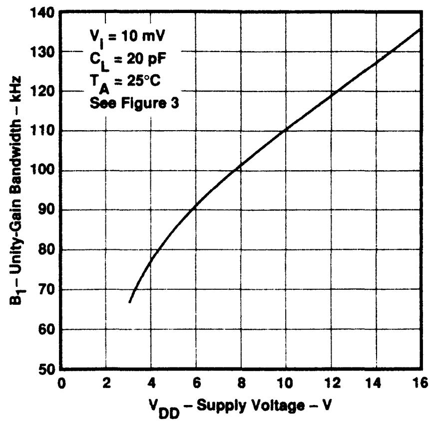


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

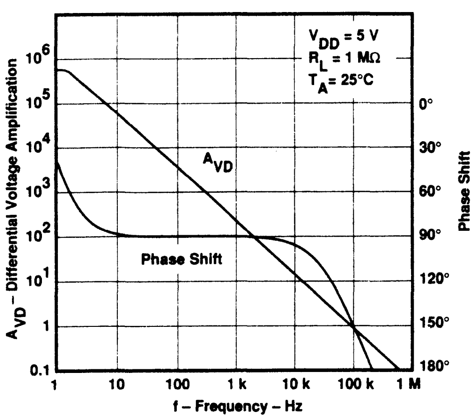


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

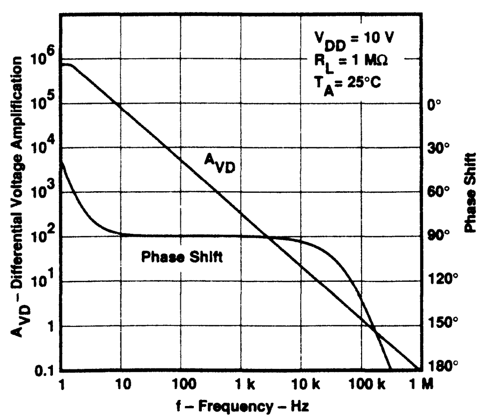


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

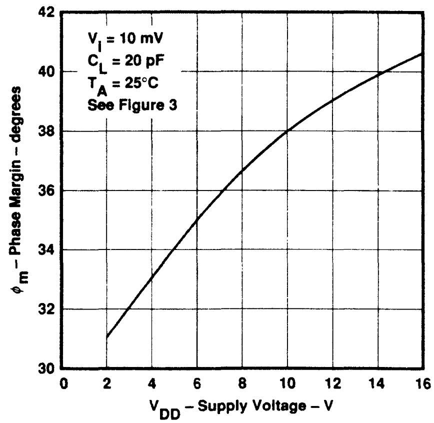


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

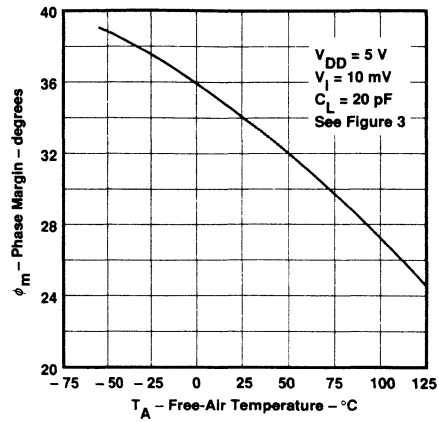


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

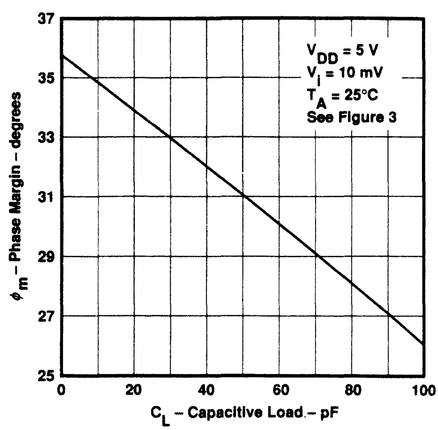


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

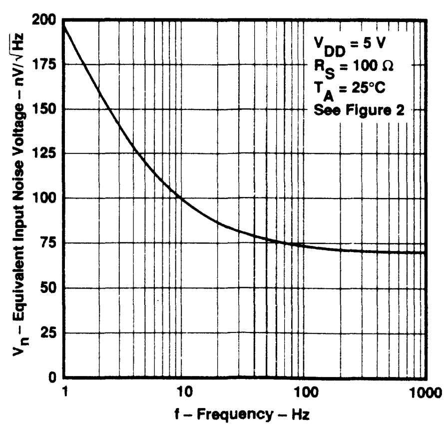


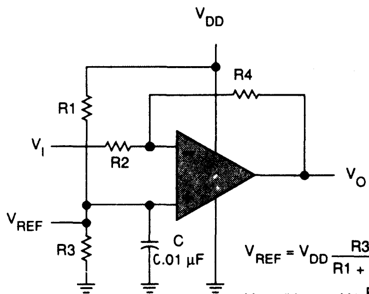
FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27L2 and TLC27L7 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.



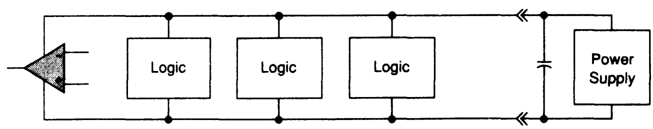
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I)\frac{R4}{R2} + V_{REF}$$

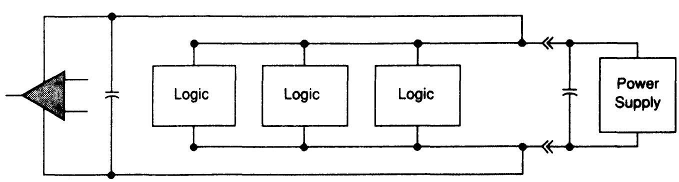
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

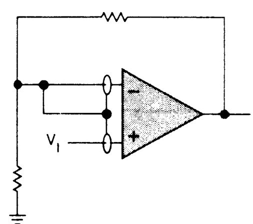
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

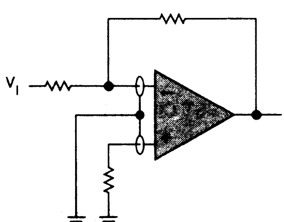
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

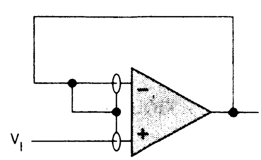
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

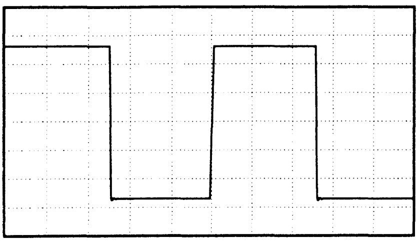
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

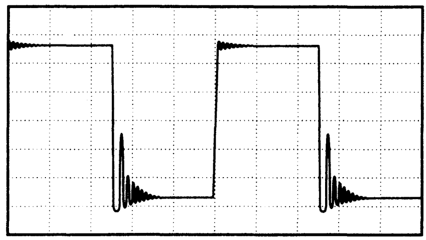
output characteristics

The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

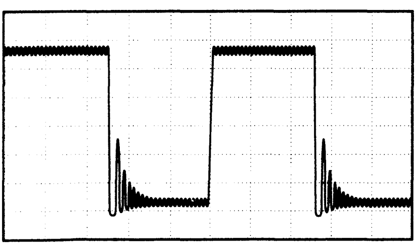
All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



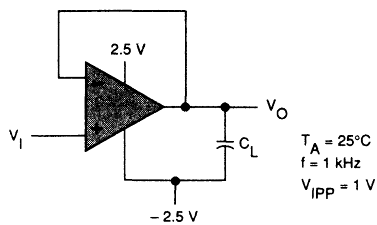
(a) C_L = 20 pF, R_L = no load



(b) C_L = 260 pF, R_L = no load



(c) C_L = 310 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor (R_P) connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

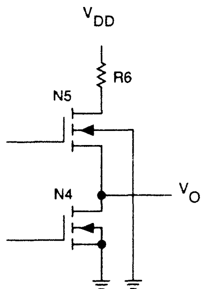


FIGURE 42. TLC27L2 / TLC27L7 OUTPUT STAGE

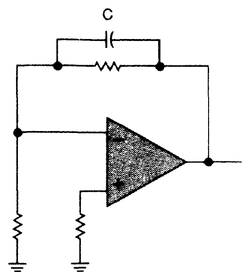


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

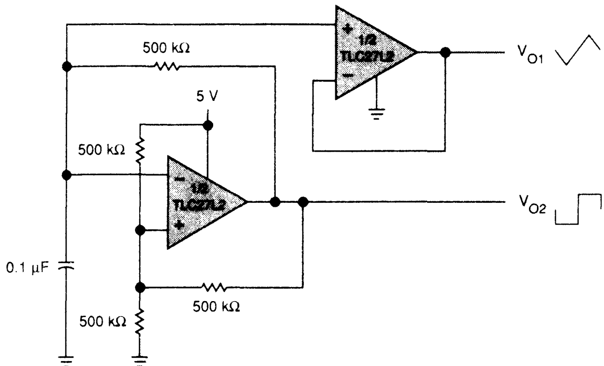
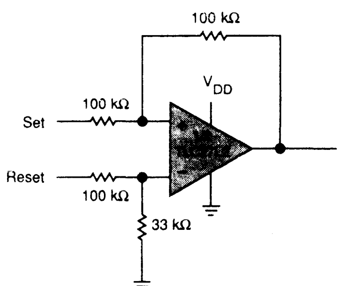


FIGURE 44. MULTIVIBRATOR

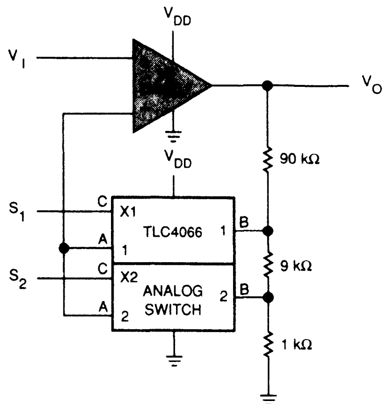


NOTES: V_{DD} = 5 V to 16V

FIGURE 45. SET / RESET FLIP-FLOP

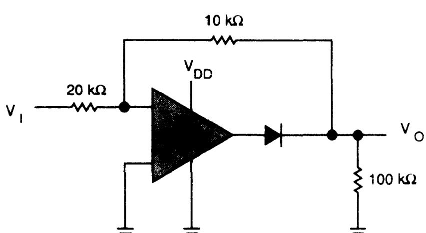
TYPICAL APPLICATION DATA

Select:	S_1	S_2
A_V	10	100



NOTES: V_{DD} = 5 V to 12V

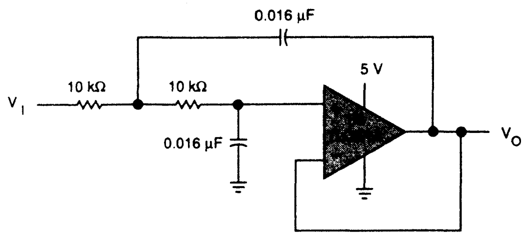
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTES: V_{DD} = 5 V to 16V

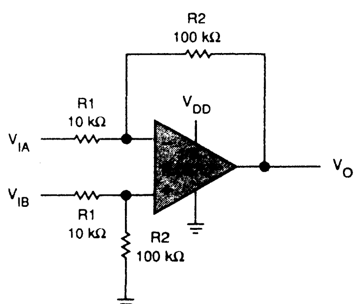
FIGURE 47. FULL WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

$V_O = \frac{R2}{R1} (V_{IB} - V_{IA})$

FIGURE 49. DIFFERENCE AMPLIFIER

3

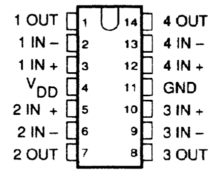
Operational Amplifiers

TEXAS INSTRUMENTS

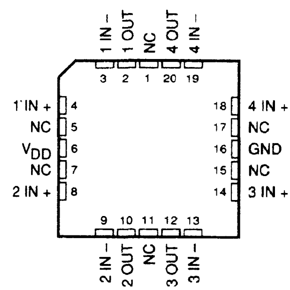
OCTOBER 1987

- **Trimmed Offset Voltage: TLC27L9 . . . 900 μV Max at 25°C, V_{DD} = 5 V**
- **Input Offset Voltage Drift Typically 0.1 μV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  - **– 55°C to125°C . . . 4 V to 16 V**
  - **– 40°C to 85°C . . . 4 V to 16 V**
  - **0°C to 70°C . . . 3 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Ultra-Low Power . . . 195 μW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

N AND J DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)

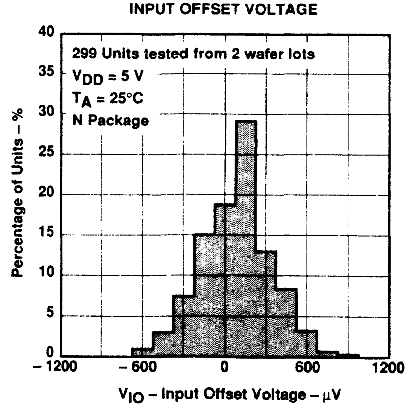


NC – No internal connection

description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE



T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	900 μV	TLC27L9CD	TLC27L9CN	TLC27L9CJ	—
	2 mV	TLC27L4BCD	TLC27L4BCN	TLC27L4BCJ	—
	5 mV	TLC27L4ACD	TLC27L4ACN	TLC27L4ACJ	—
	10 mV	TLC27L4CD	TLC27L4CN	TLC27L4CJ	—
– 40°C to 85°C	900 μV	TLC27L9ID	TLC27L9IN	TLC27L9IJ	—
	2 mV	TLC27L4BID	TLC27L4BIN	TLC27L4BIJ	—
	5 mV	TLC27L4AID	TLC27L4AIN	TLC27L4AIJ	—
	10 mV	TLC27L4ID	TLC27L4IN	TLC27L4IJ	—
– 55°C to 125°C	900 μV	—	—	TLC27L9MJ	TLC27L9MFK
	10 mV	—	—	TLC27L4MJ	TLC27L4MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27L9CDR).

description (continued)

These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications . Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single supply operation and ultra-low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

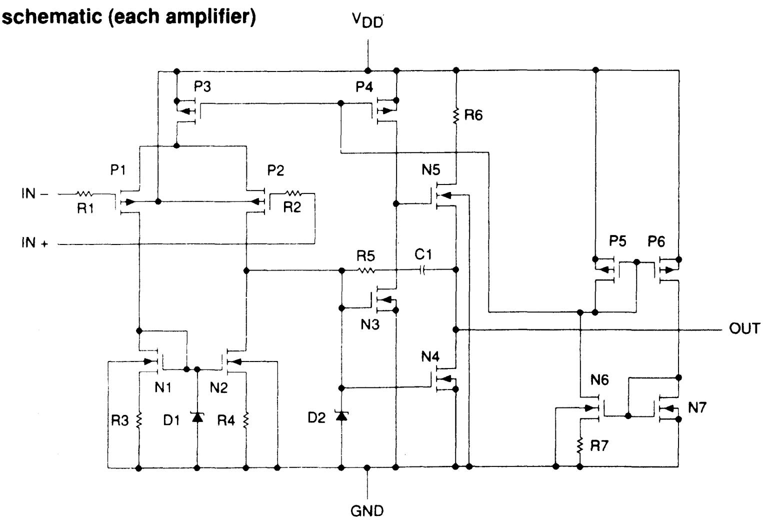
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC27L4 and TLC27L9 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... − 0.3 V to V_{DD}
Input current, I_I .... ± 5 mA
Output current, I_O (each output) .... ± 30 mA
Total current into V_{DD} terminal .... 45 mA
Total current out of ground terminal .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types .... 0°C to 70°C
I-suffix types .... − 40°C to 85°C
M-suffix types .... − 55°C to 125°C
Storage temperature range .... − 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package .... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I- suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
J (M- suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Input voltage, V_I	V_{DD} = 5 V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	V_{DD} = 10 V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	µV
				Full range			3000	
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	
				Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				70°C	3	4.2		
				0°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				70°C	50	380		
				0°C	50	700		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	95		
				0°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		
				0°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		39	68	µA
				70°C		31	56	
				0°C		48	84	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	μV
				Full range			3000	μV
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	μV
				Full range			1900	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				70°C	7.8	8.9		V
				0°C	7.8	8.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				70°C	50	660		V/mV
				0°C	50	1100		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				70°C	60	97		dB
				0°C	60	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				70°C	60	98		dB
				0°C	60	97		dB
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		57	92	μA
				70°C		44	80	μA
				0°C		72	132	μA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	µV
				Full range			3500	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				85°C	3	4.2		
				−40°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				85°C	50	330		
				−40°C	50	900		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	95		
				−40°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		
				−40°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		39	68	µA
				85°C		29	52	
				−40°C		62	108	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			7	
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	μV
				Full range			3500	
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				85°C	7.8	8.9		
				−40°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				85°C	50	585		
				−40°C	50	1550		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				85°C	60	98		
				−40°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				85°C	60	98		
				−40°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		57	92	μA
				85°C		40	72	
				−40°C		98	172	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				125°C	3	4.2		
				−55°C	3	4.1		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				125°C	25	200		
				−55°C	25	950		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	85		
				−55°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				−55°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		39	68	µA
				125°C		27	48	
				−55°C		69	120	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	− 0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				125°C	7.8	9		
				− 55°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				125°C	25	380		
				− 55°C	25	1750		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				125°C	60	91		
				− 55°C	60	97		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				125°C	60	98		
				− 55°C	60	97		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		57	92	µA
				125°C		35	60	
				− 55°C		111	192	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				70°C		0.03		
				0°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				70°C		0.02		
				0°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				70°C		4.5		
				0°C		6		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				70°C		65		
				0°C		100		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				70°C		30°		
				0°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				70°C		0.04		
				0°C		0.05		
			V_{IPP} = 5.5 V	25°C		0.04		
				70°C		0.04		
				0°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				70°C		0.9		
				0°C		1.3		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				70°C		90		
				0°C		125		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				70°C		34°		
				0°C		40°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
				− 40°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
				− 40°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				85°C		4		
				− 40°C		7		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				85°C		55		
				− 40°C		130		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				85°C		28°		
				− 40°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				85°C		0.03		
				− 40°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				85°C		0.03		
				− 40°C		0.05		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				85°C		0.8		
				− 40°C		1.4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				85°C		80		
				− 40°C		155		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				85°C		32°		
				− 40°C		42°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/µs
				125°C		0.02		
				– 55°C		0.04		
			V_{IPP} = 2.5 V	25°C		0.03		
				125°C		0.02		
				– 55°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		5		kHz
				125°C		3		
				– 55°C		8		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		85		kHz
				125°C		45		
				– 55°C		140		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		34°		
				125°C		25°		
				– 55°C		39°		

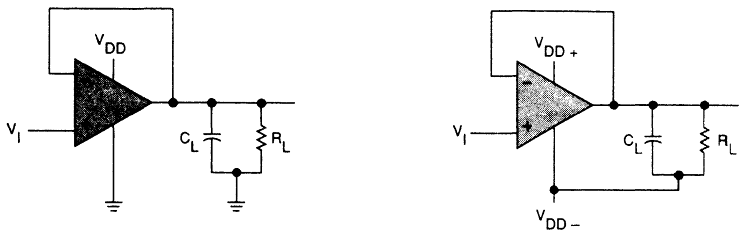
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/µs
				125°C		0.03		
				– 55°C		0.06		
			V_{IPP} = 5.5 V	25°C		0.04		
				125°C		0.03		
				– 55°C		0.06		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 1		25°C		1		kHz
				125°C		0.7		
				– 55°C		1.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		110		kHz
				125°C		70		
				– 55°C		165		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		38°		
				125°C		29°		
				– 55°C		43°		

PARAMETER MEASUREMENT INFORMATION

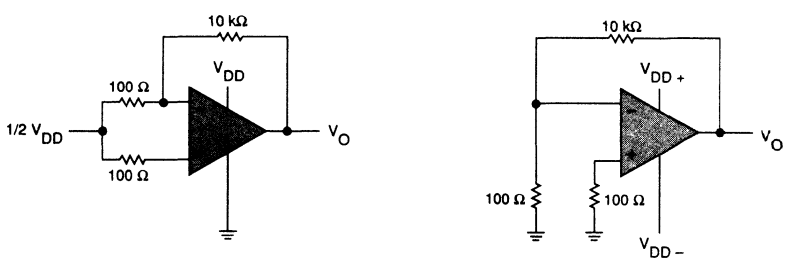
single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

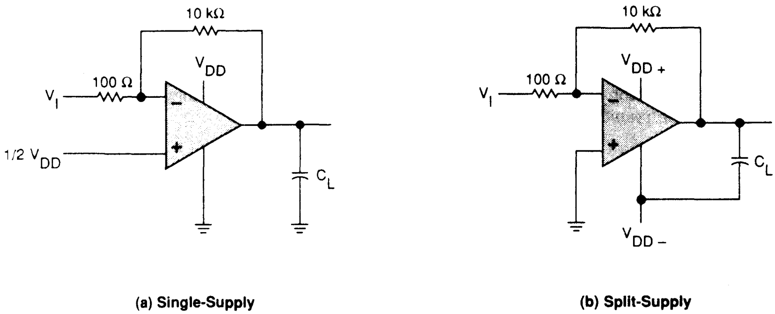


FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 op amps, attempts to measure the input bias current can result in erroneous readings. The typical bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

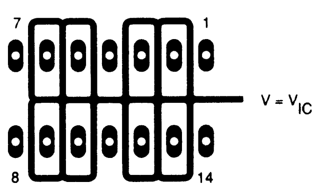


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (N AND J DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

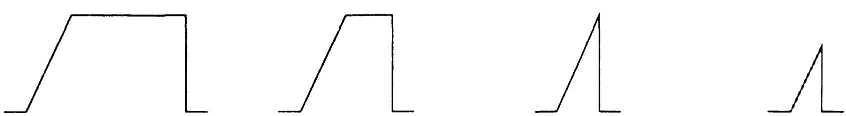
input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

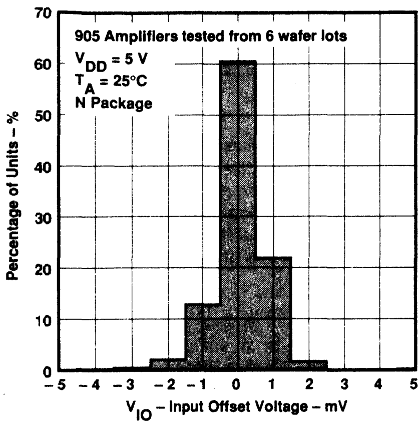


FIGURE 6

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

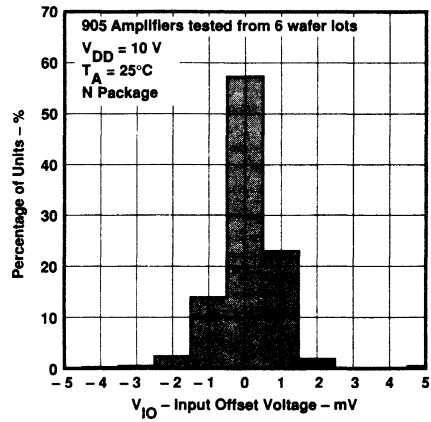


FIGURE 7

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

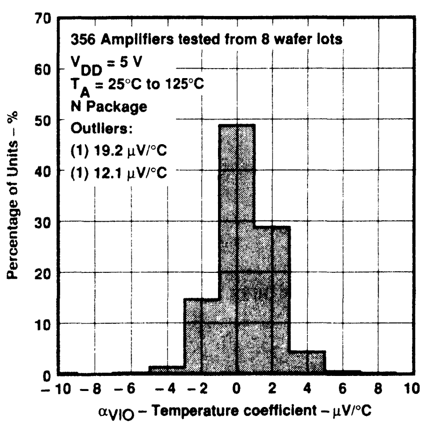


FIGURE 8

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

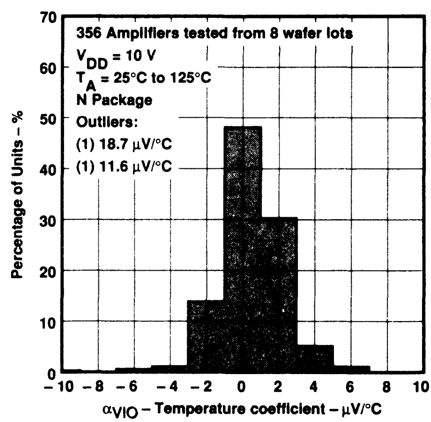


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

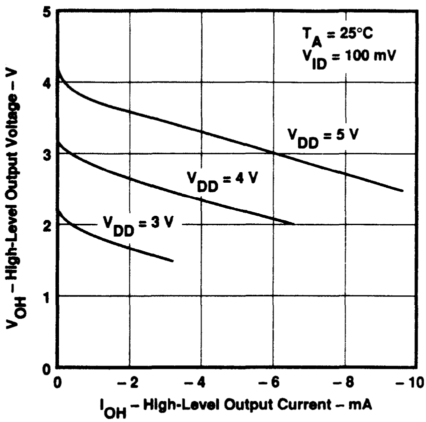


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

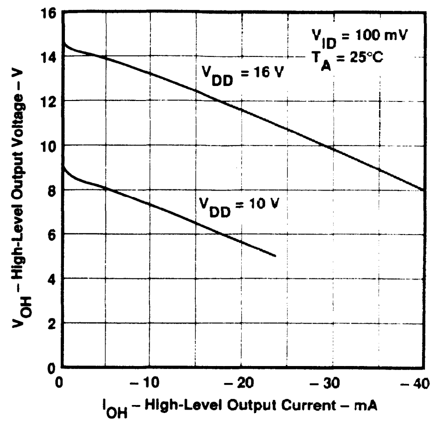


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

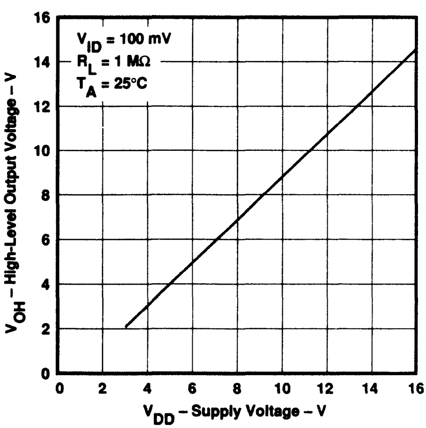


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

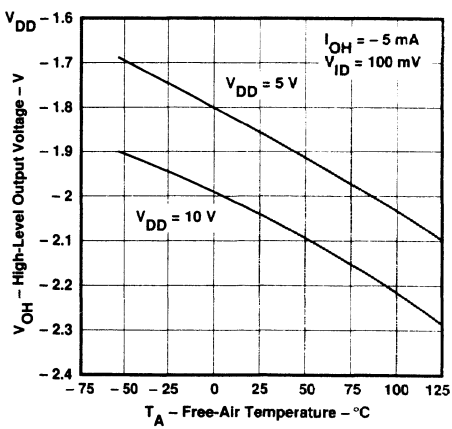


FIGURE 13

Operational Amplifiers 3

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

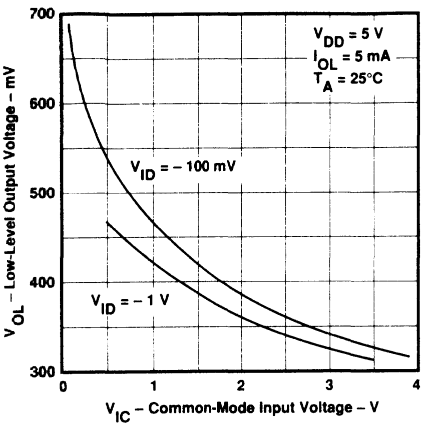


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

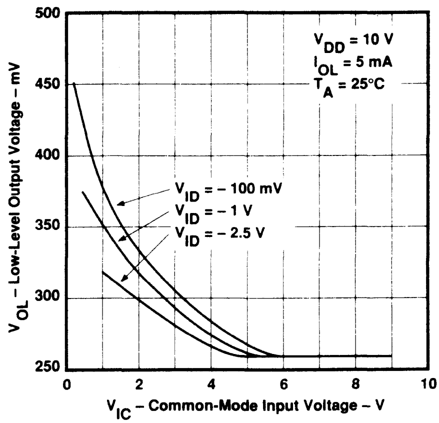


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

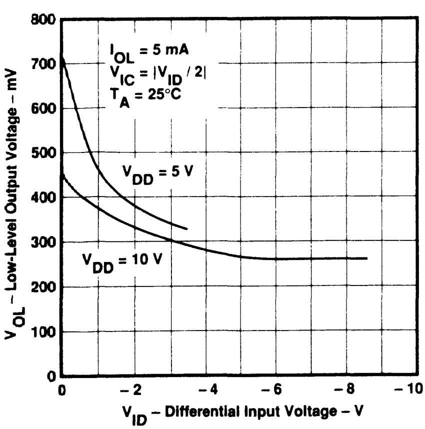


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

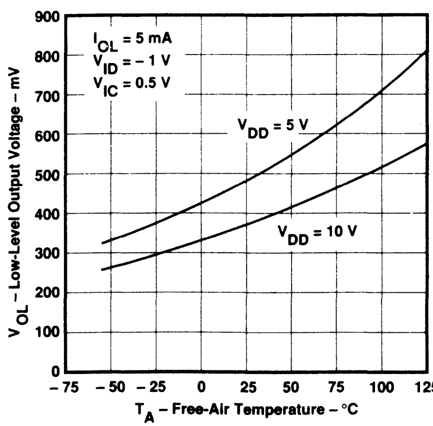


FIGURE 17

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

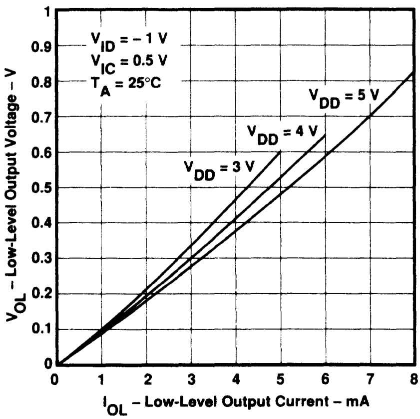


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

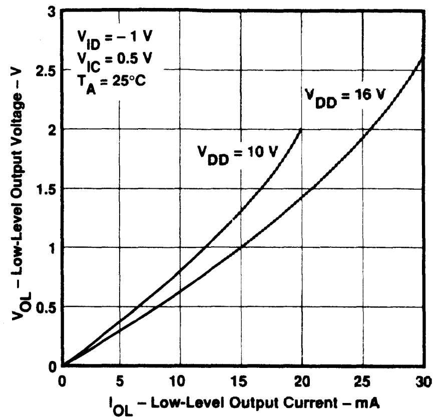


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

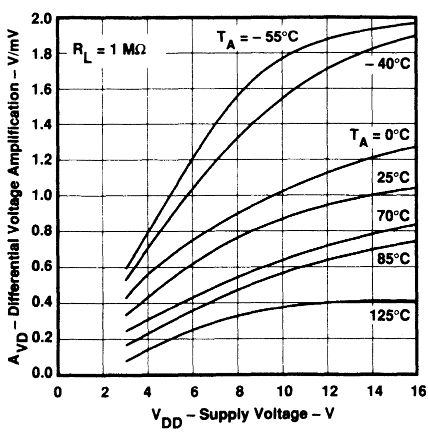


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

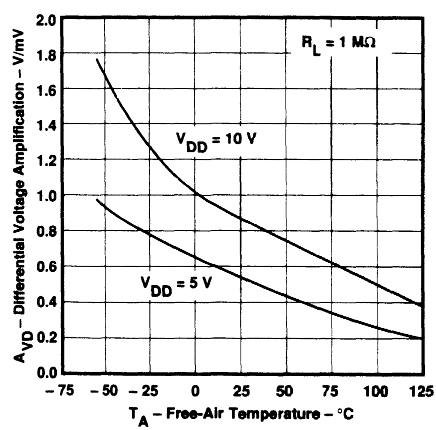


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

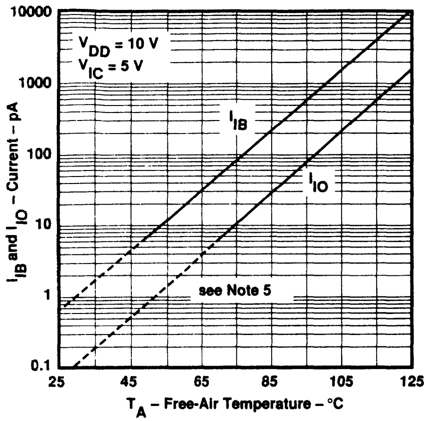


FIGURE 22

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

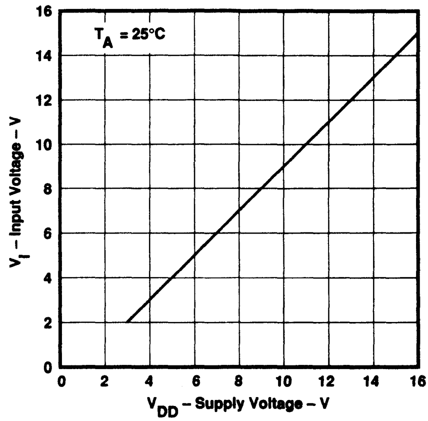


FIGURE 23

SUPPLY CURRENT vs SUPPLY VOLTAGE

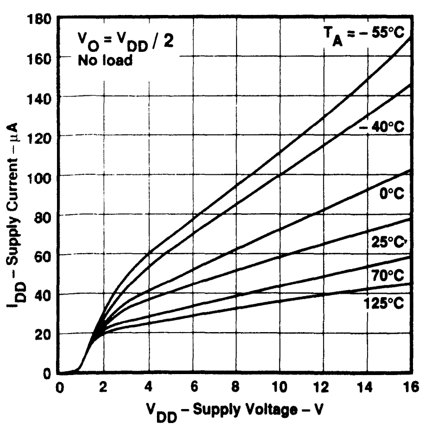


FIGURE 24

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

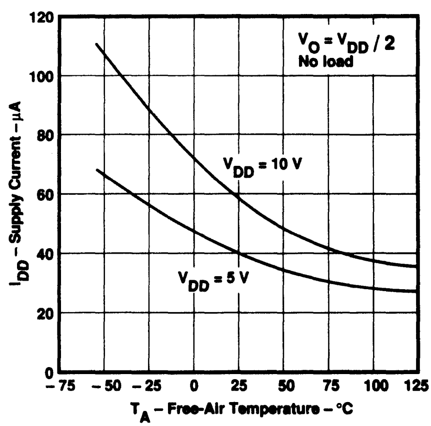


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TEXAS INSTRUMENTS

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

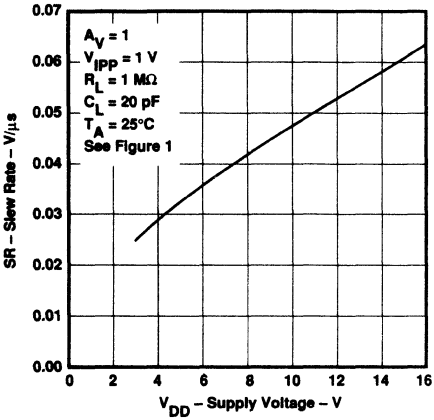


FIGURE 26

SLEW RATE vs FREE-AIR TEMPERATURE

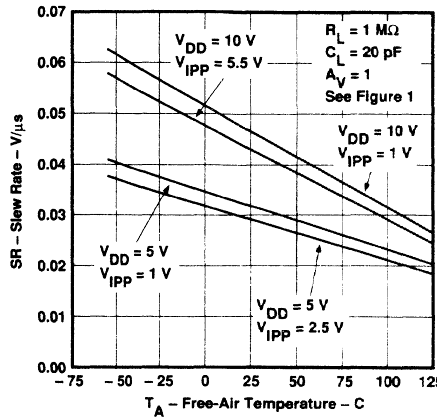


FIGURE 27

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

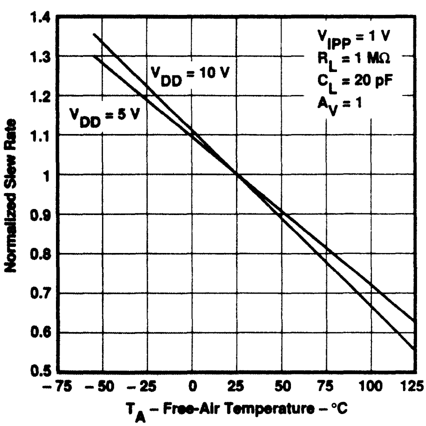


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

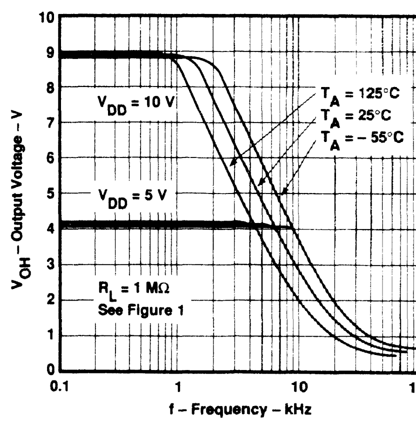


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

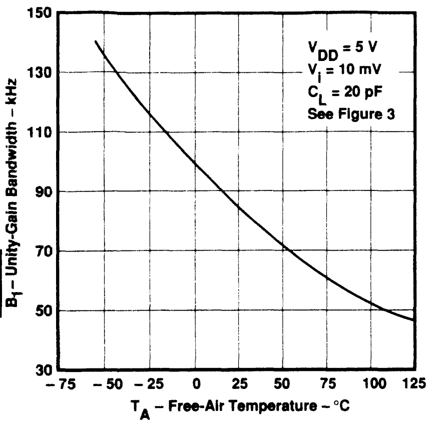


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

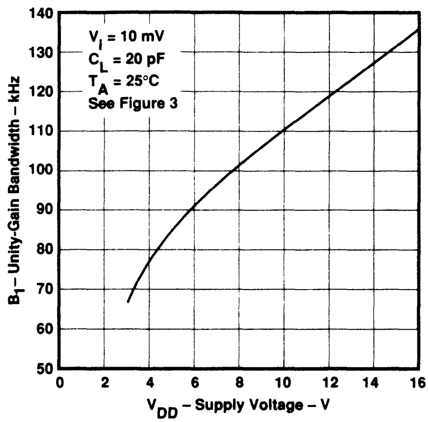


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

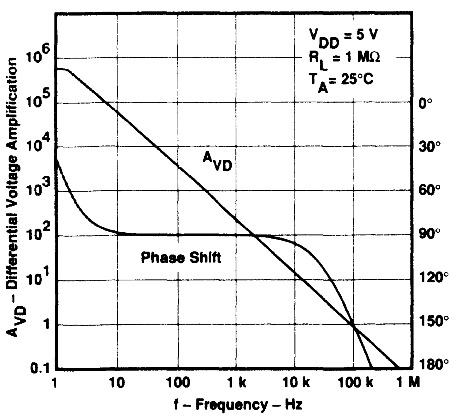


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

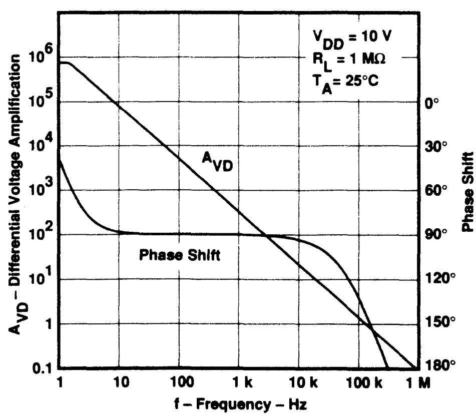


FIGURE 33

TYPICAL CHARACTERISTICS

**PHASE MARGIN
vs
SUPPLY VOLTAGE**

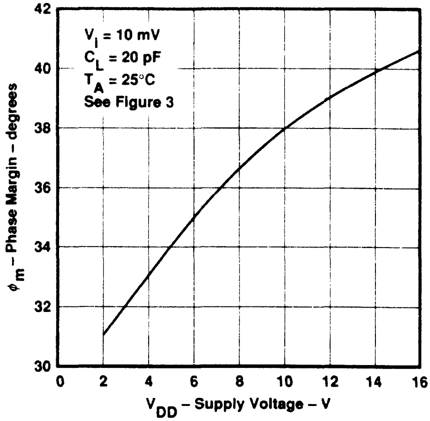


FIGURE 34

**PHASE MARGIN
vs
FREE-AIR TEMPERATURE**

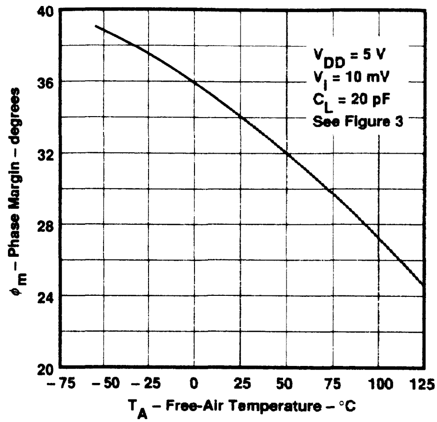


FIGURE 35

**PHASE MARGIN
vs
CAPACITIVE LOAD**

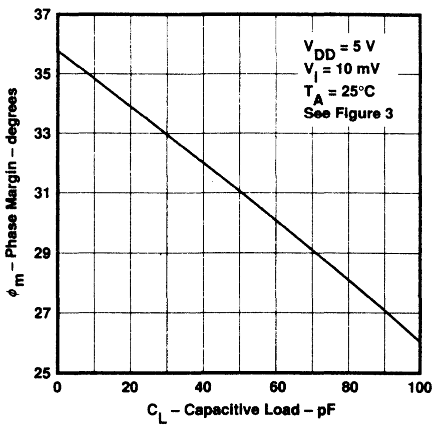


FIGURE 36

**EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY**

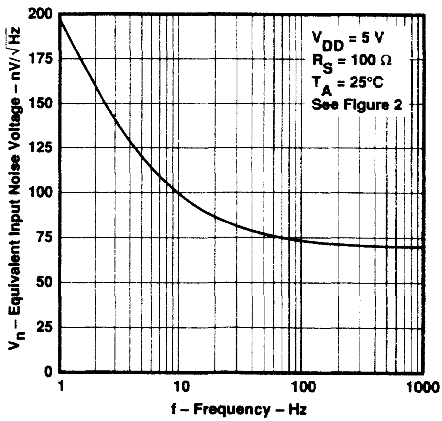


FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27L4 and TLC27L9 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

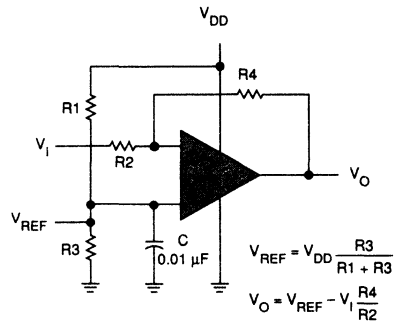
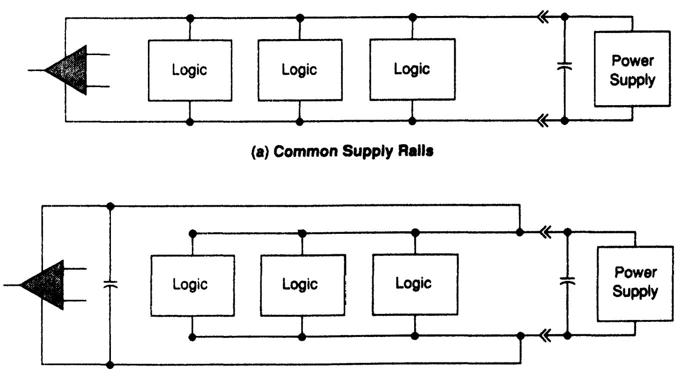


FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails

(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} − 1 V at T_A = 25°C and at V_{DD} − 1.5 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

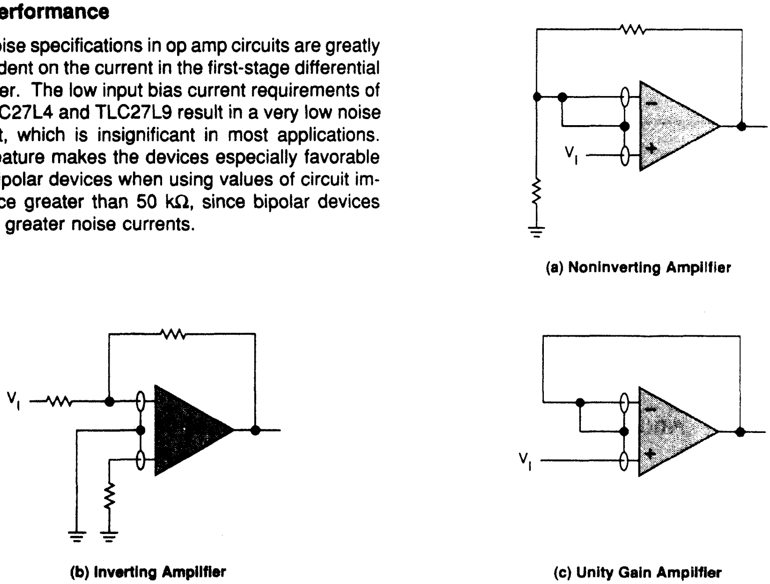


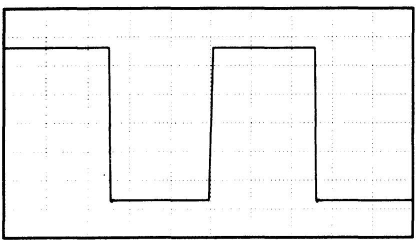
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

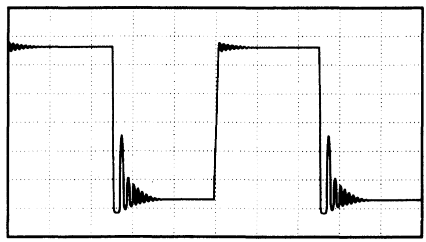
output characteristics

The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

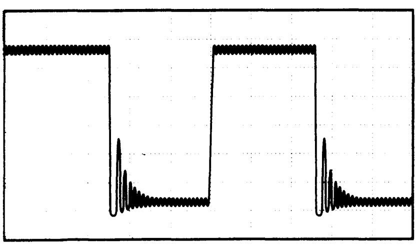
All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



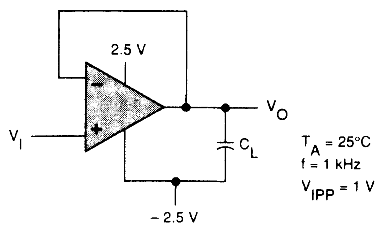
(a) C_L = 20 pF, R_L = no load



(b) C_L = 260 pF, R_L = no load



(c) C_L = 310 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R6 acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

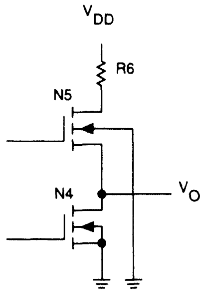


FIGURE 42. TLC27L4 / TLC27L9 OUTPUT STAGE

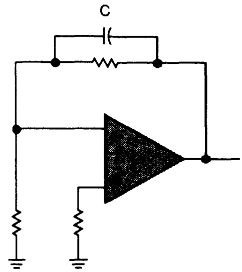


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages at or below 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occuring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA

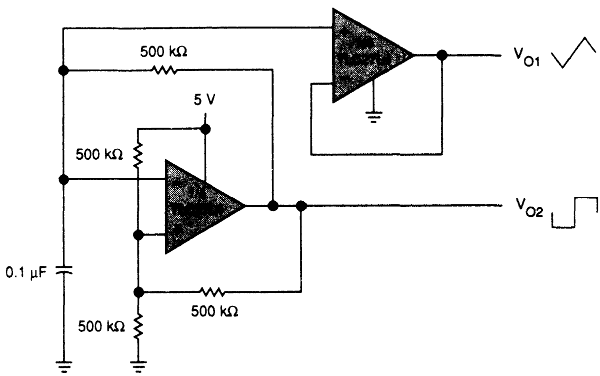
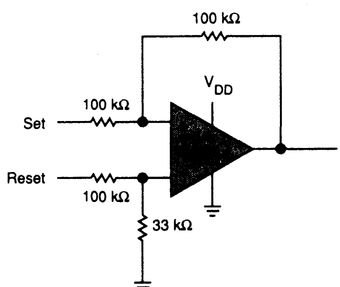


FIGURE 44. MULTIVIBRATOR

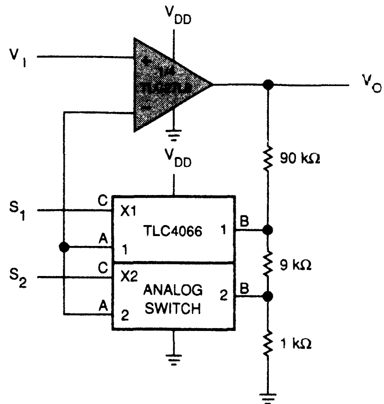


NOTES: V_{DD} = 5 V to 16V

FIGURE 45. SET / RESET FLIP-FLOP

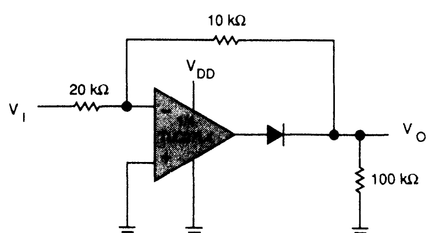
TYPICAL APPLICATION DATA

Select:	S_1	S_2
A_V	10	100



NOTES: V_{DD} = 5 V to 12V

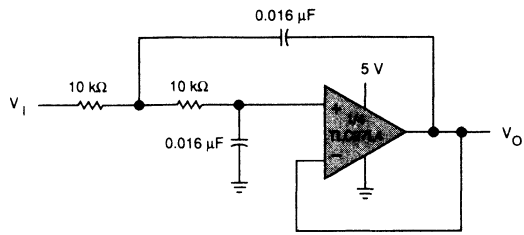
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTES: V_{DD} = 5 V to 16V

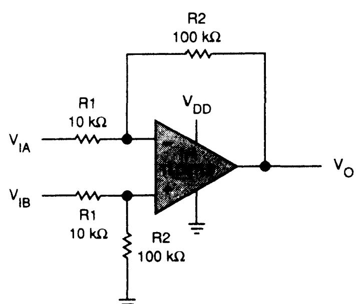
FIGURE 47. FULL WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

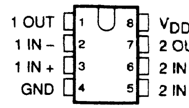
$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$

FIGURE 49. DIFFERENCE AMPLIFIER

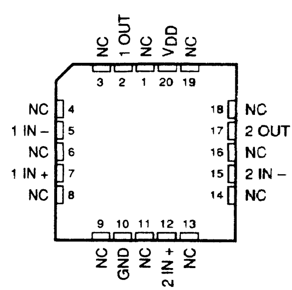
OCTOBER 1987

- **Trimmed Offset Voltage:**
  TLC27M7 . . . 500 µV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically**
  0.1 µV / Month, Including the First 30 Days
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  – 55°C to125°C . . . 4 V to 16 V
  – 40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise . . . 32 nV/√Hz Typically at f = 1 kHz**
- **Low Power . . . 2.1 mW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-In Latchup Immunity**

JG AND P DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

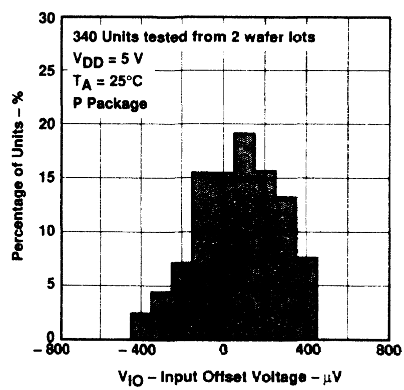
description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds

T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (P)	Ceramic DIP (JG)	Chip Carrier (FK)
0°C to 70°C	500 µV	TLC27M7CD	TLC27M7CP	TLC27M7CJG	——
	2 mV	TLC27M2BCD	TLC27M2BCP	TLC27M2BCJG	——
	5 mV	TLC27M2ACD	TLC27M2ACP	TLC27M2ACJG	——
	10 mV	TLC27M2CD	TLC27M2CP	TLC27M2CJG	——
– 40°C to 85°C	500 µV	TLC27M7ID	TLC27M7IP	TLC27M7IJG	——
	2 mV	TLC27M2BID	TLC27M2BIP	TLC27M2BIJG	——
	5 mV	TLC27M2AID	TLC27M2AIP	TLC27M2AIJG	——
	10 mV	TLC27M2ID	TLC27M2IP	TLC27M2IJG	——
– 55°C to 125°C	500 µV	——	——	TLC27M7MJG	TLC27M7MFK
	10 mV	——	——	TLC27M2MJG	TLC27M2MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27M7CDR).

DISTRIBUTION OF TLC27M7
INPUT OFFSET VOLTAGE



TEXAS INSTRUMENTS

description (continued)

comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are avaliable on LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single supply operation and low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

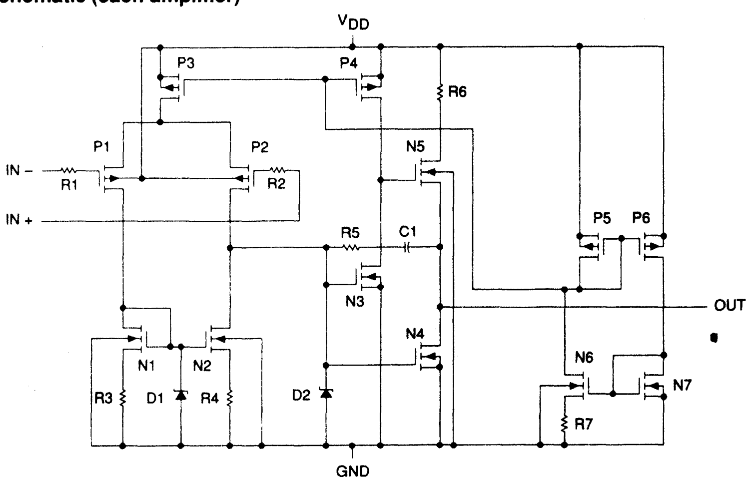
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC27M2 and TLC27M7 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... − 0.3 V to V_{DD}
Input current, I_I .... ± 5 mA
Output current, I_O (each output) .... ± 30 mA
Total current into V_{DD} terminal .... 45 mA
Total current out of ground terminal .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types .... 0°C to 70°C
I-suffix types .... − 40°C to 85°C
M-suffix types .... − 55°C to 125°C
Storage temperature range .... − 65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package .... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I- suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M- suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	− 0.2		3.5	− 0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	− 0.2		8.5	− 0.2		8.5	V
Operating free-air temperature, T_A		− 55		125	− 40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	2000	µV
				Full range			3000	µV
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	µV
				Full range			1500	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				70°C	3	4		V
				0°C	3	3.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				70°C	15	140		V/mV
				0°C	15	200		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				70°C	60	92		dB
				0°C	60	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		dB
				0°C	60	92		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		210	560	µA
				70°C		170	440	µA
				0°C		250	640	µA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27M2AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27M2BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		224	2000	µV
				Full range			3000	µV
		TLC27M7C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	µV
				Full range			1900	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				70°C	7.8	8.7		V
				0°C	7.8	8.7		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				70°C	15	230		V/mV
				0°C	15	320		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	94		dB
				0°C	60	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		dB
				0°C	60	92		dB
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		285	600	µA
				70°C		220	560	µA
				0°C		345	800	µA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	2000	µV
				Full range			3500	
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	
				Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				85°C	3	4		
				−40°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				85°C	15	130		
				−40°C	15	270		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				85°C	60	90		
				−40°C	60	90		
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		
				−40°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		210	560	µA
				85°C		160	400	
				−40°C		315	800	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M2AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M2BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		224	2000	µV
				Full range			3500	
		TLC27M7I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	− 0.2 to 9	− 0.3 to 9.2		V
				Full range	− 0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				85°C	7.8	8.7		
				− 40°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				− 40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				85°C	15	220		
				− 40°C	15	390		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	94		
				− 40°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		
				− 40°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		285	600	µA
				85°C		205	520	
				− 40°C		450	900	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		185	500	μV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 4	− 0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				125°C	3	4		
				− 55°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				125°C	15	120		
				− 55°C	15	290		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				125°C	60	91		
				− 55°C	60	89		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				− 55°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		210	560	μA
				125°C		140	360	
				− 55°C		340	880	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M7M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		190	800	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				125°C	7.8	8.8		
				−55°C	7.8	8.6		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				125°C	15	190		
				−55°C	15	420		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	93		
				−55°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				−55°C	60	91		
I_{DD}	Supply current (two amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		285	600	µA
				125°C		180	480	
				−55°C		490	1000	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				70°C		0.36		
				0°C		0.46		
			V_{IPP} = 2.5 V	25°C		0.40		
				70°C		0.34		
				0°C		0.43		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				70°C		50		
				0°C		60		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				70°C		400		
				0°C		600		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				70°C		39°		
				0°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				70°C		0.51		
				0°C		0.67		
			V_{IPP} = 5.5 V	25°C		0.56		
				70°C		0.46		
				0°C		0.61		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				70°C		30		
				0°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				70°C		510		
				0°C		710		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				70°C		42°		
				0°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				85°C		0.35		
				− 40°C		0.51		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
				− 40°C		0.48		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				85°C		45		
				− 40°C		75		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				85°C		370		
				− 40°C		770		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				85°C		38°		
				− 40°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				85°C		0.47		
				− 40°C		0.77		
			V_{IPP} = 5.5 V	25°C		0.56		
				85°C		0.44		
				− 40°C		0.70		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				85°C		25		
				− 40°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				85°C		480		
				− 40°C		880		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				85°C		41°		
				− 40°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				125°C		0.29		
				−55°C		0.54		
			V_{IPP} = 2.5 V	25°C		0.40		
				125°C		0.28		
				−55°C		0.50		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				125°C		40		
				−55°C		80		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				125°C		330		
				−55°C		850		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				125°C		36°		
				−55°C		44°		

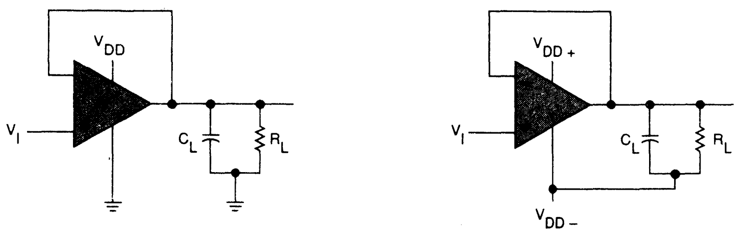
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS			M-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				125°C		0.38		
				−55°C		0.81		
			V_{IPP} = 5.5 V	25°C		0.56		
				125°C		0.35		
				−55°C		0.73		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				125°C		20		
				−55°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				125°C		440		
				−55°C		960		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				125°C		39°		
				−55°C		47°		

PARAMETER MEASUREMENT INFORMATION

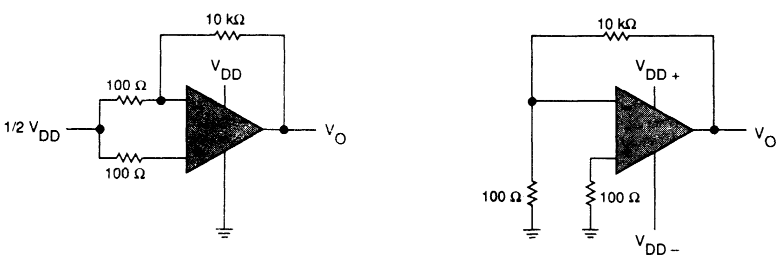
single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

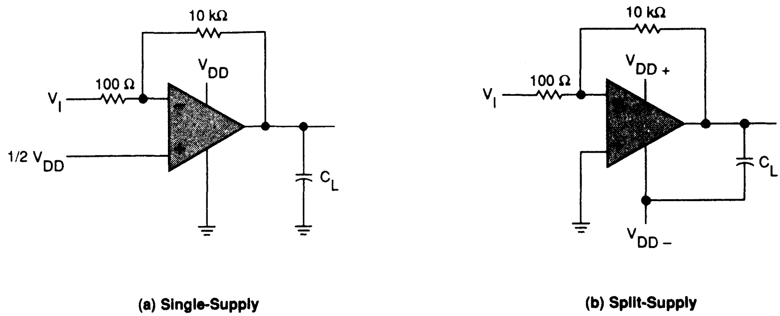


FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

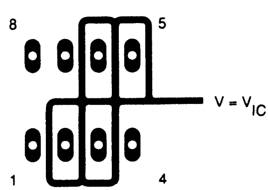


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

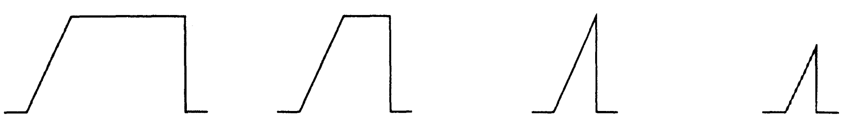
input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 1 kHz (b) B_{OM} > f > 1 kHz (c) f = B_{OM} (d) f > B_{OM}

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

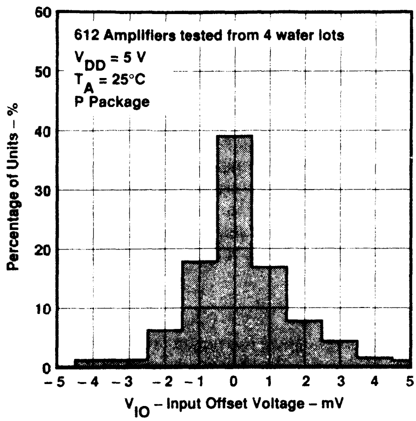


FIGURE 6

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

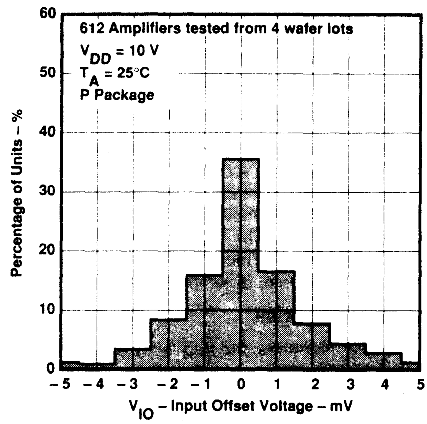


FIGURE 7

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

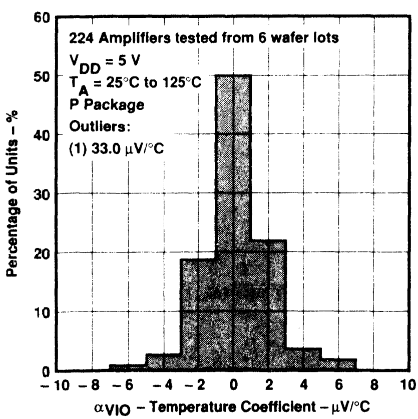


FIGURE 8

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

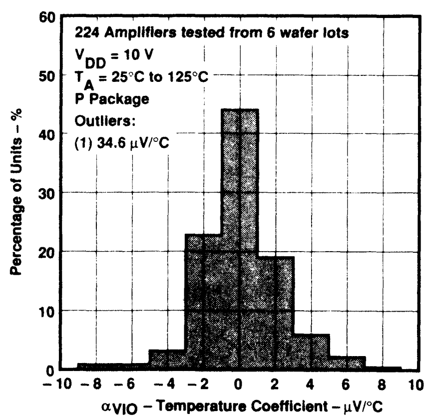


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

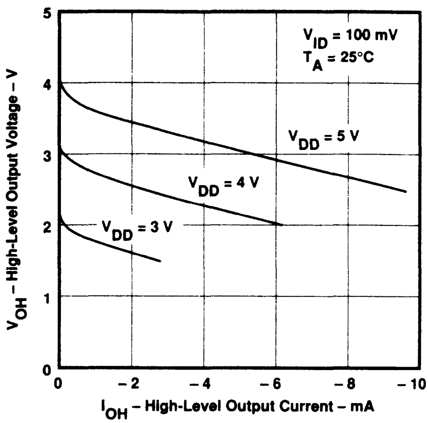


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

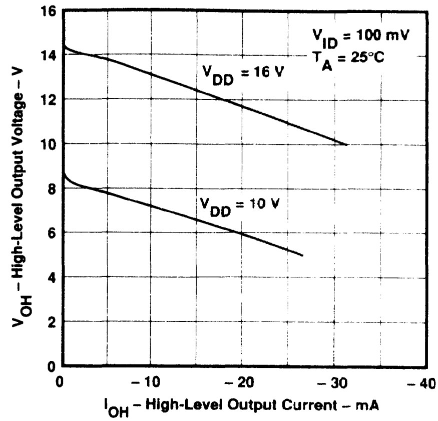


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

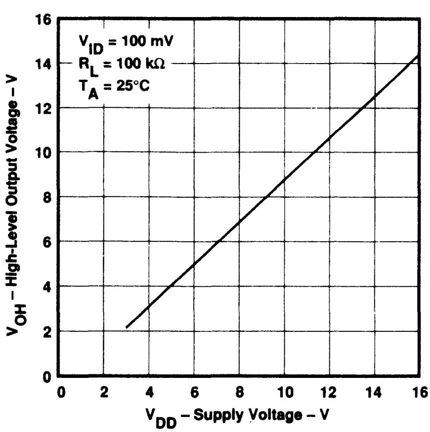


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

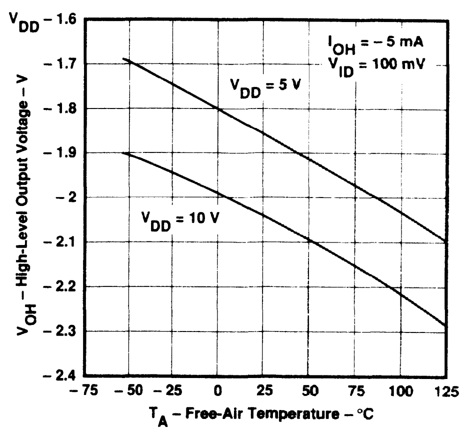


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

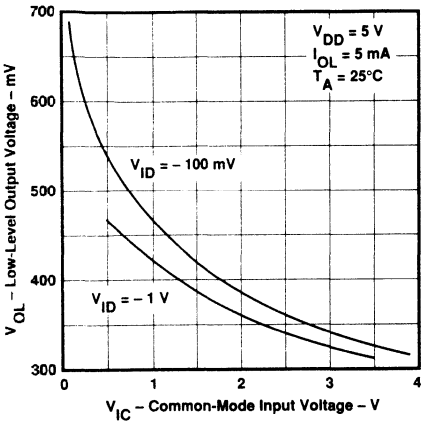


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

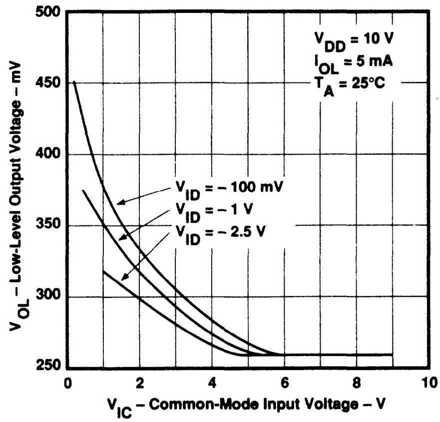


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

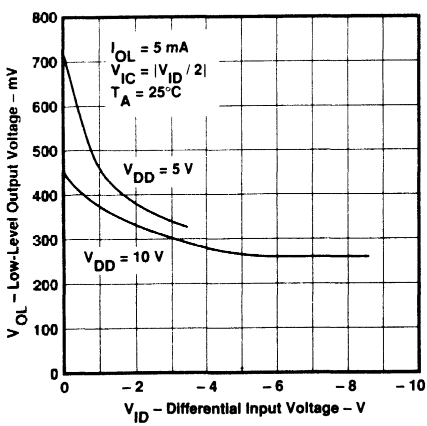


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

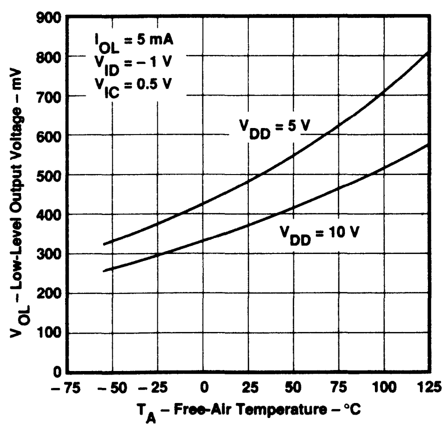


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

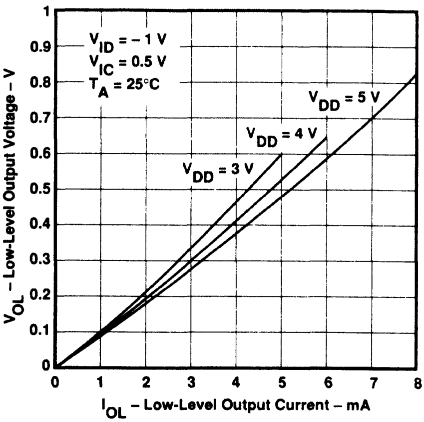


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

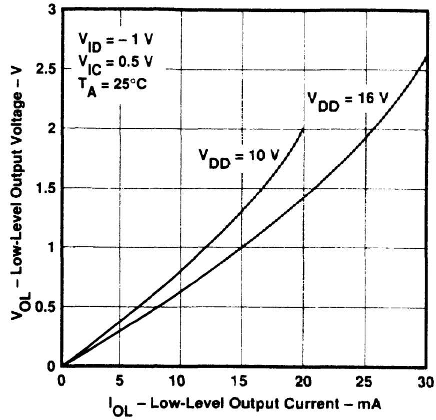


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

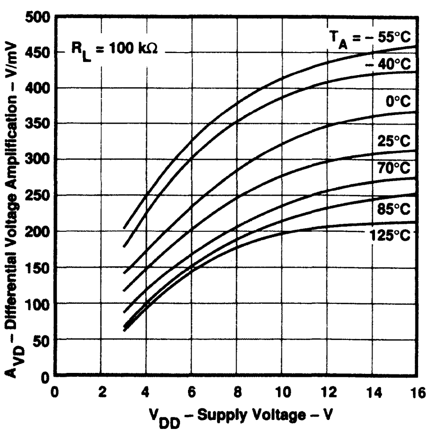


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

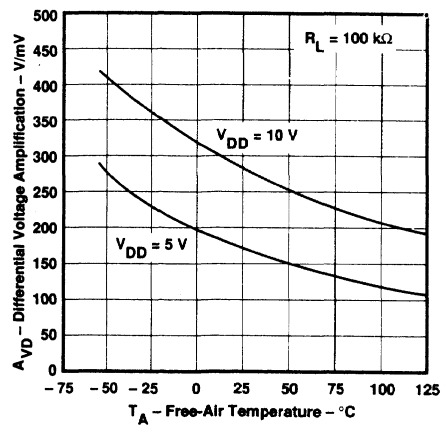


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

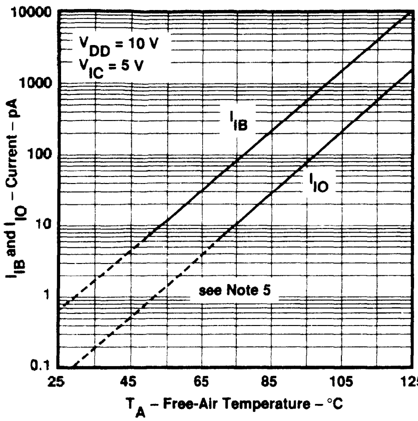


FIGURE 22

MAXIMUM INPUT VOLTAGE
vs
SUPPLY VOLTAGE

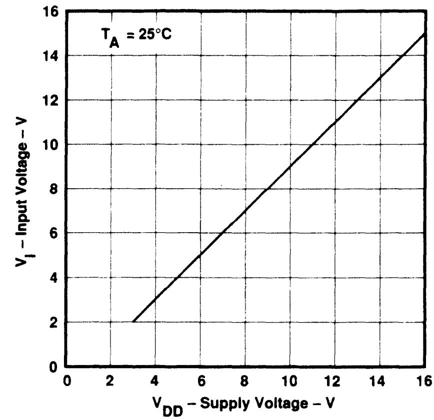


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

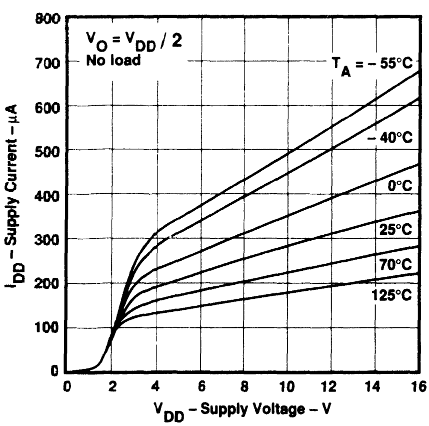


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

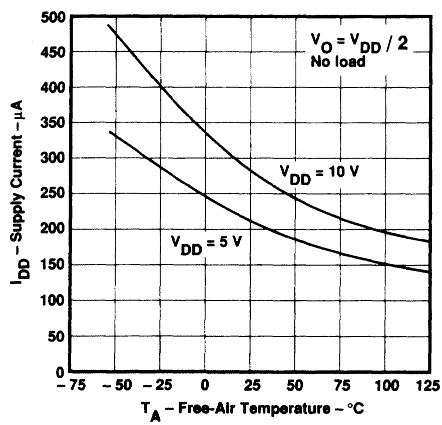


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

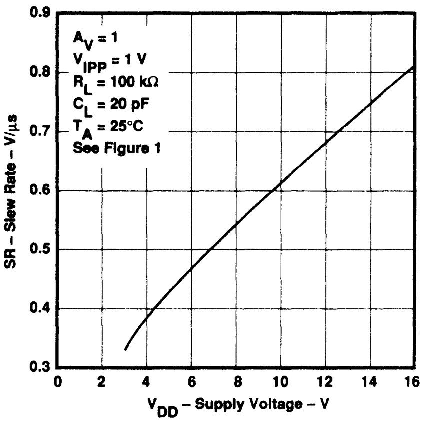


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

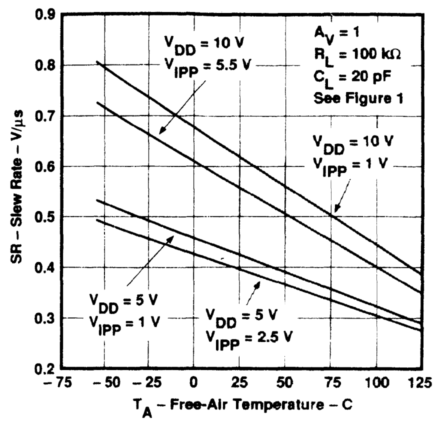


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

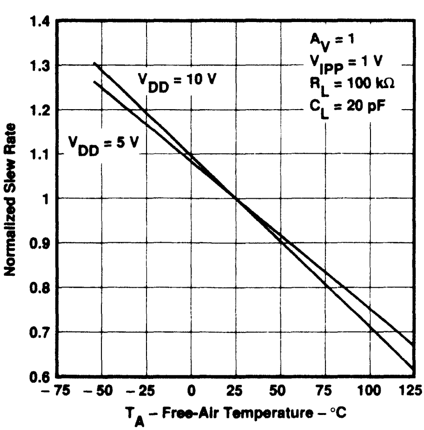


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

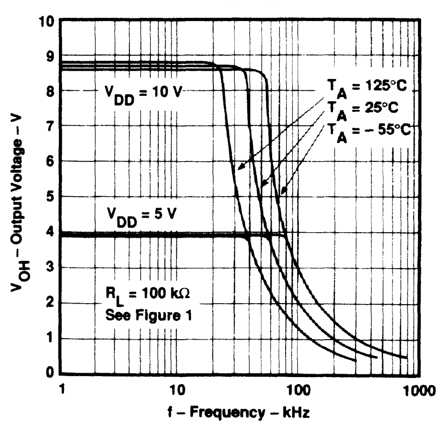


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

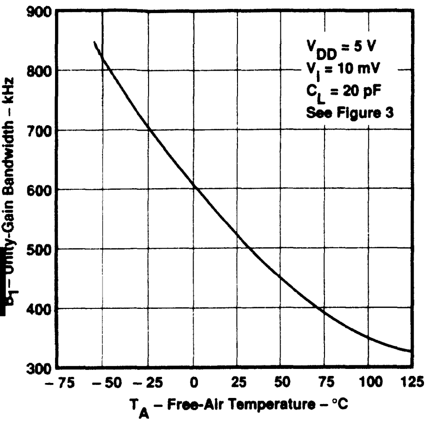


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

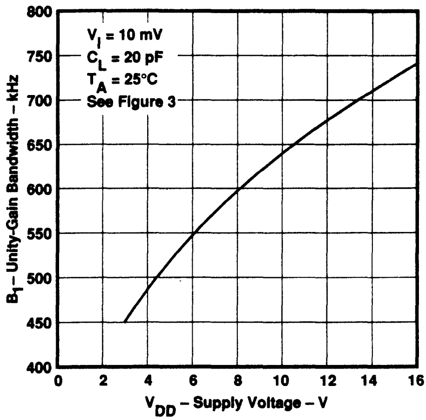


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

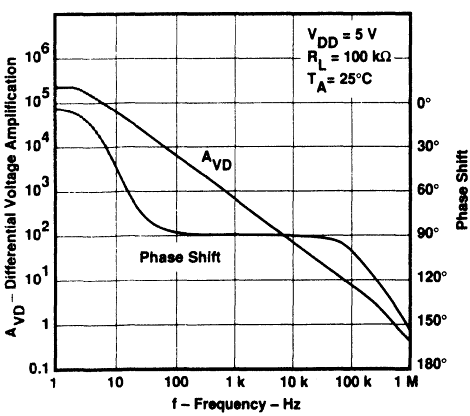


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

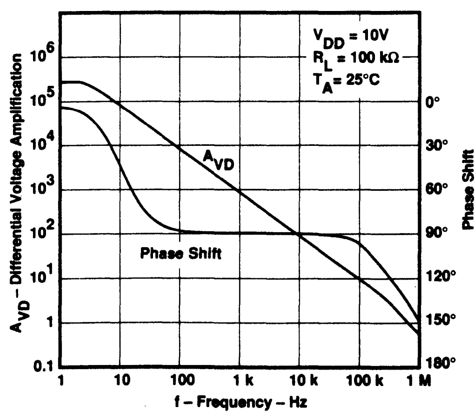


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

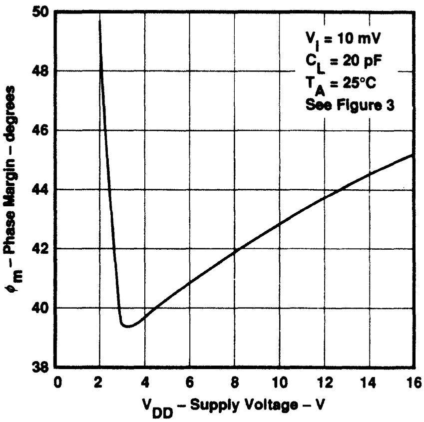


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

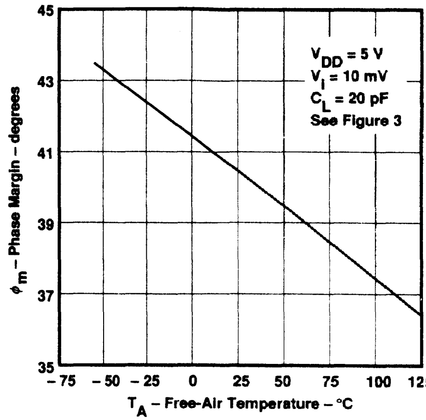


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

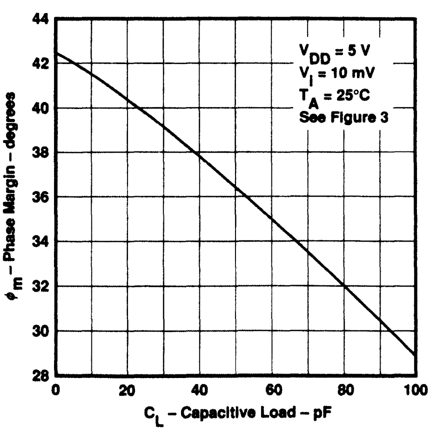


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

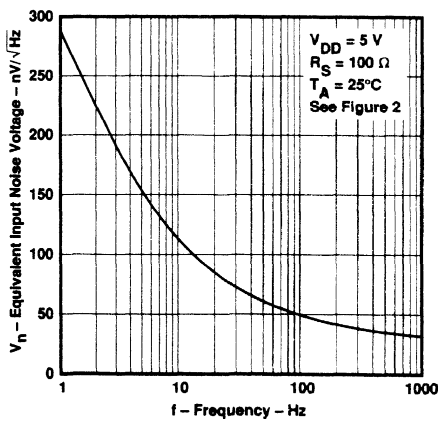


FIGURE 37

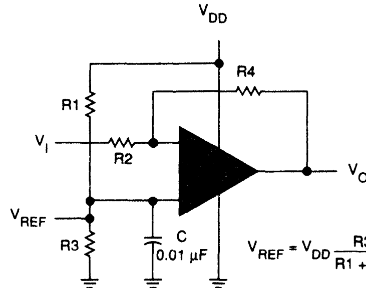
3
Operational Amplifiers

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27M2 and TLC27M7 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.



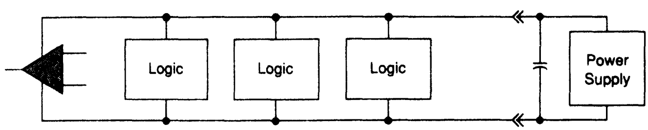
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I) \frac{R4}{R2} + V_{REF}$$

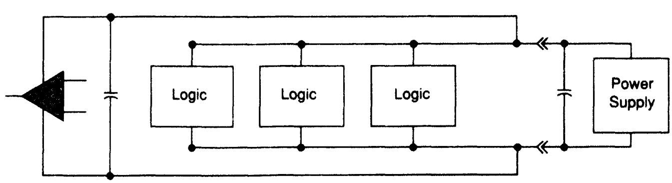
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

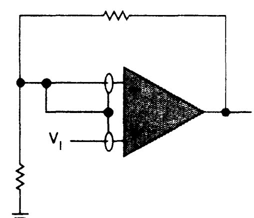
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

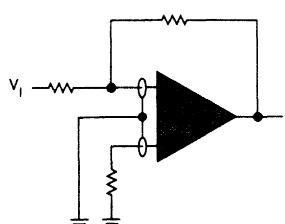
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

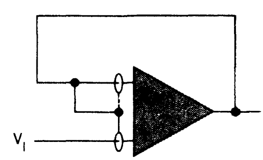
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

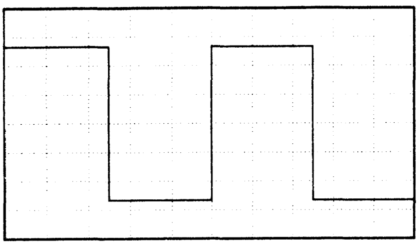
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

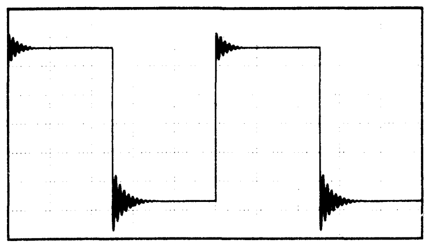
output characteristics

The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

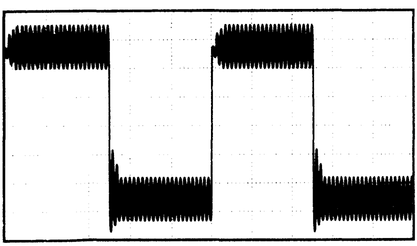
All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



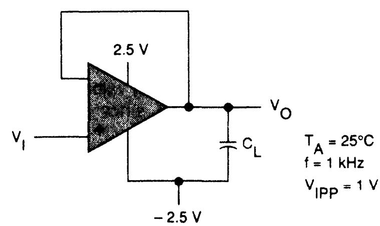
(a) C_L = 20 pF, R_L = no load



(b) C_L = 170 pF, R_L = no load



(c) C_L = 190 pF, R_L = no load



(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pull-up resistor (R_P) connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pull-up resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

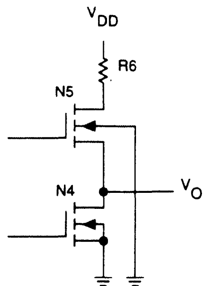


FIGURE 42. TLC27M2 / TLC27M7 OUTPUT STAGE

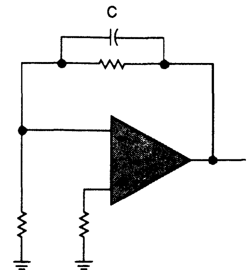


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

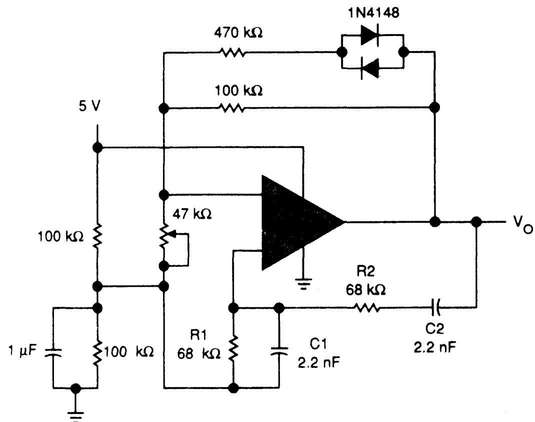
The TLC27M2 and TLC27M7 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

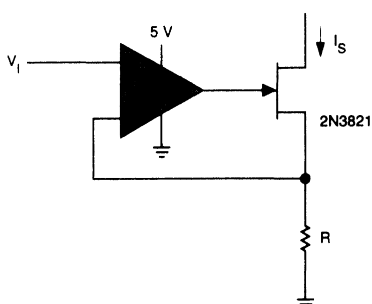
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 44. WIEN OSCILLATOR



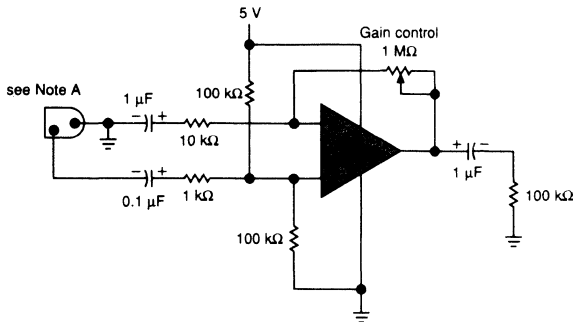
NOTES: $V_I = 0$ V TO 3 V

$$I_S = \frac{V_I}{R}$$

FIGURE 45. PRECISION LOW CURRENT SINK

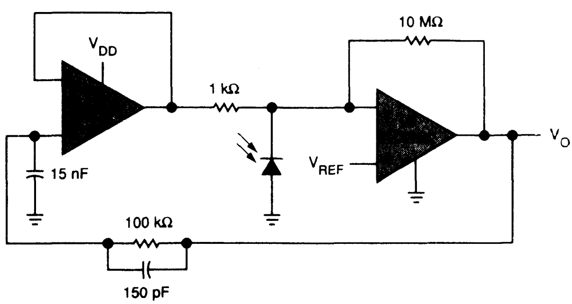
TEXAS INSTRUMENTS

TYPICAL APPLICATION DATA



NOTE A: Low to medium impedance dynamic mike

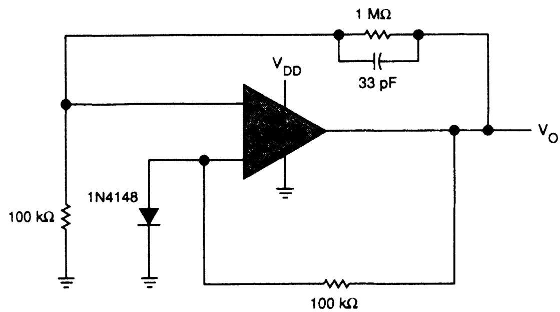
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5 V LOW POWER VOLTAGE REGULATOR

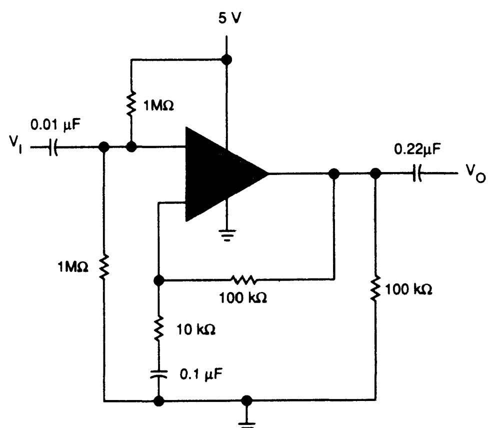
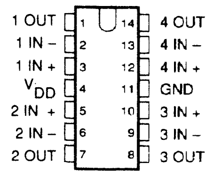


FIGURE 49. SINGLE RAIL A.C. AMPLIFIER

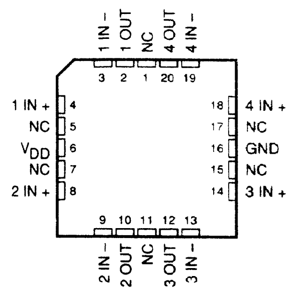
OCTOBER 1987

- **Trimmed Offset Voltage:** **TLC27M9 . . . 900 μV Max at 25°C, V_{DD} = 5 V**
- **Input Offset Voltage Drift Typically 0.1 μV / Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **−55°C to125°C . . . 4 V to 16 V**
  - **−40°C to 85°C . . . 4 V to 16 V**
  - **0°C to 70°C . . . 3 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C- suffix, I- suffix types)**
- **Low Noise . . . 32 nV/√Hz Typically at f = 1 kHz**
- **Low Power . . . 2.1 mW Typically at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape-and-Reel**
- **Designed-in Latchup Immunity**

N AND J DUAL-IN-LINE PACKAGE
D SMALL-OUTLINE PACKAGE
(TOP VIEW)



FK CHIP CARRIER PACKAGE
(TOP VIEW)

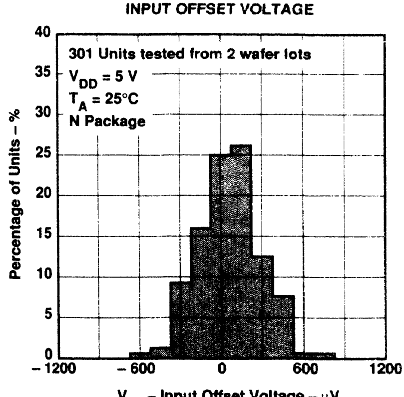


NC – No internal connection

description

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds

DISTRIBUTION OF TLC27M9
INPUT OFFSET VOLTAGE



T_A	V_{IO}max at 25°C	PACKAGE			
		Small-Outline (D) See Note 1	Plastic DIP (N)	Ceramic DIP (J)	Chip Carrier (FK)
0°C to 70°C	900 μV	TLC27M9CD	TLC27M9CN	TLC27M9CJ	—
	2 mV	TLC27M4BCD	TLC27M4BCN	TLC27M4BCJ	—
	5 mV	TLC27M4ACD	TLC27M4ACN	TLC27M4ACJ	—
	10 mV	TLC27M4CD	TLC27M4CN	TLC27M4CJ	—
−40°C to 85°C	900 μV	TLC27M9ID	TLC27M9IN	TLC27M9IJ	—
	2 mV	TLC27M4BID	TLC27M4BIN	TLC27M4BIJ	—
	5 mV	TLC27M4AID	TLC27M4AIN	TLC27M4AIJ	—
	10 mV	TLC27M4ID	TLC27M4IN	TLC27M4IJ	—
−55°C to 125°C	900 μV	—	—	TLC27M9MJ	TLC27M9MFK
	10 mV	—	—	TLC27M4MJ	TLC27M4MFK

NOTE 1: Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLC27M9CDR).

TEXAS INSTRUMENTS

description (continued)

comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C- suffix and I- suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are avaliable on LinCMOS operational amplifiers, without the power penalities of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single supply operation and low power consumption making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

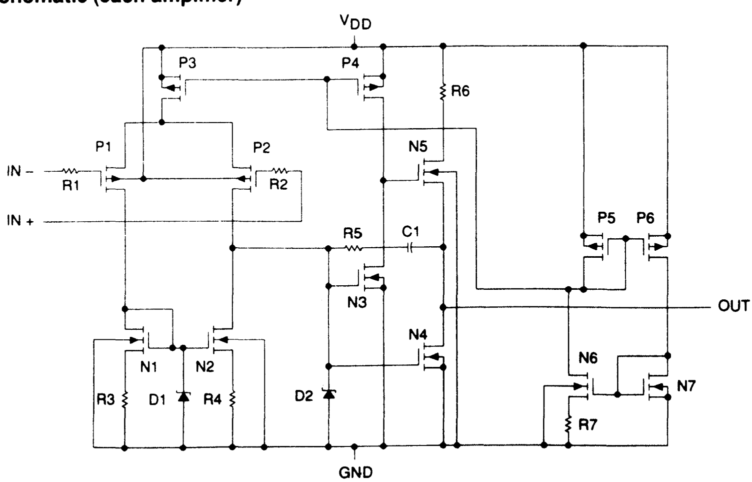
A wide range of packaging options is available, including small outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand – 100-mA surge currents without sustaining latchup.

The TLC27M4 and TLC27M9 incorporate internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M- suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C, the I- suffix devices from – 40°C to 85°C, and the C- suffix devices from 0°C to 70°C.

equivalent schematic (each amplifier)



3 Operational Amplifiers

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) .... 18 V
Differential input voltage (see Note 3) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... -0.3 V to V_{DD}
Input current, I_I .... ±5 mA
Output current, I_O (each output) .... ±30 mA
Total current into V_{DD} terminal .... 45 mA
Total current out of ground terminal .... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix types .... 0°C to 70°C
I-suffix types .... −40°C to 85°C
M-suffix types .... −55°C to 125°C
Storage temperature range .... −65°C to 150°C
Case temperature for 60 seconds: FK package .... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package .... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I- suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
J (M- suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M- SUFFIX TYPES			I- SUFFIX TYPES			C- SUFFIX TYPES			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Input voltage, V_I	$V_{DD} = 5$ V	0		3.5	−0.2		3.5	−0.2		3.5	V
	$V_{DD} = 10$ V	0		8.5	−0.2		8.5	−0.2		8.5	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	mV
		TLC27M4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	mV
				Full range			6.5	mV
		TLC27M4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		250	2000	µV
				Full range			3000	µV
		TLC27M9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	µV
				Full range			1500	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				70°C		7	300	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				70°C	3	4		V
				0°C	3	3.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	mV
				0°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				70°C	15	140		V/mV
				0°C	15	200		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				70°C	60	92		dB
				0°C	60	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		dB
				0°C	60	92		dB
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		420	1120	µA
				70°C		340	880	µA
				0°C		500	1280	µA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		C- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M4AC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		260	2000	μV
				Full range			3000	
		TLC27M9C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				70°C		8	300	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				70°C	7.8	8.7		
				0°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				70°C		0	50	
				0°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				70°C	15	230		
				0°C	15	320		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				70°C	60	94		
				0°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				70°C	60	94		
				0°C	60	92		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		570	1200	μA
				70°C		440	1120	
				0°C		690	1600	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

3 Operational Amplifiers

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	mV
		TLC27M4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	mV
				Full range			7	mV
		TLC27M4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		250	2000	µV
				Full range			3500	µV
		TLC27M9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	µV
				Full range			2000	µV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				85°C		24	1000	pA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				85°C		200	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				85°C	3	4		V
				−40°C	3	3.9		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	mV
				−40°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				85°C	15	130		V/mV
				−40°C	15	270		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				85°C	60	90		dB
				−40°C	60	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		dB
				−40°C	60	91		dB
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		420	1120	µA
				85°C		320	800	µA
				−40°C		630	1600	µA

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		I- SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
		TLC27M4AI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
		TLC27M4BI	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		260	2000	μV
				Full range			3500	
		TLC27M9I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	
				Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				85°C		26	1000	
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				85°C	7.8	8.7		
				−40°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				85°C		0	50	
				−40°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				85°C	15	220		
				−40°C	15	390		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				85°C	60	94		
				−40°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				85°C	60	94		
				−40°C	60	91		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		570	1200	μA
				85°C		410	1040	
				−40°C		900	1800	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M- SUFFIX TYPES			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		210	900	µV
				Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.7		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.1		pA
				125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 2.5 V, V_O = 2.5 V	25°C		0.6		pA
				125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 4	− 0.3 to 4.2		V
				Full range	0.0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		V
				125°C	3	4		
				− 55°C	3	3.9		
V_{OL}	Low-level output voltage		V_{ID} = − 100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				− 55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 100 kΩ	25°C	25	170		V/mV
				125°C	15	120		
				− 55°C	15	290		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	91		dB
				125°C	60	91		
				− 55°C	60	89		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				− 55°C	60	91		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 2.5 V, V_{IC} = 2.5 V	25°C		420	1120	µA
				125°C		280	720	
				− 55°C		680	1760	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDTIONS		M-SUFFIX TYPES MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27M9M	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		220	1200	µV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		2.1		µV/°C
I_{IO}	Input offset current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		V_{IC} = 5 V, V_O = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)			25°C	0.0 to 9	−0.3 to 9.2		V
				Full range	0.0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	8	8.7		V
				125°C	7.8	8.8		
				−55°C	7.8	8.6		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				125°C		0	50	
				−55°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 100 kΩ	25°C	25	275		V/mV
				125°C	15	190		
				−55°C	15	420		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				125°C	60	93		
				−55°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		dB
				125°C	60	94		
				−55°C	60	91		
I_{DD}	Supply current (four amplifiers)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		570	1200	µA
				125°C		360	960	
				−55°C		980	2000	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				70°C		0.36		
				0°C		0.46		
			V_{IPP} = 2.5 V	25°C		0.40		
				70°C		0.34		
				0°C		0.43		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				70°C		50		
				0°C		60		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				70°C		400		
				0°C		600		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				70°C		39°		
				0°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			C-SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				70°C		0.51		
				0°C		0.67		
			V_{IPP} = 5.5 V	25°C		0.56		
				70°C		0.46		
				0°C		0.61		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				70°C		30		
				0°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				70°C		510		
				0°C		710		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				70°C		42°		
				0°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/µs
				85°C		0.35		
				−40°C		0.51		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
				−40°C		0.48		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				85°C		45		
				−40°C		75		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				85°C		370		
				−40°C		770		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				85°C		38°		
				−40°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			I- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/µs
				85°C		0.47		
				−40°C		0.77		
			V_{IPP} = 5.5 V	25°C		0.56		
				85°C		0.44		
				−40°C		0.70		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				85°C		25		
				−40°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				85°C		480		
				−40°C		880		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				85°C		41°		
				−40°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				125°C		0.29		
				– 55°C		0.54		
			V_{IPP} = 2.5 V	25°C		0.40		
				125°C		0.28		
				– 55°C		0.50		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		55		kHz
				125°C		40		
				– 55°C		80		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		525		kHz
				125°C		330		
				– 55°C		850		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		40°		
				125°C		36°		
				– 55°C		44°		

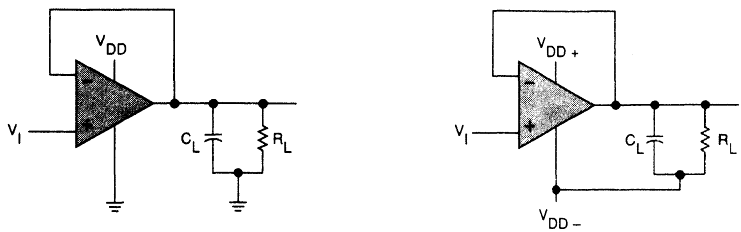
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDTIONS			M- SUFFIX TYPES MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				125°C		0.38		
				– 55°C		0.81		
			V_{IPP} = 5.5 V	25°C		0.56		
				125°C		0.35		
				– 55°C		0.73		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 2		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 1		25°C		35		kHz
				125°C		20		
				– 55°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		635		kHz
				125°C		440		
				– 55°C		960		
ϕ_m	Phase margin	f = B_1, V_i = 10 mV, C_L = 20 pF, See Figure 3		25°C		43°		
				125°C		39°		
				– 55°C		47°		

PARAMETER MEASUREMENT INFORMATION

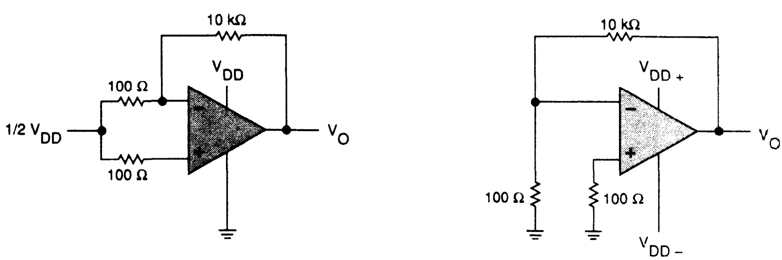
single-supply versus split-supply test circuits

Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



(a) Single-Supply (b) Split-Supply

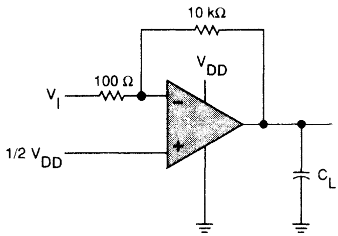
FIGURE 1. UNITY-GAIN AMPLIFIER



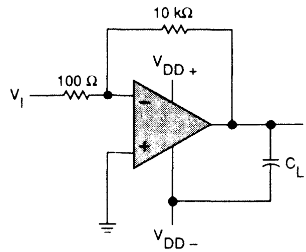
(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION



(a) Single-Supply



(b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

input bias current

Because of the high input impedance of the TLC27M4 and TLC27M9 op amps, attempts to measure the input bias current can result in erroneous readings. The typical bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1 Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2 Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

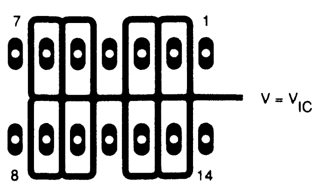


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS
(N AND J DUAL-IN-LINE PACKAGE)

PARAMETER MEASUREMENT INFORMATION

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 thru 19 in the Typical Characteristics section of this data sheet.

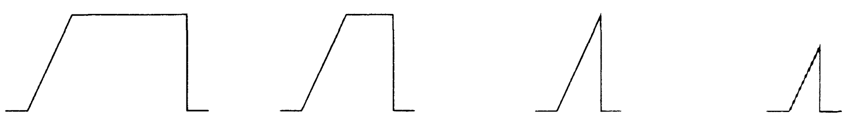
input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no affect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 1 kHz (b) B_{OM} > f > 1 kHz (c) f = B_{OM} (d) f > B_{OM}

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

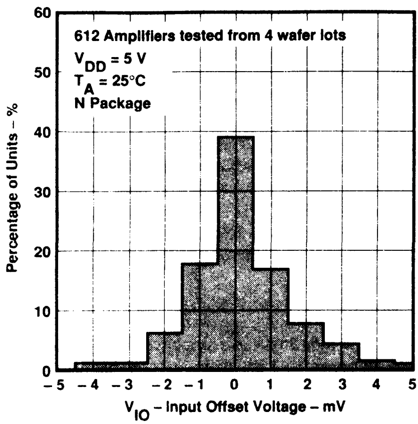


FIGURE 6

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

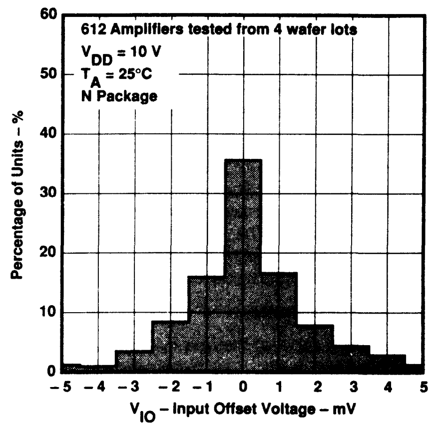


FIGURE 7

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

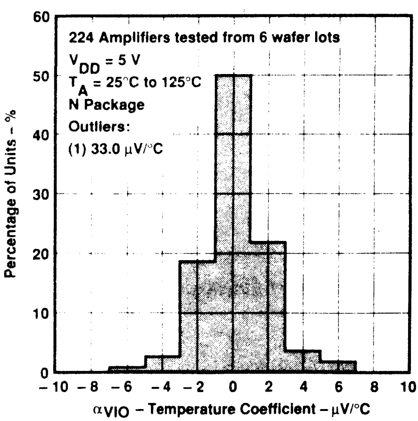


FIGURE 8

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

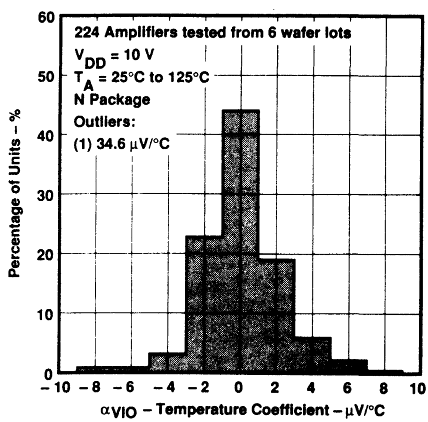


FIGURE 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

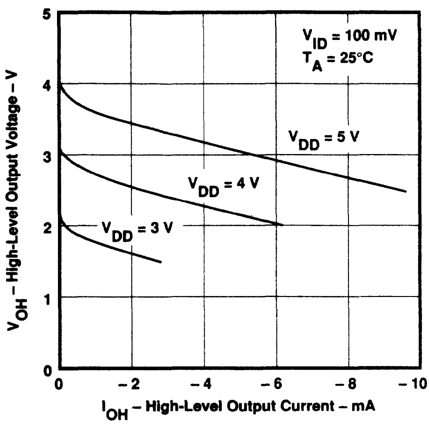


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

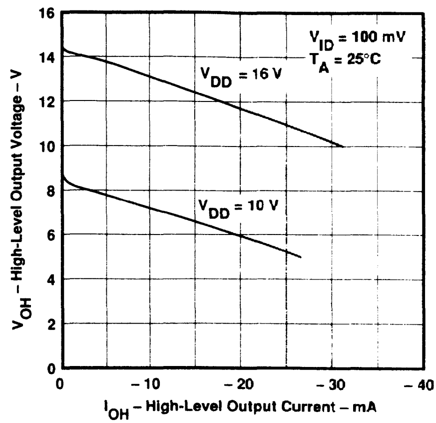


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

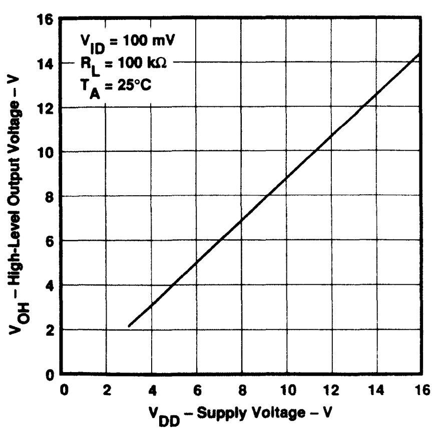


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

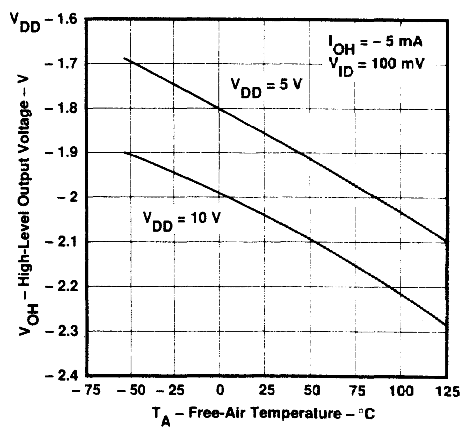


FIGURE 13

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

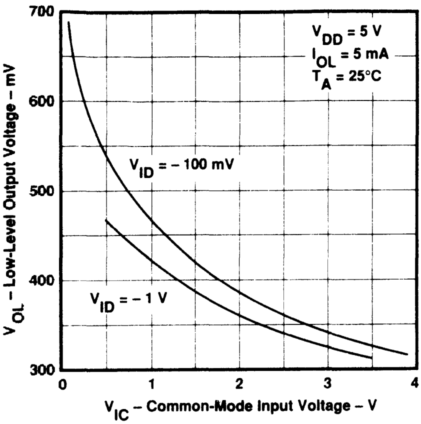


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

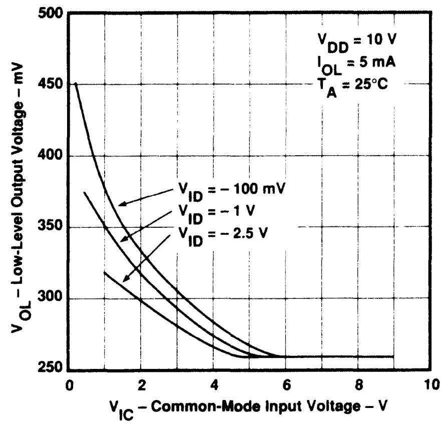


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

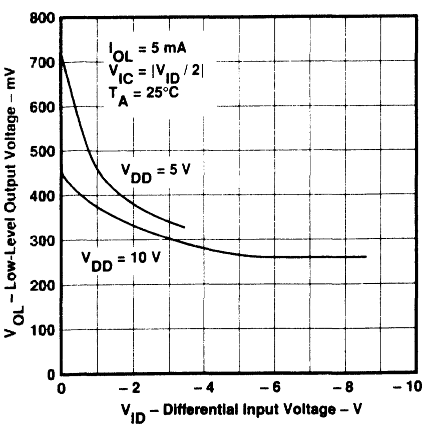


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

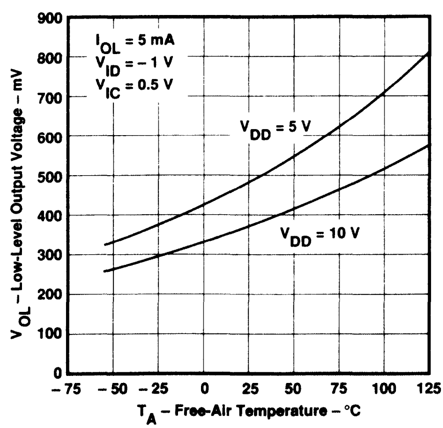


FIGURE 17

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

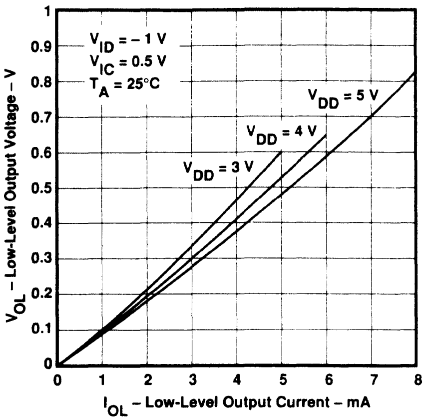


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

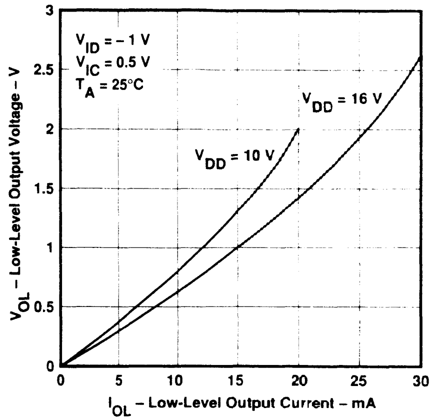


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

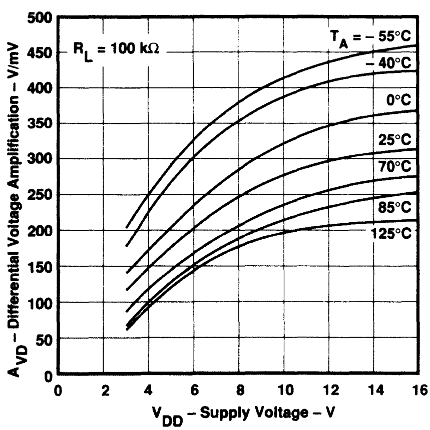


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

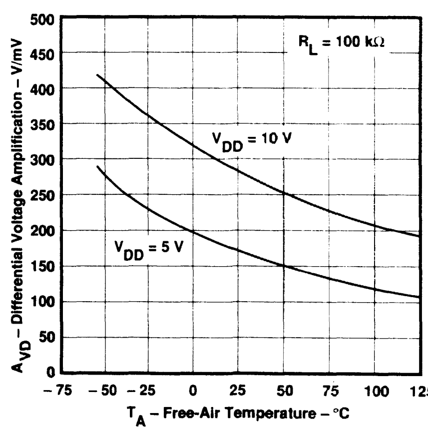


FIGURE 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

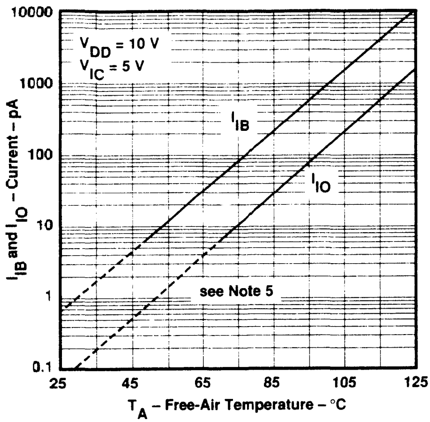


FIGURE 22

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

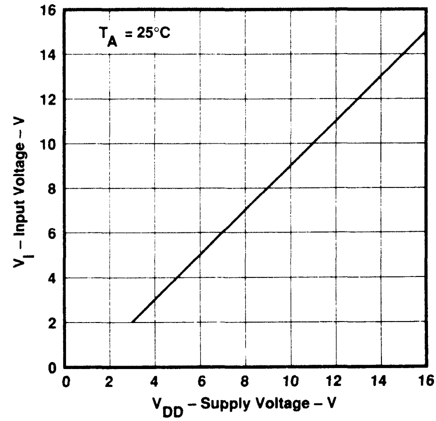


FIGURE 23

SUPPLY CURRENT vs SUPPLY VOLTAGE

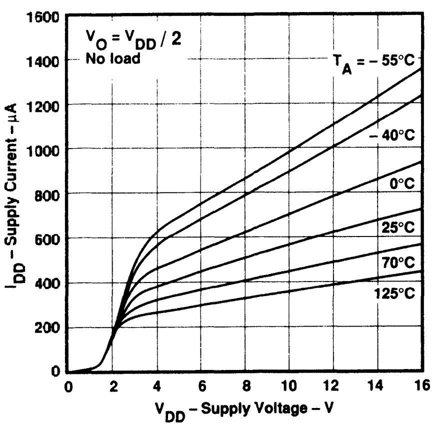


FIGURE 24

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

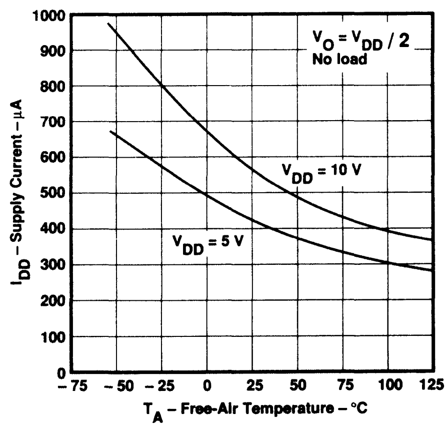


FIGURE 25

NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TEXAS INSTRUMENTS

3 Operational Amplifiers

TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

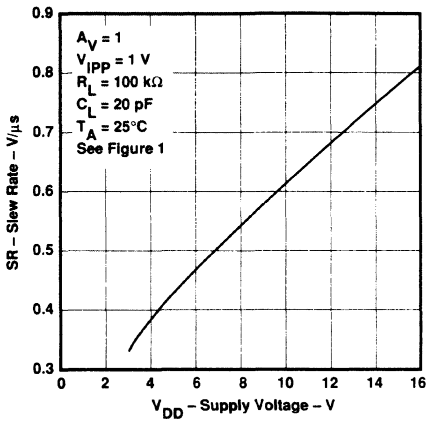


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

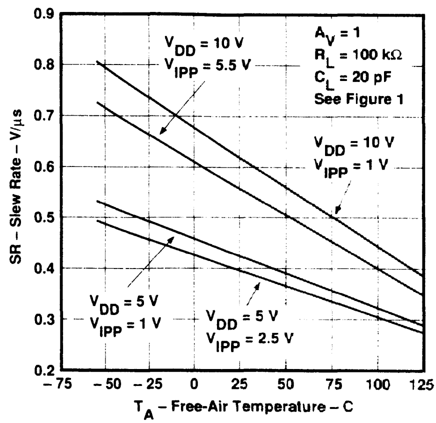


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

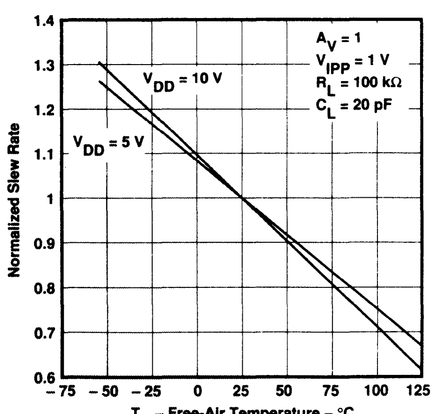


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

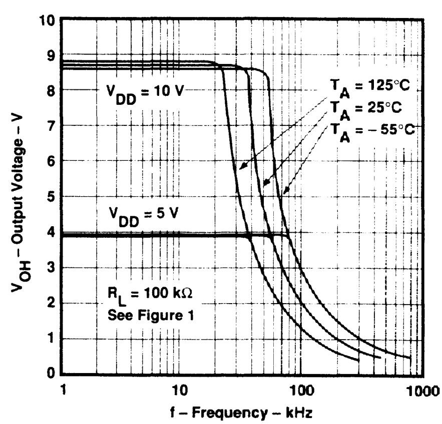


FIGURE 29

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

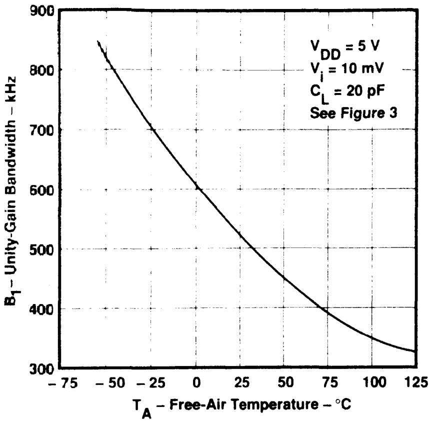


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

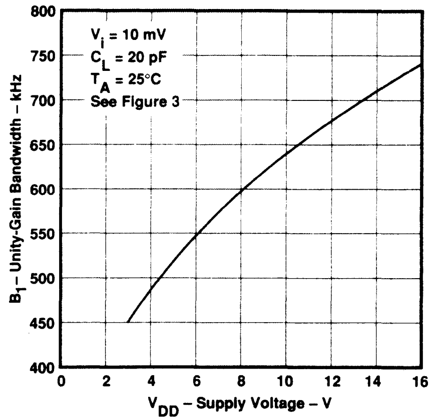


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

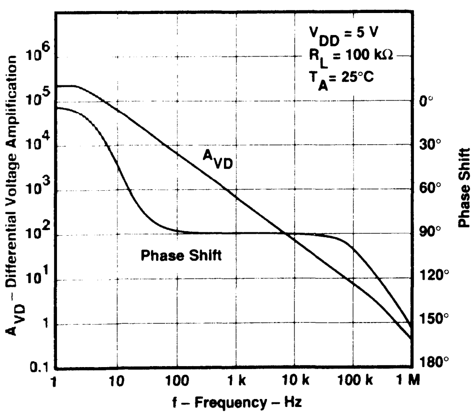


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

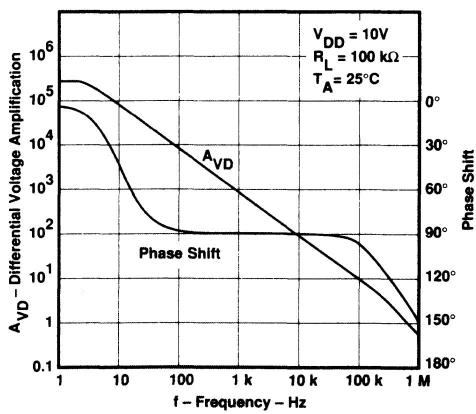


FIGURE 33

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

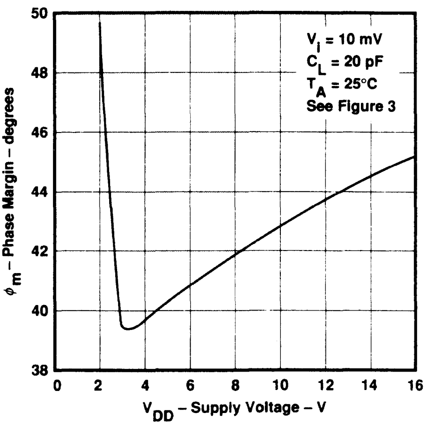


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

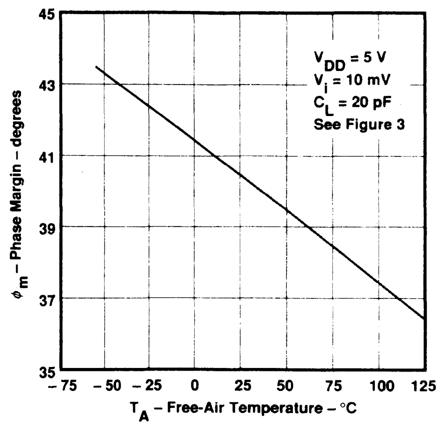


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

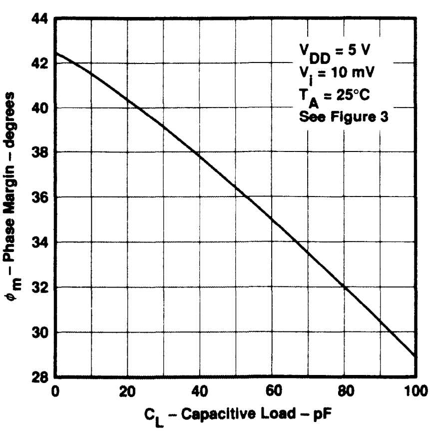


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

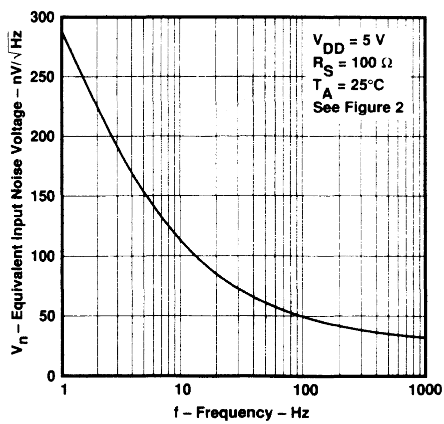


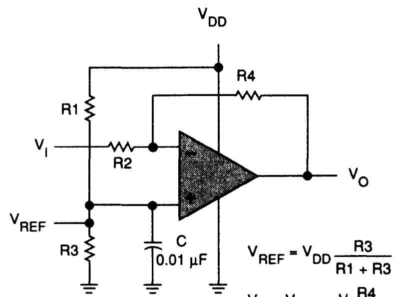
FIGURE 37

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27M4 and TLC27M9 will perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C- suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current consumption of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.



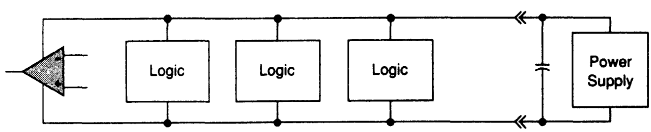
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = V_{REF} - V_I\frac{R4}{R2}$$

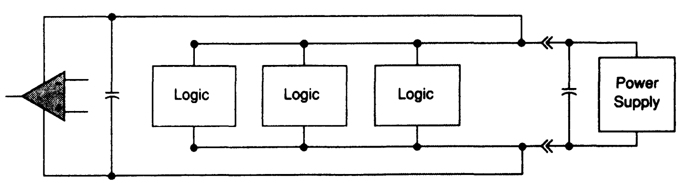
FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VERSUS SEPARATE SUPPLY RAILS

3 Operational Amplifiers

TYPICAL APPLICATION DATA

input characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

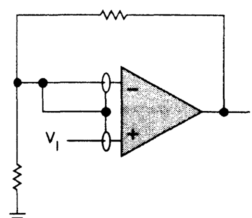
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the PARAMETER MEASUREMENT INFORMATION section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

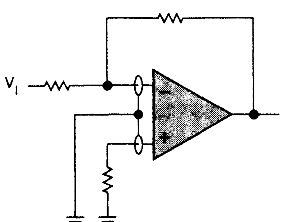
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

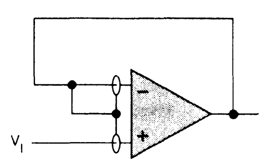
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier



(b) Inverting Amplifier



(c) Unity Gain Amplifier

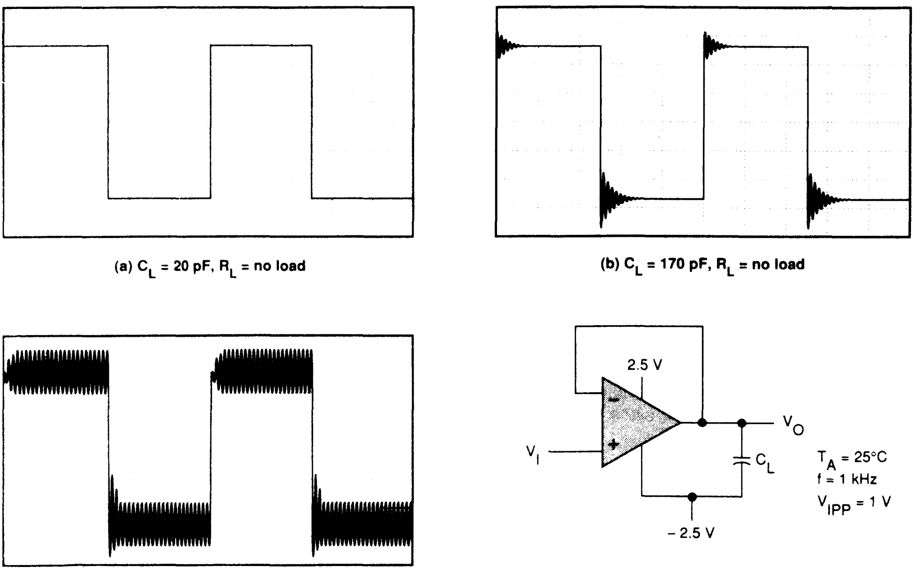
Figure 40. GUARD RING SCHEMES

TYPICAL APPLICATION DATA

output characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



(a) C_L = 20 pF, R_L = no load

(b) C_L = 170 pF, R_L = no load

(c) C_L = 190 pF, R_L = no load

(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor connected from the output to the positive supply rail. There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor, N4 (see Figure 42) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R6, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R6 acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

TYPICAL APPLICATION DATA

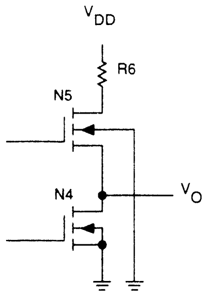


FIGURE 42. TLC27M4 / TLC27M9 OUTPUT STAGE

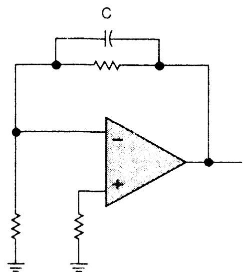


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

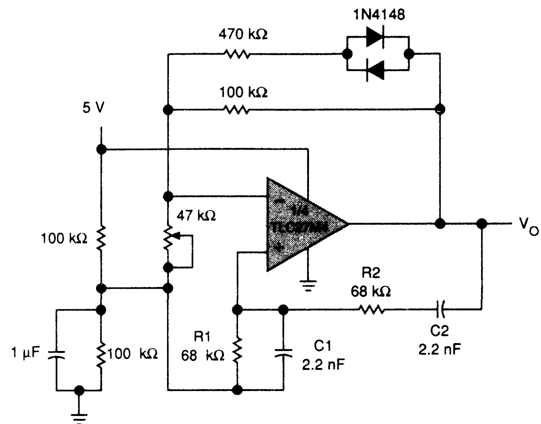
The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages at or below 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protect circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M4 and TLC27M9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and / or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

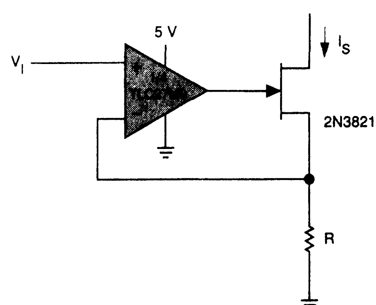
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$f_O = \frac{1}{2\pi \sqrt{R1R2C1C2}}$

FIGURE 44. WIEN OSCILLATOR

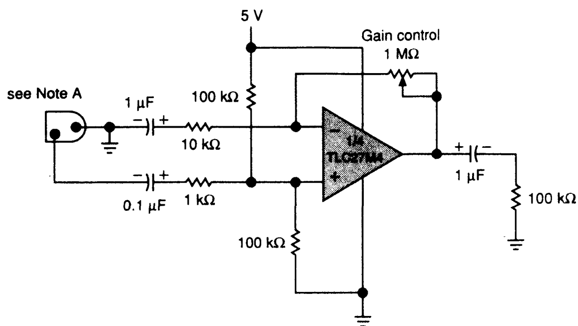


NOTES: V_I = 0 V TO 3 V

$I_S = \frac{V_I}{R}$

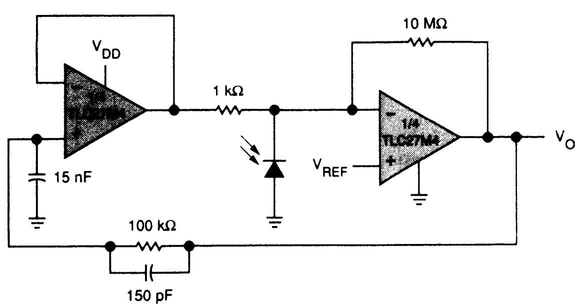
FIGURE 45. PRECISION LOW CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A: Low to medium impedance dynamic mike

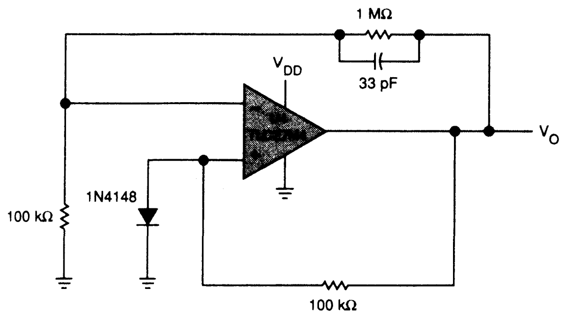
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5 V LOW POWER VOLTAGE REGULATOR

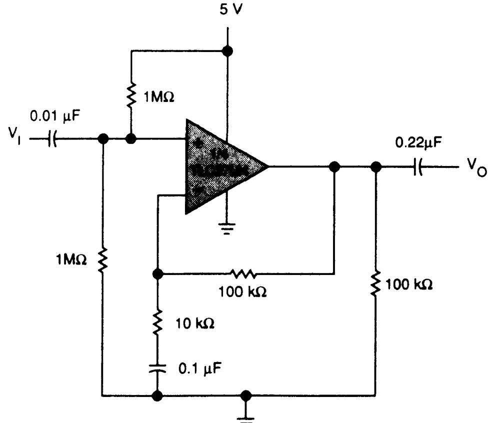


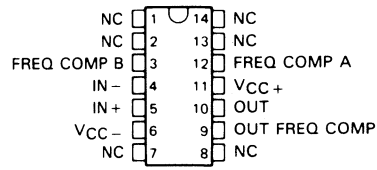
FIGURE 49. SINGLE RAIL A.C. AMPLIFIER

TYPES uA709AM, uA709M, uA709C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

D942, FEBRUARY 1971—REVISED AUGUST 1983

- **Common-Mode Input Range . . . ±10 V Typical**
- **Designed to be Interchangeable with Fairchild μA709A, μA709, and μA709C**
- **Maximum Peak-to-Peak Output Voltage Swing . . . 28-V Typical with 15-V Supplies**

uA709AM, uA709M . . . J OR W PACKAGE
(TOP VIEW)



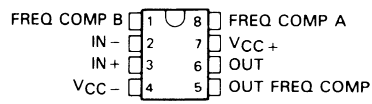
description

These circuits are general-purpose operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

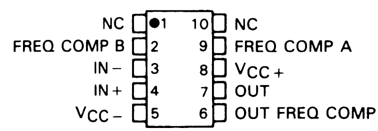
The uA709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the uA709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are guaranteed.

The uA709AM and uA709M are characterized for operation over the full military temperature range of −55 °C to 125 °C. The uA709C is characterized for operation from 0 °C to 70 °C.

uA709AM, uA709M . . . JG PACKAGE
uA709C . . . JG OR P PACKAGE
(TOP VIEW)

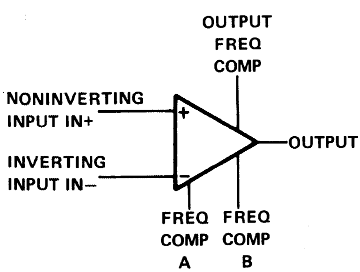


uA709AM, uA709M . . . U FLAT PACKAGE
(TOP VIEW)

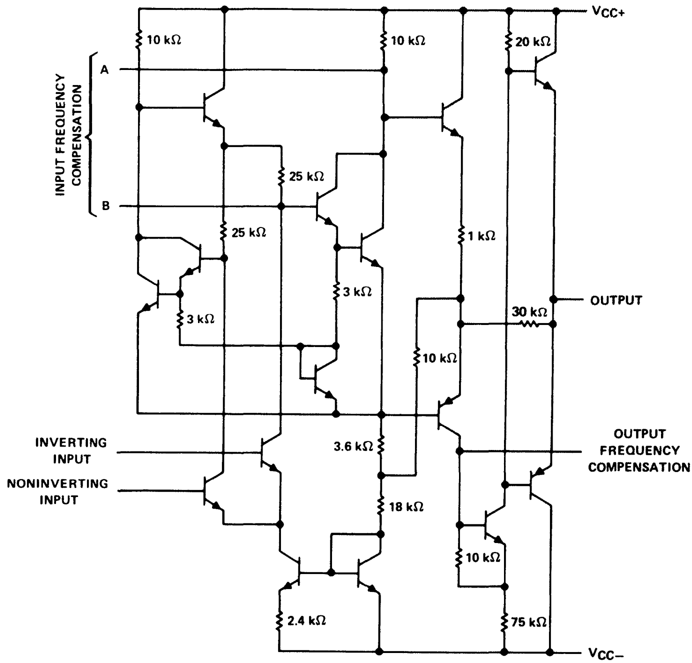


NC—No internal connection

symbol



schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA709AM uA709M	uA709C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation of uA709AM and uA709M above 70°C free-air temperature, refer to the Dissipation Derating Curves, Section 2. In the J and JG packages, uA709AM and uA709M chips are alloy-mounted; uA709C chips are glass-mounted.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 9$ V to ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		uA709AM MIN	uA709AM TYP‡	uA709AM MAX	uA709M MIN	uA709M TYP‡	uA709M MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S \leq 10$ kΩ	25°C		0.6	2		1	5	mV
			Full range			3			6	
α_{VIO}	Average temperature coefficient of input* offset voltage	$V_O = 0$, $R_S = 50$ Ω	Full range		1.8	10		3		μV/°C
		$V_O = 0$, $R_S = 10$ kΩ	Full range		4.8	25		6		
I_{IO}	Input offset current	$V_O = 0$	25°C		10	50		50	200	nA
			−55°C		40	250		100	500	
			125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input* offset current	$V_O = 0$	−55°C to 25°C		0.45	2.8				nA/°C
			25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current	$V_O = 0$	25°C		0.1	0.2		0.2	0.5	μA
			−55°C		0.3	0.6		0.5	1.5	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm} = \pm 15$ V	25°C	±8	±10		±8	±10		V
			Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L \geq 10$ kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm} = \pm 15$ V, $R_L = 2$ kΩ	25°C	20	26		20	26		
		$V_{CC\pm} = \pm 15$ V, $R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C		45			45		V/mV
			Full range	25		70	25		70	
r_i	Input resistance		25°C	350	750		150	400		kΩ
			−55°C	85	185		40	100		
r_o	Output resistance	$V_O = 0$ See Note 6	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	80	110		70	90		dB
			Full range	80			70			
k_{SVS}	Power supply sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V	25°C		40	100		25	150	μV/V
			Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm} = \pm 15$ V, No load, $V_O = 0$	25°C		2.5	3.6		2.6	5.5	mA
			−55°C		2.7	4.5				
			125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm} = \pm 15$ V, No load, $V_O = 0$	25°C		75	108		78	165	mW
			−55°C		81	135				
			125°C		63	90				

† All characteristics are specified under open-loop with zero common-mode input voltage unless otherwise specified. Full range for uA709AM and uA709M is −55°C to 125°C.

‡ All typical values are at $V_{CC\pm} = \pm 15$ V.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

*For M suffix devices these parameters are guaranteed but not tested.

3 Operational Amplifiers

electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm} = \pm 15$ V)

PARAMETER		TEST CONDITIONS†		uA709C MIN	uA709C TYP	uA709C MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		2	7.5	mV
			Full range			10	
I_{IO}	Input offset current	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		100	500	nA
			Full range			750	
I_{IB}	Input bias current	$V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$	25°C		0.3	1.5	μA
			Full range			2	
V_{ICR}	Common-mode input voltage range		25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 10$ kΩ	25°C	24	28		V
			Full range	24			
		$R_L = 2$ kΩ	25°C	20	26		
		$R_L \geq 2$ kΩ	Full range	20			
A_{VD}	Large-signal differential voltage amplification	$R_L \leq 2$ kΩ, $V_O = \pm 10$ V	25°C	15	45		V/mV
			Full range	12			
r_i	Input resistance		25°C	50	250		kΩ
			Full range	35			
r_o	Output resistance	$V_O = 0$, See Note 6	25°C		150		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	65	90		dB
k_{SVS}	Supply voltage sensitivity	$V_{CC} = \pm 9$ V to ± 15 V	25°C		25	200	μV/V
P_D	Total power dissipation	$V_O = 0$ No load	25°C		80	200	mW

†All characteristics are specified under open-loop operation with zero volts common-mode voltage unless otherwise specified. Full range for uA709C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		uA709AM uA709M uA709C MIN	TYP	MAX	UNIT
t_r	Rise time *	$V_I = 20$ mV, $R_L = 2$ kΩ, See Figure 1	$C_L = 0$		0.3	1	μs
	Overshoot factor *		$C_L = 100$ pF		6%	30%	

PARAMETER MEASUREMENT INFORMATION

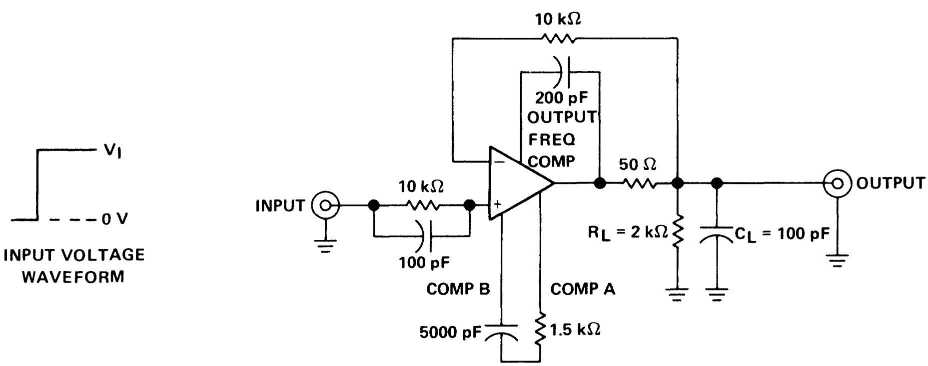


FIGURE 1—RISE TIME AND SLEW RATE

*For M suffix devices these parameters are guaranteed but not tested.

TEXAS INSTRUMENTS

TYPES uA741M, uA741C GENERAL-PURPOSE OPERATIONAL AMPLIFIER

D920, NOVEMBER 1970 – REVISED AUGUST 1983

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-up**
- **Designed to be Interchangeable with Fairchild μA741M, μA741C**

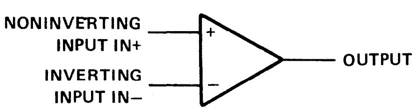
description

The uA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

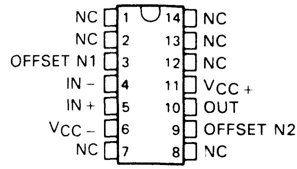
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA741M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA741C is characterized for operation from 0°C to 70°C.

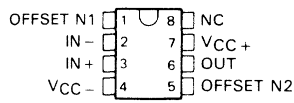
symbol



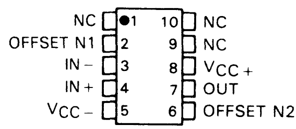
uA741M . . . J PACKAGE
(TOP VIEW)



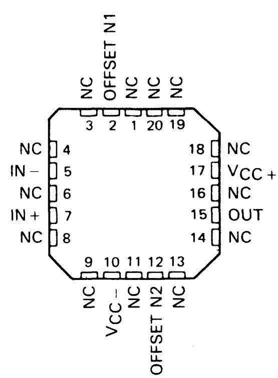
uA741M . . . JG PACKAGE
uA741C . . . D, P, OR JG PACKAGE
(TOP VIEW)



uA741M . . . U FLAT PACKAGE
(TOP VIEW)

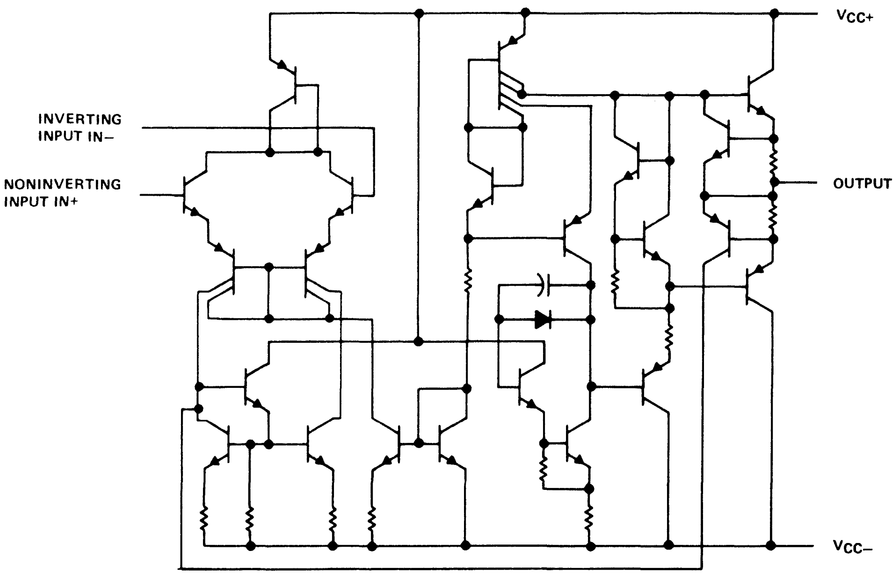


uA741M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA741M	uA741C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage any input (see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK, J, JG, or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG packages, uA741M chips are alloy mounted; uA741C chips are glass mounted.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		uA741M			uA741C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$	25°C		±15			±15		mV
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±14		±12	±14		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			
		$R_L = 2\ k\Omega$	25°C	±10	±13		±10	±13		
		$R_L \geq 2\ k\Omega$	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$	25°C	50	200		20	200		V/mV
		$V_O = \pm 10$ V	Full range	25			15			
r_i	Input resistance *		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current (see note 7)		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, $V_O = 0$	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, $V_O = 0$	25°C		50	85		50	85	mW
			Full range			100			100	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA741M is −55°C to 125°C and for uA741C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

NOTE 7: A short circuit from the output to V_{CC+} with a rise time greater than 0.5 V/µs can cause the short circuit protection to fail. Under these circumstances, the short circuit cannot be sustained.

*For M suffix devices this parameter is guaranteed but not tested.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	uA741M			uA741C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ,		0.3			0.3		μs
	Overshoot factor	$C_L = 100$ pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

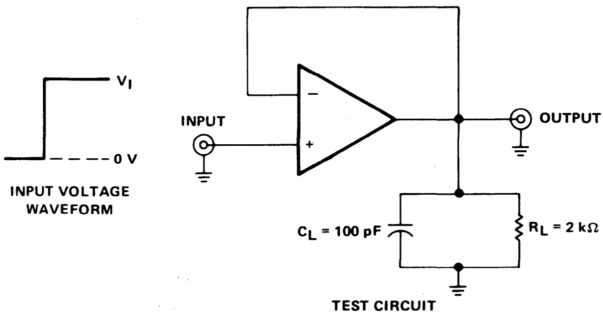


FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

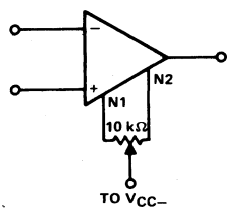


FIGURE 2 – INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

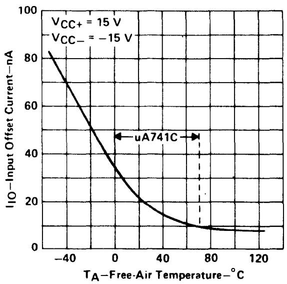


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

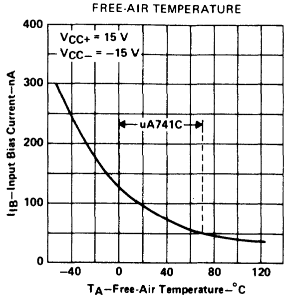


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

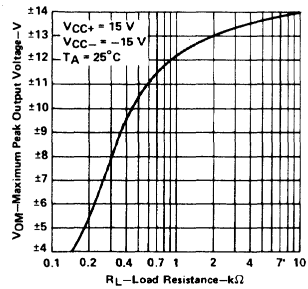


FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

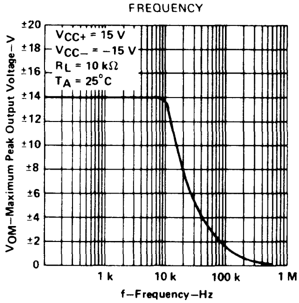


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

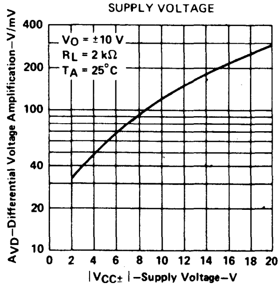


FIGURE 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

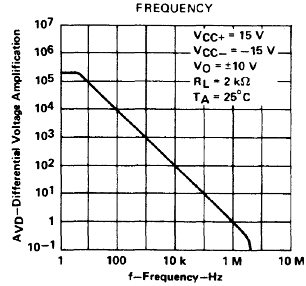


FIGURE 8

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

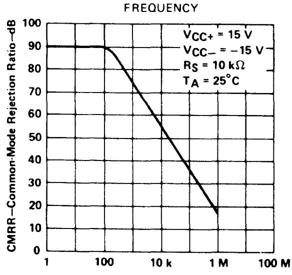


FIGURE 9

OUTPUT VOLTAGE
vs
ELAPSED TIME

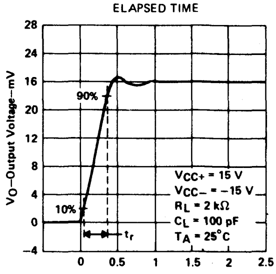


FIGURE 10

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

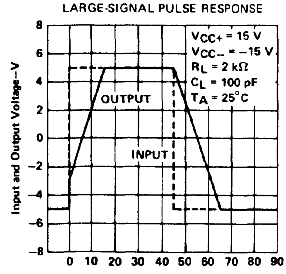


FIGURE 11

TYPES uA747M, uA747C DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 11446, FEBRUARY 1971–REVISED OCTOBER 1979

- No Frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- No Latch-up
- Designed to be Interchangeable with Fairchild μA747M and μA747C

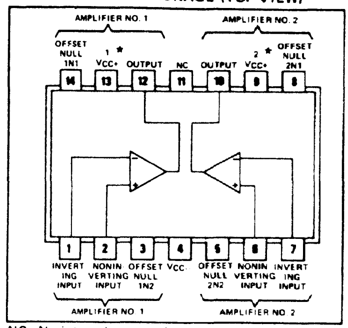
description

The uA747 is a dual general-purpose operational amplifier featuring offset-voltage null capability. Each half is electrically similar to uA741.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA747M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA747C is characterized for operation from 0°C to 70°C.

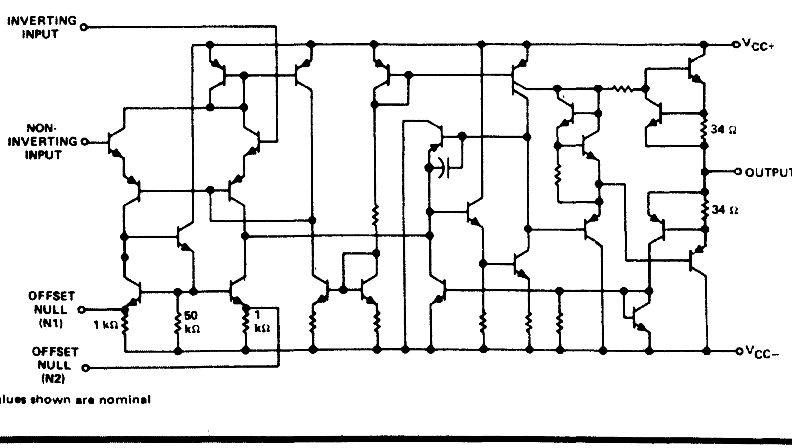
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



NC–No internal connection

* On parts date-coded 7701 or higher, the two positive supply terminals (1 V_{CC+} and 2 V_{CC+}) are connected together internally. For parts without this internal connection, order uA747-1M or uA747-1C.

schematic (each amplifier)



Resistor values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			uA747M	uA747C	UNIT
Supply voltage V_{CC+} (see Note 1)			22	18	V
Supply voltage V_{CC-} (see Note 1)			−22	−18	V
Differential input voltage (see Note 2)			±30	±30	V
Input voltage any input (see Notes 1 and 3)			±15	±15	V
Voltage between any offset null terminal (N1/N2) and V_{CC-}			±0.5	±0.5	V
Duration of output short-circuit (see Note 4)			unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	Each amplifier		500	500	mW
	Total package	J,N, or W package	800	800	mW
Operating free-air temperature range			−55 to 125	0 to 70	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds		J or W package	300	300	°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds		N package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA747M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature and for total package ratings, refer to Dissipation Derating Table. In the J package, uA747M chips are alloy-mounted; uA747C chips are glass-mounted.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

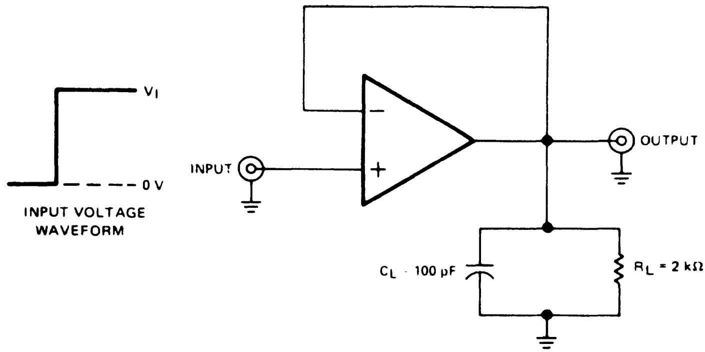
PARAMETER		TEST CONDITIONS†		uA747M MIN	uA747M TYP	uA747M MAX	uA747C MIN	uA747C TYP	uA747C MAX	UNIT
V_{IO}	Input offset voltage	$R_S \le 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10\ k\Omega$	25°C	24	28		24	28		V
		$R_L \ge 10\ k\Omega$	Full range	24			24			
		$R_L = 2\ k\Omega$	25°C	20	26		20	26		
		$R_L \ge 2\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \ge 2\ k\Omega$, $V_O = \pm 10$ V	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \le 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$R_S \le 10\ k\Omega$	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (each amplifier)	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

† All characteristics are specified under open-loop operation. Full range for uA747M is −55°C to 125°C and for uA747C is 0°C to 70°C.
NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS	uA747M			uA747C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Rise time	V_I = 20 mV, R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot factor	C_L = 100 pF, See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

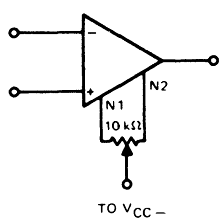


FIGURE 2—INPUT OFFSET VOLTAGE NULL CIRCUIT

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	800 mW	11.0 mW/°C	77°C
J (Glass-Mounted Chip)	800 mW	8.2 mW/°C	52°C
N	800 mW	9.2 mW/°C	63°C
W	800 mW	8.0 mW/°C	50°C

Also see Dissipation Derating Curves, Section 2.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

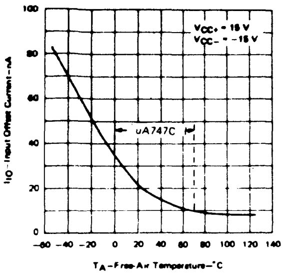


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

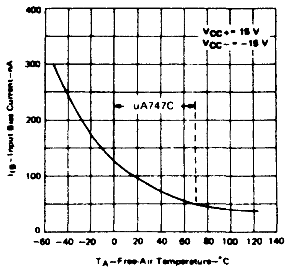


FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

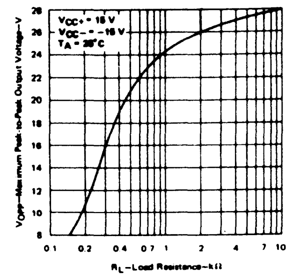


FIGURE 5

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

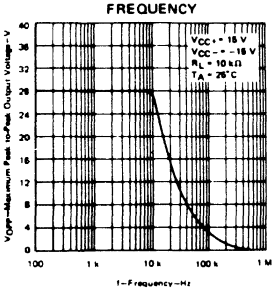


FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

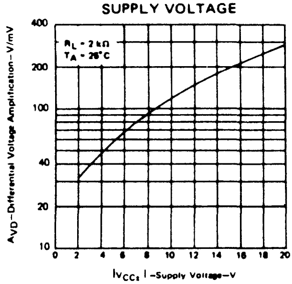


FIGURE 7

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

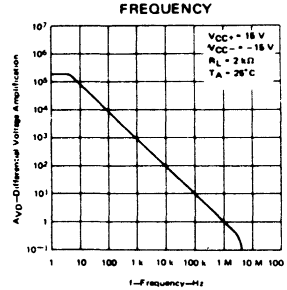


FIGURE 8

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

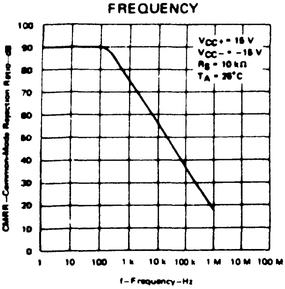


FIGURE 9

OUTPUT VOLTAGE
vs
ELAPSED TIME

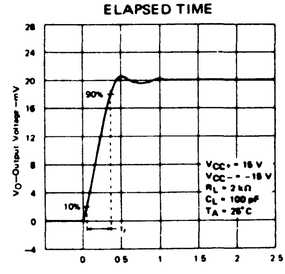


FIGURE 10

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

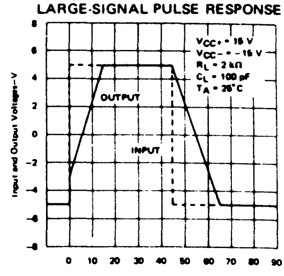


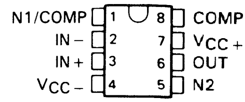
FIGURE 11

TYPES uA748M, uA748C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

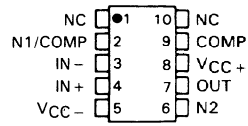
D921, DECEMBER 1970—REVISED AUGUST 1983

- **Frequency and Transient Response Characteristics Adjustable**
- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**
- **Same Pin Assignments as uA709**

uA748M . . . JG
uA748C . . . D, JG, OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



uA748M . . . U FLAT PACKAGE
(TOP VIEW)



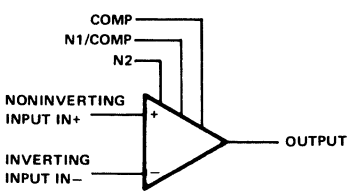
NC—No internal connection

description

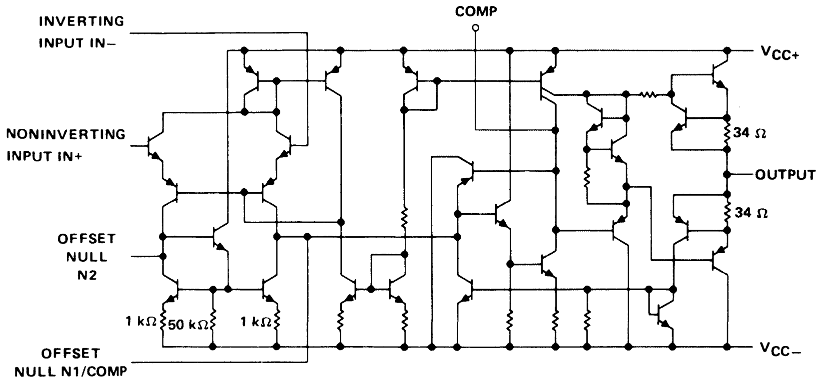
The uA748 is a general-purpose operational amplifier that offers the same advantages and attractive features as the uA741 except for internal compensation. External compensation can be as simple as a 30-pF capacitor for unity-gain conditions and, when the closed-loop gain is greater than one, can be changed to obtain wider bandwidth or higher slew rate. This circuit features high gain, large differential and common-mode input voltage range, and output short-circuit protection. Input offset voltage adjustment can be provided by connecting a variable resistor between the offset null pins as shown in Figure 12.

The uA748M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA748C is characterized for operation from 0°C to 70°C.

symbol



schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

		uA748M	uA748C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA748M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG package, uA748M chips are alloy-mounted; uA748C chips are glass-mounted.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V, C_C = 30 pF

PARAMETER		TEST CONDITIONS†		uA748M			uA748C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	50	200		20	200		V/mV
			Full range	25			15			
r_i	Input resistance *		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, V_O = 0	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, V_O = 0	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, V_O = 0	25°C		50	85		50	85	mW
			Full range			100			100	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA748M is −55°C to 125°C and for uA748C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

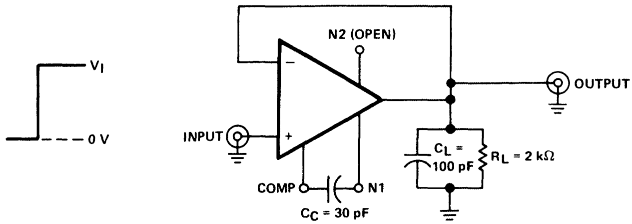
operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	uA748M			uA748C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.3			0.3		µs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, C_C = 30 pF, See Figure 1		0.5			0.5		V/µs

*For M suffix devices this parameter is guaranteed but not tested.

3 Operational Amplifiers

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

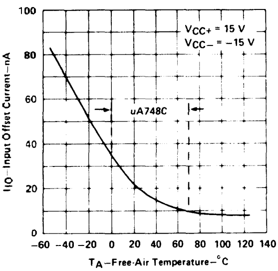


FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

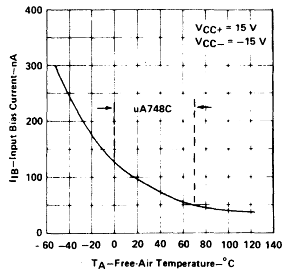


FIGURE 3

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

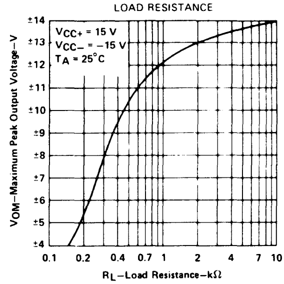


FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

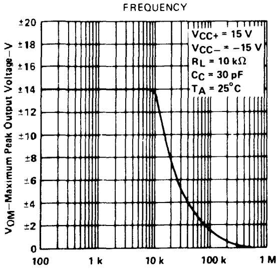


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

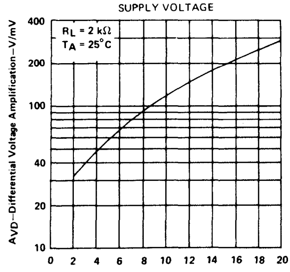


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

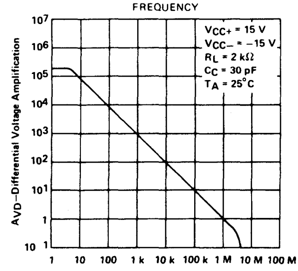


FIGURE 7

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

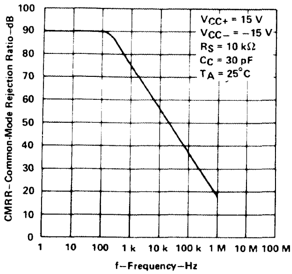


FIGURE 8

OUTPUT VOLTAGE
vs
ELAPSED TIME

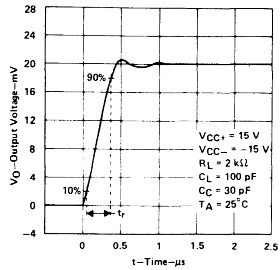


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

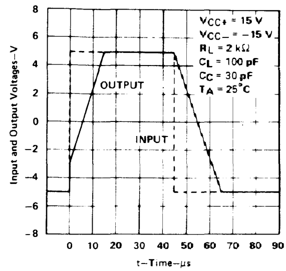
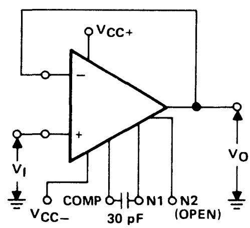


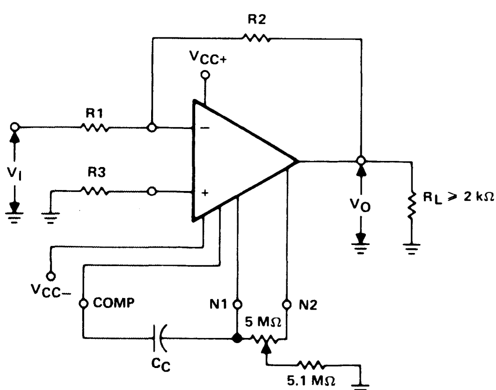
FIGURE 10

TYPICAL APPLICATION DATA



r_i = 400 MΩ, r_o < Ω,
C_i = 1 pF, BW = 1 MHz

FIGURE 11–UNITY-GAIN VOLTAGE FOLLOWER



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\text{ pF}}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 12–INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

3

Operational Amplifiers

CONTENTS

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to the specified level.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left[\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left[\frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at the specified level.

High-Level Strobe Current ($I_{IH(S)}$)

The current flowing into or out of* the strobe at a high-level voltage.

Low-Level Strobe Current ($I_{IL(S)}$)

The current flowing out of* the strobe at a low-level voltage.

High-Level Strobe Voltage ($V_{IH(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed not to interfere with the operation of the comparator.

Low-Level Strobe Voltage ($V_{IL(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed to force the output high or low, as specified, independently of the differential inputs.

Input Voltage Range (V_I)

The range of voltage that if exceeded at either input terminal will cause the comparator to cease functioning properly.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

*Current out of a terminal is given as a negative value.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the comparator to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Differential Input Voltage Range (V_{ID})

The range of voltage between the two input terminals that if exceeded will cause the comparator to cease functioning properly.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant.

High-Level Output Voltage (V_{OH})

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Voltage (V_{OL})

The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

High-Level Output Current, (I_{OH})

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Current, (I_{OL})

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Output Resistance (r_O)

The resistance between an output terminal and ground.

Common-Mode Rejection Ration (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Current (I_{CC+}, I_{CC-})

The current into* the V_{CC+} or V_{CC-} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

*Current out of a terminal is given as a negative value.

Response Time

The interval between the application of an input step function and the instant at when the output crosses the logic threshold voltage.
NOTE: The input step drives the comparator from some initial condition sufficient to saturate the output (or in the case of high-to-low-level response time, to turn the output off) to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

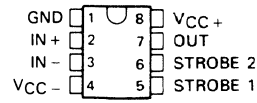
Strobe Release Time

The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from its active logic level to its inactive logic level.

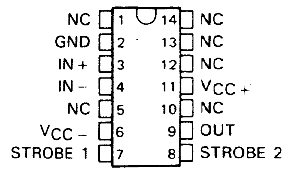
LM106, LM206, LM306 DIFFERENTIAL COMPARATORS WITH STROBES

- **Fast Response Times**
- **Improved Gain and Accuracy**
- **Fan-Out to 10 Series 54/74 TTL Loads**
- **Strobe Capability**
- **Short-Circuit and Surge Protection**
- **Designed to be Interchangeable with National Semiconductor LM106, LM206, and LM306**

LM106 . . . JG PACKAGE
LM206, LM306 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LM106 . . . J DUAL-IN-LINE
OR W FLAT PACKAGE
(TOP VIEW)



NC – No internal connection

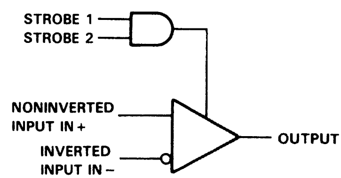
description

The LM106, LM206, and LM306 are high-speed voltage comparators with differential inputs, a low-impedance high-sink-current (100 mA) output, and two strobe inputs. These devices detect low-level analog or digital signals and can drive digital logic or lamps and relays directly. Short-circuit protection and surge-current limiting is provided.

A low-level input at either strobe causes the output to remain high regardless of the differential input. When both strobe inputs are either open or at a high logic level, the output voltage is controlled by the differential input voltage. The circuit will operate with any negative supply voltage between −3 V and −12 V with little difference in performance.

The LM106 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM206 is characterized for operation from −25°C to 85°C, and the LM306 from 0°C to 70°C.

functional block diagram

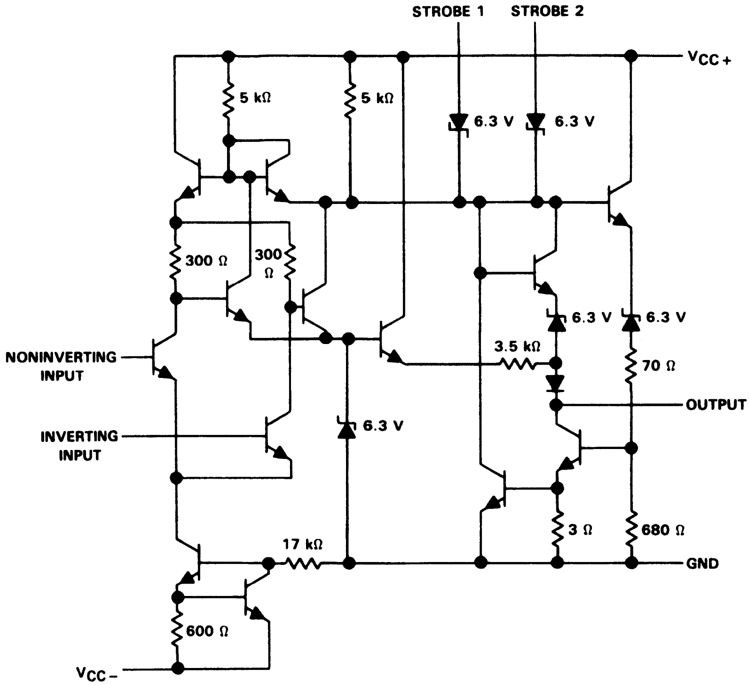


AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE				
		SMALL OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CERAMIC DIP (J)	CERAMIC FLAT (W)
0°C to 70°C	5 mV	LM306D	LM306P	LM306JG	–	–
−25°C to 85°C	2 mV	LM206D	LM206P	LM206JG	–	–
−55°C to 125°C	2 mV	–	–	LM106JG	LM106J	LM106W

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM306DR)

schematic



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) .... 15 V
Supply voltage, V_{CC-} (see Note 1) .... −15 V
Differential input voltage (see Note 2) .... ±5 V
Input voltage range (either input, see Notes 1 and 3) .... ±7 V
Strobe voltage range (see Note 1) .... 0 V to V_{CC+}
Output voltage (see Note 1) .... 24 V
Voltage from output to V_{CC-} .... 30 V
Duration of output short-circuit to ground (see Note 4) .... 10 s
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range: LM106 .... −55°C to 125°C
LM206 .... −25°C to 85°C
LM306 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, or W package .... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package .... 260°C

NOTES: 1. All voltage values, except differential voltages and the voltage from the output to V_{CC-}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 7 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	600 mW	5.8 mW/°C	46°C	464 mW	377 mW	–
J	600 mW	11.0 mW/°C	95°C	600 mW	600 mW	275 mW
JG (LM106)	600 mW	8.4 mW/°C	78°C	600 mW	546 mW	210 mW
JG (LM206, LM306)	600 mW	6.6 mW/°C	59°C	528 mW	429 mW	–
P	600 mW	8.0 mW/°C	75°C	600 mW	520 mW	–
W	600 mW	8.0 mW/°C	75°C	600 mW	520 mW	200 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −3 V to −12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM106‡, LM206			LM306			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \le 200\ \Omega$, See Note 5		25°C		0.5§	2		1.6§	5	mV
				Full range			3			6.5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$, See Note 5		Full range		3	10		5	20	µV/°C
I_{IO}	Input offset current	See Note 5		25°C		0.7‡	3		1.8‡	5	µA
				MIN		2	7		1	7.5	
				MAX		0.4	3		0.5	5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 5		MIN to 25°C		15	75		24	100	nA/°C
				25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	V_O = 0.5 V to 5 V		MIN to 25°C			45			40	µA
				25°C to MAX		7‡	20		16‡	25	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)}$ = 0.4 V		Full range		−1.7‡	−3.2		−1.7‡	−3.2	mA
$V_{IH(S)}$	High-level strobe voltage			Full range	2.2			2.2			V
$V_{IL(S)}$	Low-level strobe voltage			Full range			0.9			0.9	V
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V to −12 V		Full range	±5			±5			V
V_{ID}	Differential input voltage range			Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0.5 V to 5 V		25°C		40‡			40‡		V/mV
V_{OH}	High-level output voltage	I_{OH} = −400 µA	V_{ID} = 5 mV	Full range	2.5		5.5				V
			V_{ID} = 8 mV	Full range				2.5		5.5	
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	V_{ID} = −5 mV	25°C		0.8‡	1.5				V
			V_{ID} = −7 mV	25°C					0.8‡	2	
		I_{OL} = 50 mA	V_{ID} = −5 mV	Full range			1				
			V_{ID} = −8 mV	Full range						1	
		I_{OL} = 16 mA	V_{ID} = −5 mV	Full range			0.4				
			V_{ID} = −8 mV	Full range						0.4	
I_{OH}	High-level output current	V_{OH} = 8 V to 24 V	V_{ID} = 5 mV	MIN to 25°C		0.02‡	1				µA
				25°C to MAX			100				
			V_D = 7 mV	MIN to 25°C					0.02‡	2	
			V_{ID} = 8 mV	25°C to MAX						100	
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load		Full range		6.6‡	10		6.6‡	10	mA
I_{CC-}	Supply current from V_{CC-}	No load		Full range		−1.9‡	−3.6		−1.9‡	−3.6	mA

† Unless otherwise noted, all characteristics are measured with both strobes open.

‡ LM106 limits are performed by equivalent testing unless otherwise noted.

§ These typical values are at V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C. Full range (MIN to MAX) for LM106 is −55°C to 125°C; for LM206 is −25°C to 85°C; and for LM306 is 0°C to 70°C.

NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output down to the low range (V_{OL}) or up to the high range (V_{OH}). Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS†	LM106, LM206			LM306			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Response time, low-to-high-level output	R_L = 390 Ω to 5 V, C_L = pF, See Note 6		28	40		28	40	ns

NOTE 6: The response time specified is for a 100-mV input step with 5-mV overdive and is the interval between the input step function and the instant when the output crosses 1.4 V.

4 Voltage Comparators

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

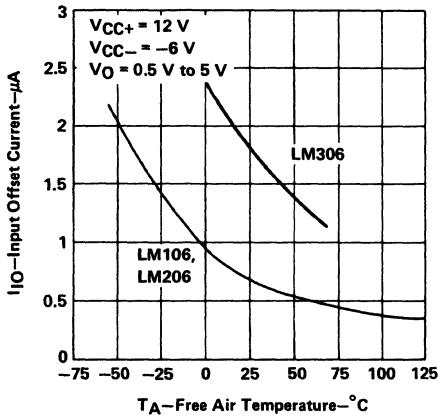


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

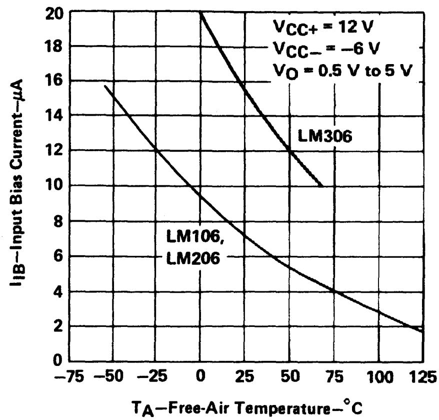


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

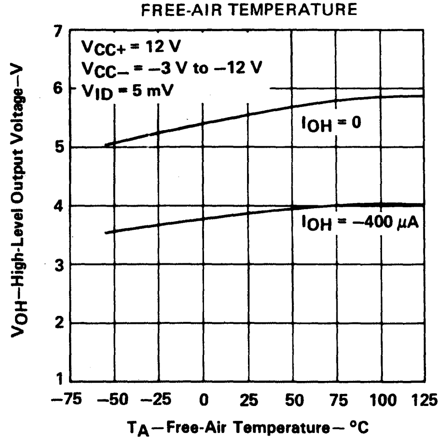


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

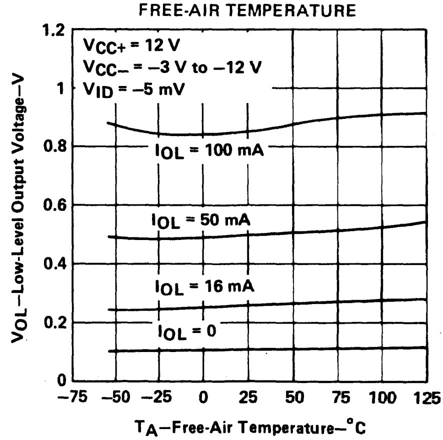


FIGURE 4

† Data for free-air temperature outside the range specified in the absolute maximum ratings for LM206 or LM306 is not applicable.

4 Voltage Comparators

TYPICAL CHARACTERISTICS†

VOLTAGE TRANSFER CHARACTERISTICS

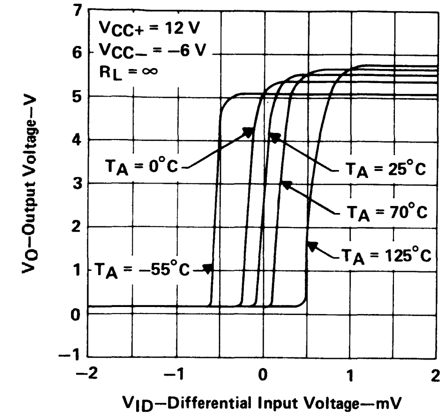


FIGURE 5

OUTPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

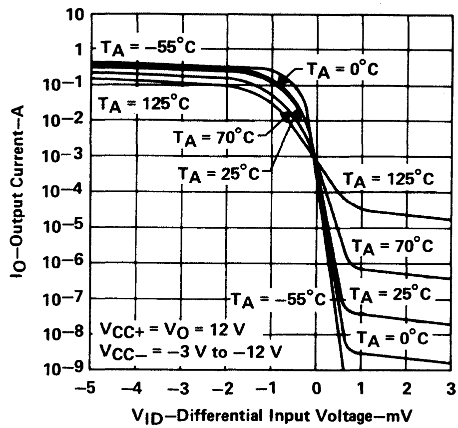


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

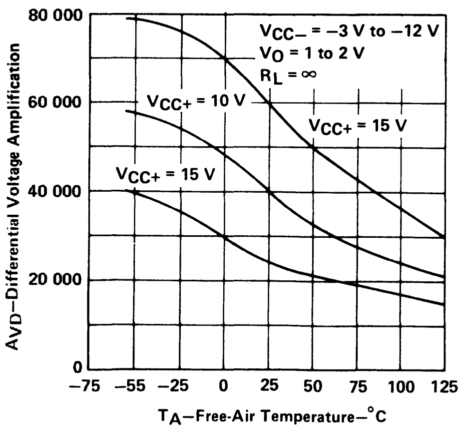


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

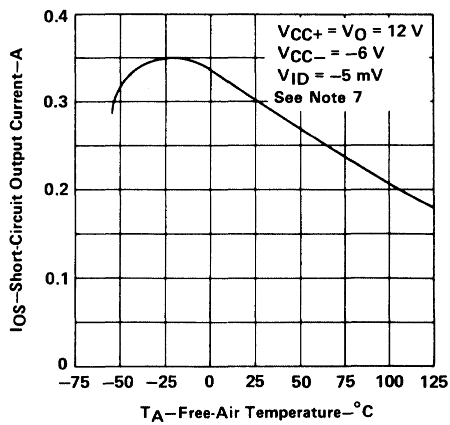


FIGURE 8

† Data for free-air temperature outside the range specified in the absolute maximum ratings for LM206 or LM306 is not applicable.
NOTE 7: This parameter was measured using a single 5-ms pulse.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS†

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

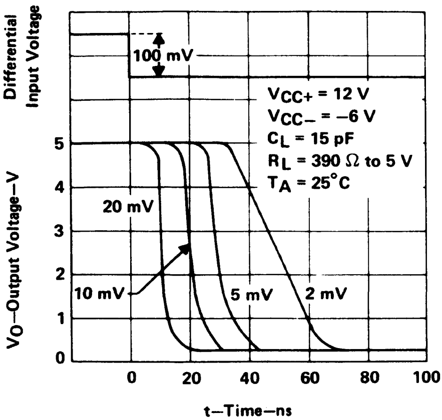


FIGURE 9

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

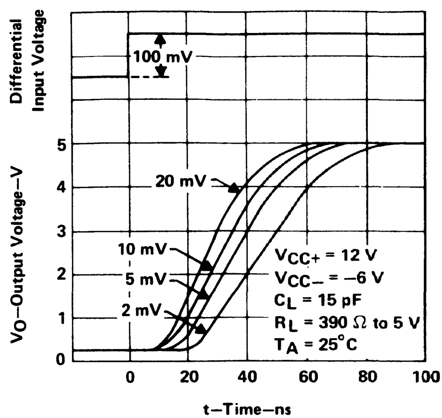


FIGURE 10

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

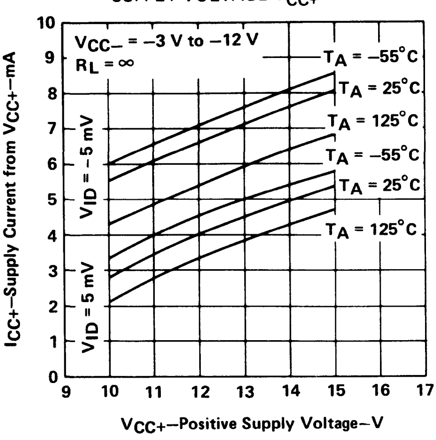


FIGURE 11

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

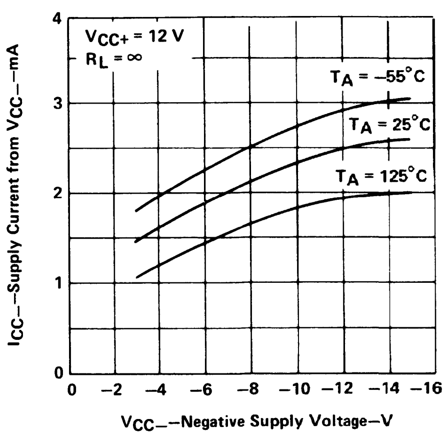


FIGURE 12

† Data for free-air temperature outside the range specified in the absolute maximum ratings for LM206 or LM306 is not applicable.

TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

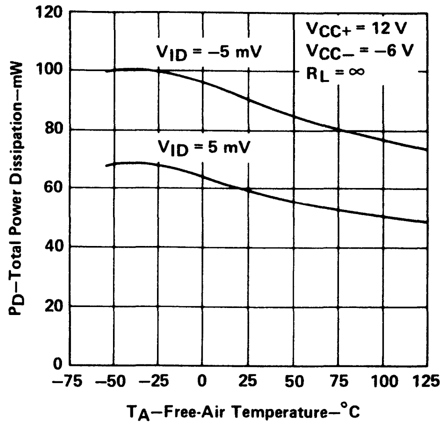


FIGURE 13

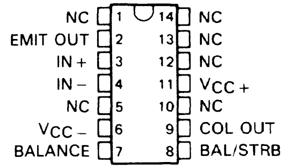
† Data for free-air temperature outside the range specified in the absolute maximum ratings for LM206 or LM306 is not applicable.

TEXAS INSTRUMENTS

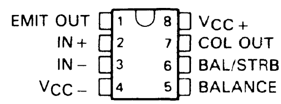
D1312, SEPTEMBER 1973—REVISED MARCH 1988

- **Fast Response Times**
- **Strobe Capability**
- **Designed to be Interchangeable with National Semiconductor LM111, LM211, and LM311**
- **Maximum Input Bias Current . . . 300 nA**
- **Maximum Input Offset Current . . . 70 nA**
- **Can Operate from Single 5-V Supply**

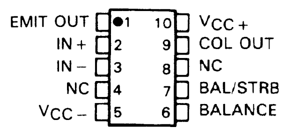
LM111 . . . J PACKAGE
(TOP VIEW)



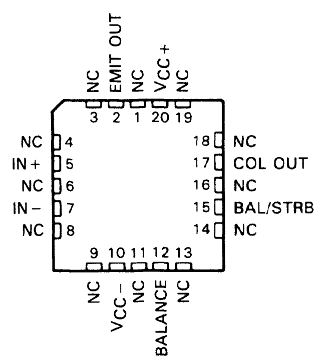
LM111 . . . JG PACKAGE
LM211, LM311 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LM111 . . . U FLAT PACKAGE
(TOP VIEW)



LM111 . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



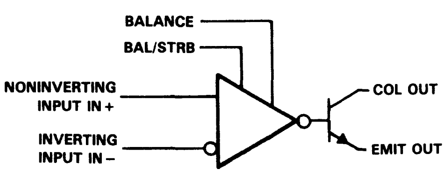
NC—No internal connection

description

The LM111, LM211, and LM311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltage, including ±15-V supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+} or V_{CC-}. Offset balancing and strobe capability are available and the outputs can be wire-OR connected. If the strobe is low, the output will be in the off state regardless of the differential input.

The LM111 is characterized for operation over the full military range of −55°C to 125°C. The LM211 is characterized for operation from −25°C to 85°C, and the LM311 is characterized for operation from 0°C to 70°C.

functional block diagram

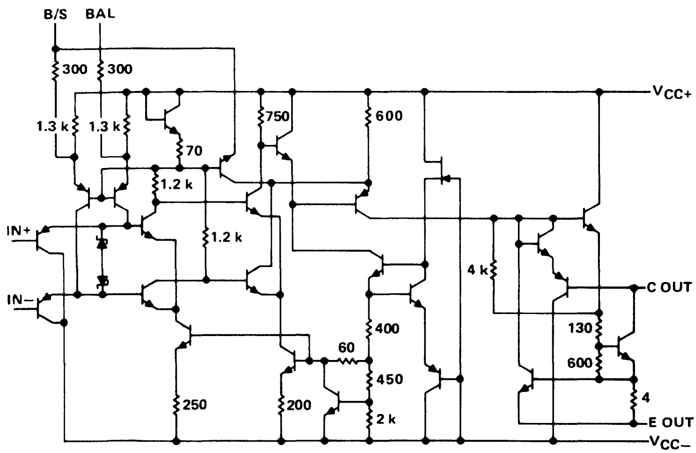


AVAILABLE OPTIONS

OPERATING TEMPERATURE RANGE	V_{IO} MAX AT T_A = 25°C	PACKAGE					
		D SMALL OUTLINE	FK CERAMIC CHIP CARRIER	J CERAMIC DIP	JG CERAMIC DIP	P PLASTIC DIP	U FLATPACK
−55°C to 125°C	3 mV		LM111FK	LM111J			LM111U
−40°C to 85°C	3 mV	LM211D+			LM211JG	LM211P	
0°C to 70°C	7.5 mV	LM311D+			LM311JG	LM311P	

†The D package is available in tape and reel. Add an R suffix when ordering, e.g., LM311DR.

schematic



BAL	Balance
B/S	Balance/Strobe
C OUT	Collector Output
E OUT	Emitter Output
IN+	Noninverting Input
IN−	Inverting Input
NC	No Internal Connection
V_{CC+}	Positive Supply Voltage
V_{CC-}	Negative Supply Voltage

Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM111	LM211	LM311	UNIT
Supply voltage, V_{CC+} (see Note 1)	18	18	18	V
Supply voltage, V_{CC-} (see Note 1)	−18	−18	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)	±15	±15	±15	V
Voltage from emitter output to V_{CC-}	30	30	30	V
Voltage from collector output to V_{CC-}	50	50	40	V
Duration of output short-circuit (see Note 4)	10	10	10	s
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK Package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, FK, or U package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D or P package		260	260	°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	–
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J (LM111)	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	8.2 mW/°C	89°C	500 mW	500 mW	–
JG (LM111)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	–
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	–
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 volts, whichever is less.
4. The output may be shorted to ground or either power supply.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM111, LM211 MIN	LM111, LM211 TYP‡	LM111, LM211 MAX	LM311 MIN	LM311 TYP‡	LM311 MAX	UNIT
V_{IO}	Input offset voltage	See Note 5		25°C		0.7	3		2	7.5	mV
				Full range			4			10	
I_{IO}	Input offset current	See Note 5		25°C		4	10		6	50	nA
				Full range			20			70	
I_{IB}	Input bias current	V_O = 1 V to 14 V		25°C		75	100		100	250	nA
				Full range			150			300	
$I_{IL(S)}$	Low-level strobe current (see Note 6)	$V_{(strobe)}$ = 0.3 V, $V_{ID} \le -10$ mV		25°C		−3			−3		mA
V_{ICR}	Common-mode input voltage range			Full range	13 to −14.5	13.8 to −14.7		13 to −14.5	13.8 to −14.7		V
A_{VD}	Large-signal differential voltage amplification	V_O = 5 V to 35 V, R_L = 1 kΩ		25°C	40	200		40	200		V/mV
I_{OH}	High-level (collector) output current	I_{strobe} = −3 mA, V_{ID} = 5 mV,	V_{OH} = 35 V	25°C		0.2	10				nA
				Full range			0.5				μA
		V_{ID} = 5 mV,	V_{OH} = 35 V	25°C					0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	I_{OL} = 50 mA	V_{ID} = −5 mV	25°C		0.75	1.5				V
			V_{ID} = −10 mV	25°C					0.75	1.5	
		V_{CC+} = 4.5 V, V_{CC-} = 0, I_{OL} = 8 mA	V_{ID} = −6 mV	Full range		0.23	0.4				
			V_{ID} = −10 mV	Full range					0.23	0.4	
I_{CC+}	Supply current from V_{CC+}, output low	V_{ID} = −10 mV,	No load	25°C		5.1	6		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-}, output high	V_{ID} = 10 mV,	No load	25°C		−4.1	−5		−4.1	−5	mA

†Unless otherwise noted, all characteristics are measured with the balance and balance/strobe terminals open and the emitter output grounded. Full range for LM111 is −55°C to 125°C, for LM211 is −25°C to 85°C, and for LM311 is 0°C to 70°C.

‡All typical values are at T_A = 25°C.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pull-up resistor of 7.5 kΩ to V_{CC+}. Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. The strobe should not be shorted to ground; it should be current driven at −3 to −5 mA, e.g., see Figures 13 and 27.

switching characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	R_C = 500 Ω to 5 V, C_L = 5 pF, See Note 7		115		ns
Response time, high-to-low-level output			165		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

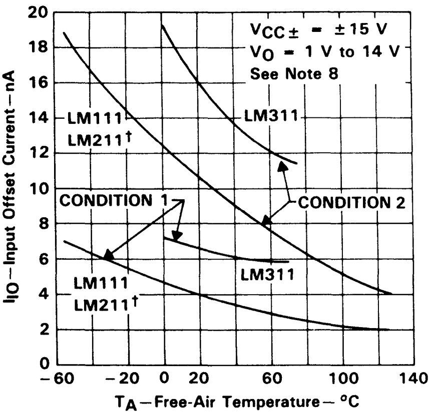


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

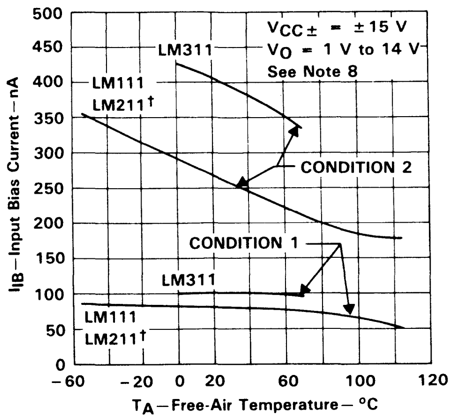


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS

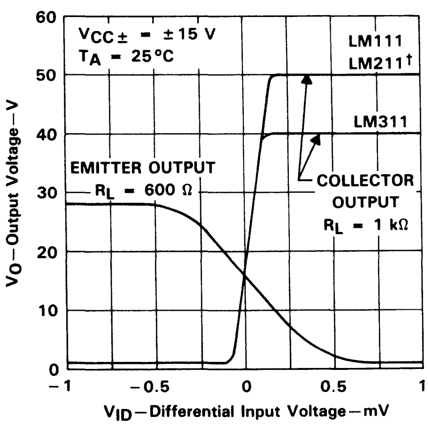
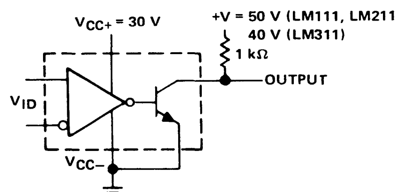
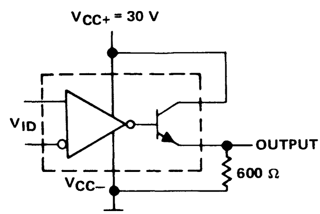


FIGURE 3



COLLECTOR OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3



EMITTER OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

NOTE 8: Condition 1 is with the balance and balance/strobe terminals open. Condition 2 is with the balance and balance/strobe terminals connected to V_{CC+}.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

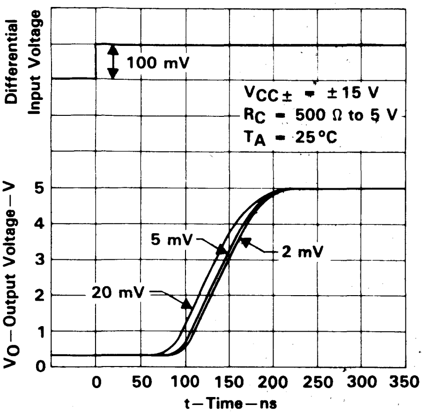


FIGURE 4

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

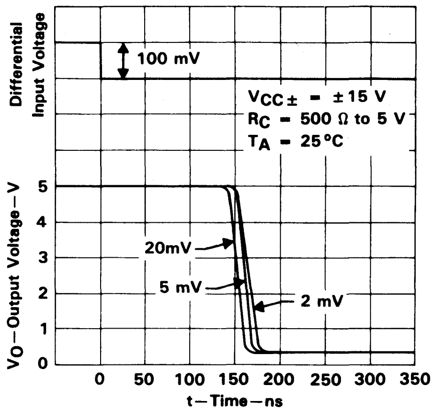
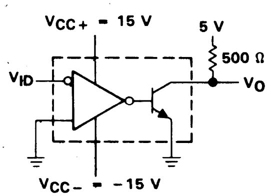


FIGURE 5



TEST CIRCUIT FOR FIGURES 4 AND 5

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

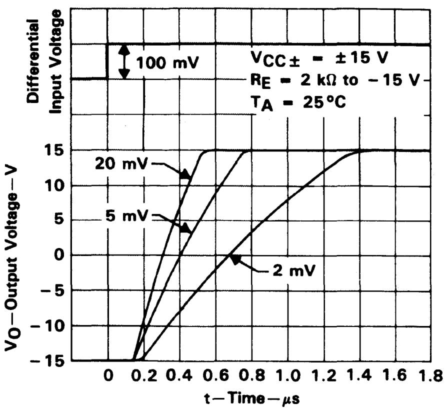


FIGURE 6

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

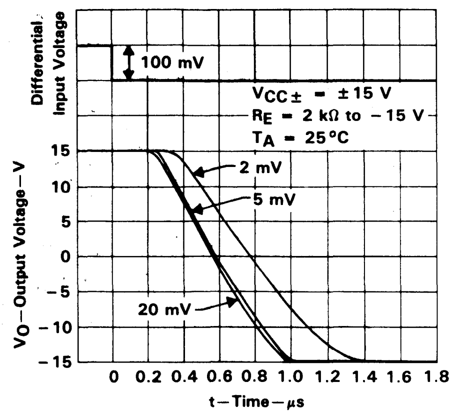
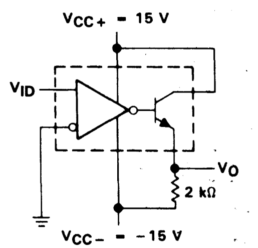


FIGURE 7



TEST CIRCUIT FOR FIGURES 6 AND 7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT and DISSIPATION
vs
OUPUT VOLTAGE

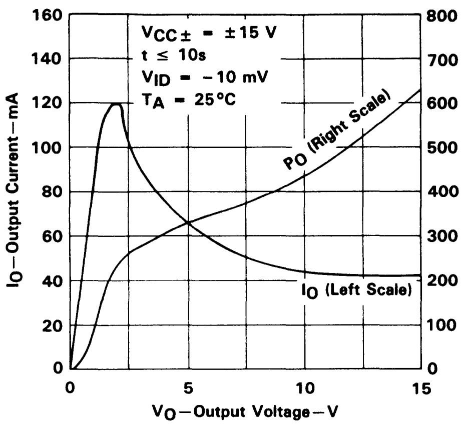


FIGURE 8

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

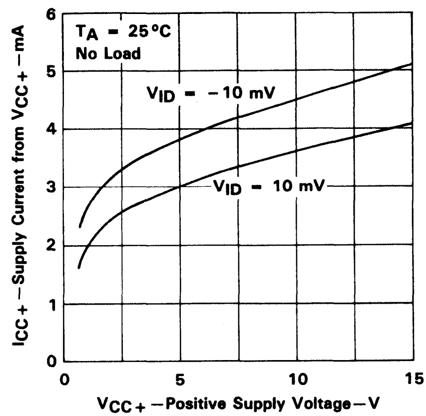


FIGURE 9

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

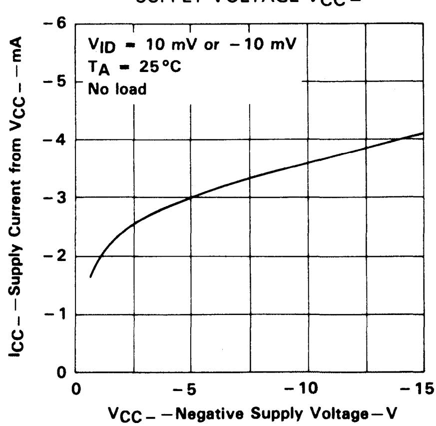


FIGURE 10

4 Voltage Comparators

TEXAS INSTRUMENTS

TYPICAL APPLICATION DATA

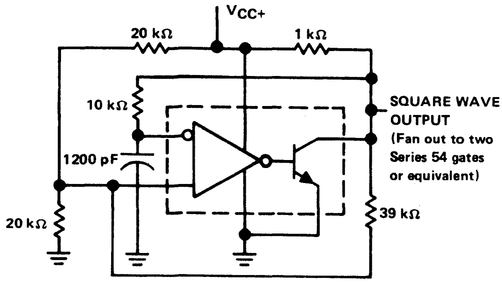


FIGURE 11. 100 kHz FREE-RUNNING MULTIVIBRATOR

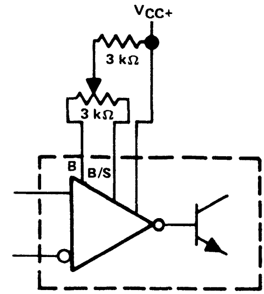


FIGURE 12. OFFSET BALANCING

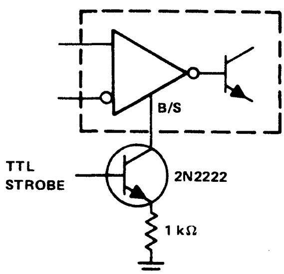


FIGURE 13. STROBING

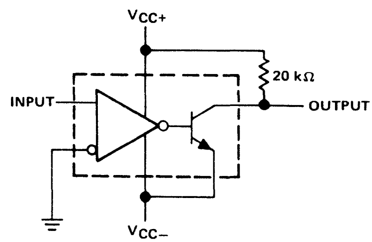
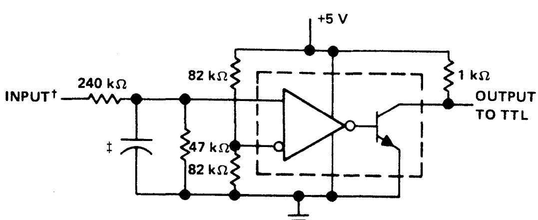


FIGURE 14. ZERO-CROSSING DETECTOR



†Resistor values shown are for a 0-to-30-V logic swing and a 15-V threshold.

‡May be added to control speed and reduce susceptibility to noise spikes.

FIGURE 15. TTL INTERFACE WITH HIGH-LEVEL LOGIC

4

Voltage Comparators

TYPICAL APPLICATION DATA

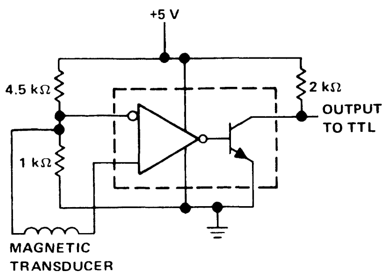


FIGURE 16. DETECTOR FOR MAGNETIC TRANSDUCER

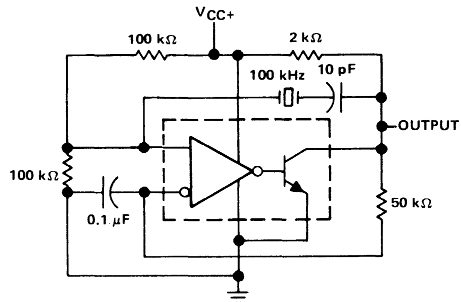


FIGURE 17. 100 kHz CRYSTAL OSCILLATOR

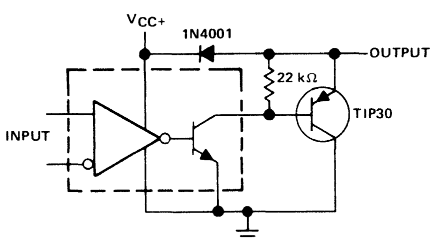
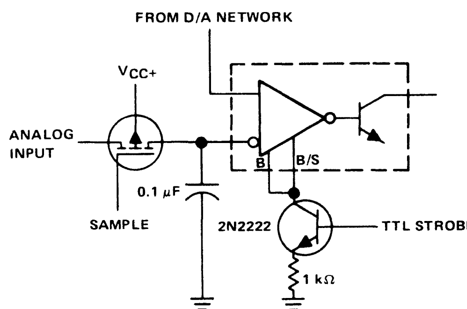


FIGURE 18. COMPARATOR AND SOLENOID DRIVER



Typical input current is 50 pA with inputs strobed off.

FIGURE 19. STROBING BOTH INPUT AND OUTPUT STAGES SIMULTANEOUSLY

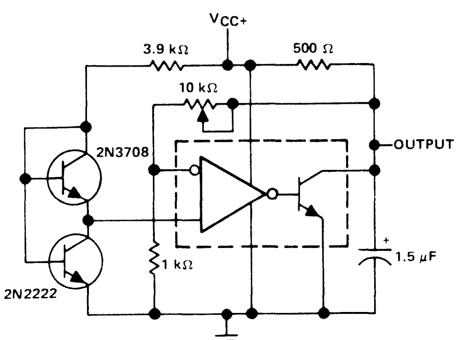


FIGURE 20. LOW-VOLTAGE ADJUSTABLE REFERENCE SUPPLY

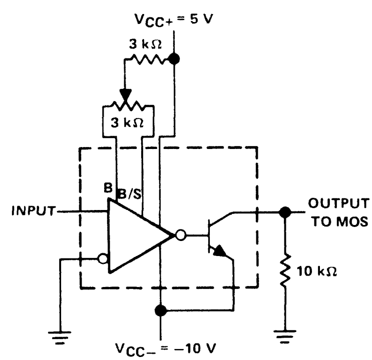
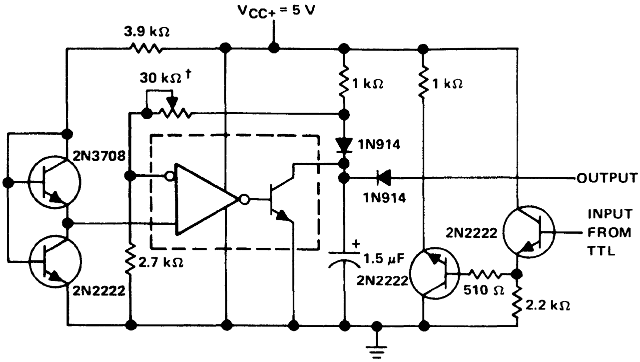


FIGURE 21. ZERO-CROSSING DETECTOR DRIVING MOS LOGIC

TYPICAL APPLICATION DATA



†Adjust to set clamp level.

FIGURE 22. PRECISION SQUARER

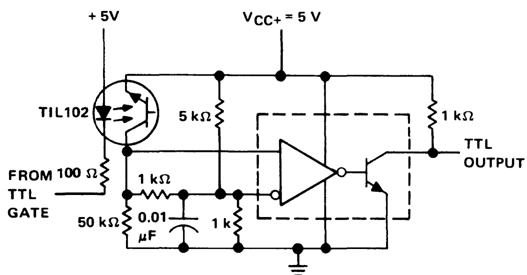


FIGURE 23. DIGITAL TRANSMISSION ISOLATOR

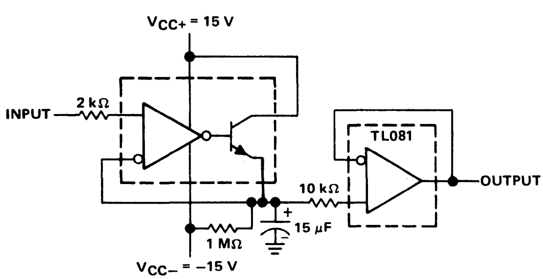


FIGURE 24. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA

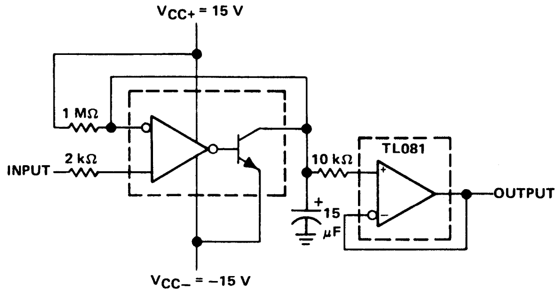
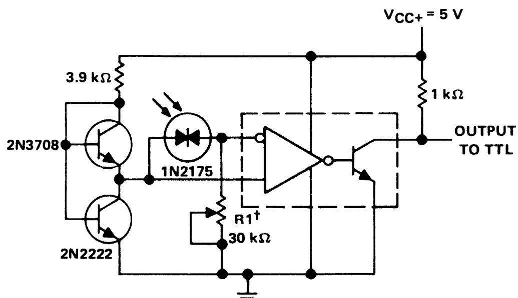
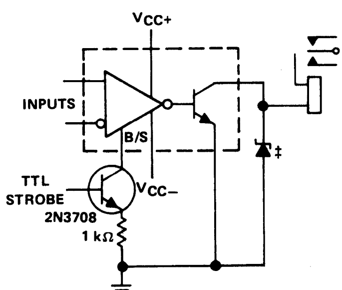


FIGURE 25. NEGATIVE-PEAK DETECTOR



†R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it decreasing dark current by an order of magnitude.

FIGURE 26. PRECISION PHOTODIODE COMPARATOR



‡Transient voltage and inductive kickback protection

FIGURE 27. RELAY DRIVER WITH STROBE

TYPICAL APPLICATION DATA

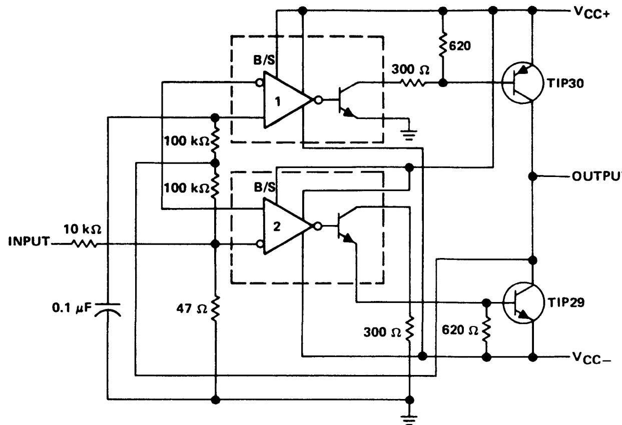


FIGURE 28. SWITCHING POWER AMPLIFIER

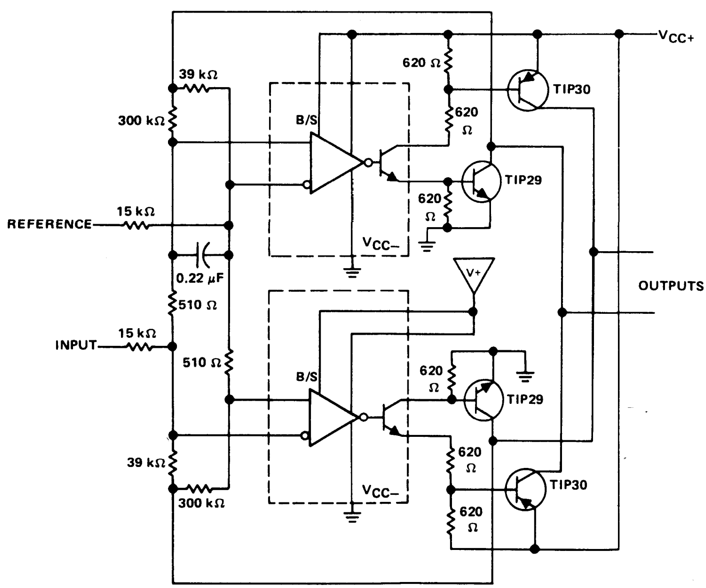


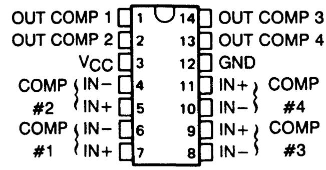
FIGURE 29. SWITCHING POWER AMPLIFIERS

4

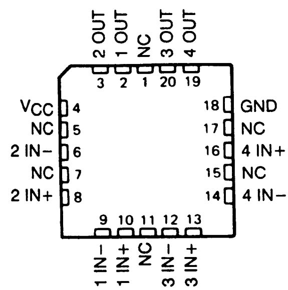
Voltage Comparators

- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage . . . 2 to 36 V**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Low Input Bias Current . . . 25 nA Typ**
- **Low Input Offset Current . . . 3 nA Typ (LM139)**
- **Low Input Offset Voltage . . . 2 mV Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V**
- **Low Output Saturation Voltage**
- **Output Compatible with TTL, MOS, and CMOS**

LM139, LM139A . . . J PACKAGE
ALL OTHERS . . . D, J, OR N PACKAGE
(TOP VIEW)



LM139, LM139A
FK CHIP CARRIER PACKAGE
(TOP VIEW)

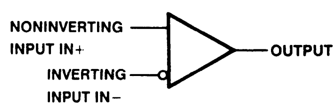


NC – No internal connection

description

These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and pin 3 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

symbol (each comparator)

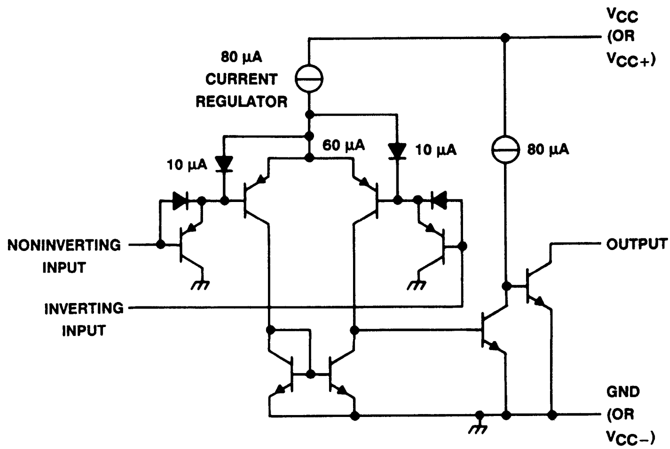


AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE: SMALL OUTLINE (D)	PACKAGE: CERAMIC (FK)	PACKAGE: CERAMIC DIP (J)	PACKAGE: PLASTIC DIP (N)
0°C to 70°C	5 mV	LM339D	–	LM339J	LM339N
	2 mV	LM339AD	–	LM339AJ	LM339AN
−25°C to 85°C	5 mV	LM239D	–	LM239J	LM239N
	2 mV	LM239AD	–	LM239AJ	LM239AN
−40°C to 85°C	7 mV	LM2901ID	–	LM2901IJ	LM2091IN
−55°C to 125°C	5 mV	–	LM139FK	LM139J	–
	2 mV	–	LM139AFK	LM139AJ	–

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM339DR)

schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range: LM139	−55°C to 125°C
LM239, LM239A	−25°C to 85°C
LM339, LM339A	0°C to 70°C
LM2901	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	31°C	608 mW	494 mW	–
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM139, LM139A)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (All others)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	–
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	–

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM139			LM139A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		25°C		2	5		1	2	mV
				−55°C to 125°C			9			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		3	25	nA
				−55°C to 125°C			100			100	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−100		−25	−100	nA
				−55°C to 125°C			−300			−300	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				−55°C to 125°C	0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±7.5 V, V_O = −5 V to 5 V		25°C		200		50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 30 V	−55°C to 125°C			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				−55°C to 125°C			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V, No load		25°C		0.8	2		0.8	2	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 4	100-mV input step with 5-mV overdrive		1.3		μs
		TTL-level input step		0.3		

‡ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM239, LM339			LM239A, LM339A			LM2901			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V	25°C		2	5		1	2		2	7	mV
			Full range			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		5	50		5	50		5	50	nA
			Full range			150			150			200	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−25	−250		−25	−250		−25	−250	nA
			Full range			−400			−400			−500	
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
			Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15\ k\Omega$ to V_{CC}	25°C	50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 5 V	25°C		0.1	50		0.1	50		0.1	50	nA
		V_{ID} = 1 V, V_{OH} = 30 V	Full range			1			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		150	400		150	400		150	500	mV
			Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V, V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V, No load	25°C		0.8	2		0.8	2		0.8	2	mA
		V_{CC} = 30 V, V_O = 15 V, No load									1	2.5	

† Full range (MIN to MAX) for LM239 and LM239A is −25°C to 85°C, for LM339 and LM339A is 0°C to 70°C, and for LM2901 is −40°C to 85°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 4	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

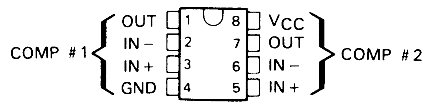
‡ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

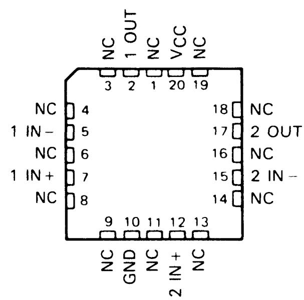
D2232, JUNE 1976—REVISED APRIL 1988

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (LM139)
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

LM193 . . . JG PACKAGE
ALL OTHERS . . . D, JG, OR P PACKAGE
(TOP VIEW)



LM193 . . . FK PACKAGE
(TOP VIEW)

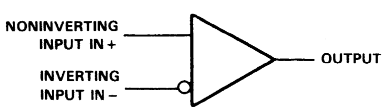


NC—No internal connection

description

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and pin 8 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

symbol (each comparator)

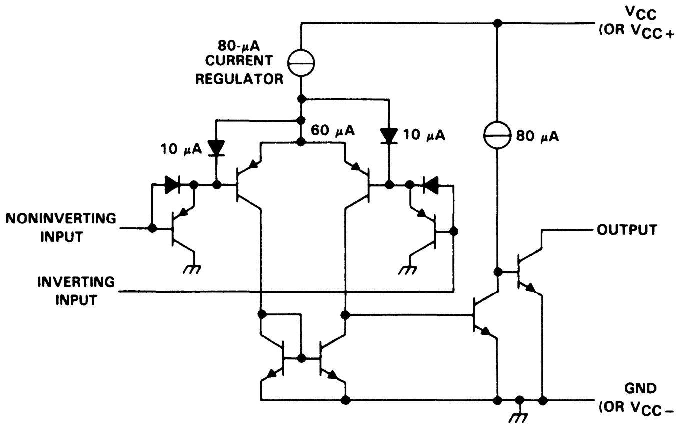


AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX AT T_A = 25°C
DEVICE	PACKAGE SUFFIX		
LM193	FK, JG	−55°C to 125°C	5 mV
LM293	D, JG, P	−25°C to 85°C	5 mV
LM293A	D, JG, P	−25°C to 85°C	2 mV
LM393	D, JG, P	0°C to 70°C	5 mV
LM393A	D, JG, P	0°C to 70°C	2 mV
LM2903	D, JG, P	−40°C to 85°C	7 mV

The D package is available in tape and reel. Add an R suffix when ordering. (e.g., LM393DR)

schematic (each comparator)



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range: LM193	−55°C to 125°C
LM293, LM293A	−25°C to 85°C
LM393, LM393A	0°C to 70°C
LM2903	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	25°C	464 mW	377 mW	–
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
JG (LM193)	900 mW	8.4 mW/°C	43°C	672 mW	546 mW	210 mW
JG (All others)	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	–
P	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	–

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM193			LM293, LM393			LM293A, LM393A			LM2903			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR}, V_O = 1.4 V	25°C		2	5		2	5		1	2		2	7	mV
			Full range			9			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	25		5	50		5	50		5	50	nA
			Full range			100			150			150			200	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		25	100		25	250		25	250		25	250	nA
			Full range			300			400			400			500	
V_{ICR}	Common-mode input voltage range‡		25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq$ 15 kΩ to VCC	25°C	50	200		50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V, V_{ID} = 1 V	25°C		0.1			0.1	50		0.1	50		0.1	50	nA
		V_{OH} = 30 V, V_{ID} = 1 V	Full range			1			1			1			1	μA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, V_{ID} = −1 V,	25°C		150	400		150	400		150	400		150	400	mV
			Full range			700			700			700			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V, V_{ID} = −1 V	25°C	6			6			6			6			mA
I_{CC}	Supply current	$R_L = \infty$, V_{CC} = 5 V	25°C		0.8	1		0.8	1		0.8	1		0.8	1	mA
		$R_L = \infty$, V_{CC} = 30 V	Full range			2.5			2.5			2.5			2.5	

† Full range (MIN to MAX) for LM193 is −55°C to 125°C, for LM293 and LM293A is 25°C to 85°C, for the LM393 and LM393A is 0°C to 70°C, and for LM2903 is −40°C to 85°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

‡ The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} −1.5 V, but either or both inputs can go to 30 V without damage.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,§ See Note 4	100-mV input step with 5-mV overdrive		1.3		μs
		TTL-level input step		0.3		

§ C_L includes probe and jig capacitance.

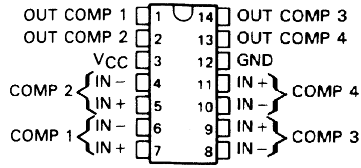
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPE LM3302
QUADRUPLE DIFFERENTIAL COMPARATOR

D2402, OCTOBER 1977—REVISED AUGUST 1983

- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage . . . 2 to 28 Volts**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Low Input Bias Current . . . 25 nA Typ**
- **Low Input Offset Current . . . 3 nA Typ**
- **Low Input Offset Voltage . . . 3 mV Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±28 V**
- **Low Output Saturation Voltage**
- **Output Compatible with TTL, MOS, and CMOS**

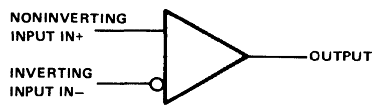
D, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



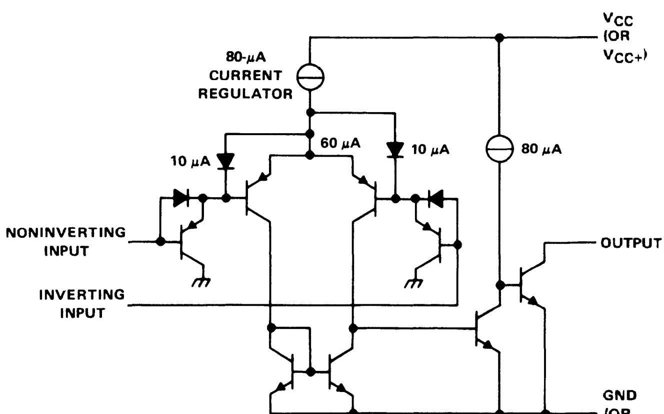
description

This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 volts to 28 volts and pin 3 is at least 1.5 volts more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

symbol (each comparator)



schematic (each comparator)



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	28 V
Differential input voltage (see Note 2)	±28 V
Input voltage range (either input)	−0.3 V to 28 V
Output voltage	28 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	500 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, LM3302 chips are glass-mounted.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 28 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		3	20	mV
			−40°C to 85°C			40	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	100	nA
			−40°C to 85°C			300	
I_{IB}	Input bias current		25°C		−25	−500	nA
			−40°C to 85°C			−1000	
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{CC}-1.5$			V
			−40°C to 85°C	0 to $V_{CC}-2$			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L = 15 kΩ to V_{CC}	25°C	2	30		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 5 V	25°C		0.1		nA
			−40°C to 85°C			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		150	500	mV
			−40°C to 85°C			700	
I_{OL}	Low-level output current	V_{ID} = 1 V, V_{OL} = 1.5 V	25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V, No load	25°C		0.8	2	mA

†All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ to 5 V, C_L = 15 pF‡, See Note 5	100-mV input step with 5 mV overdrive		1.3		μs
		TTL-level input step		0.3		

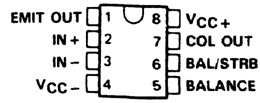
‡C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

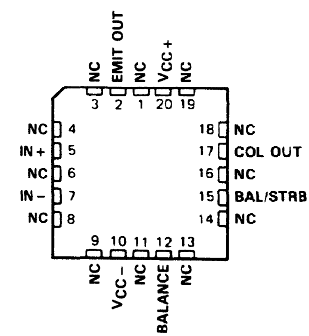
D3019, JUNE 1987

- Low Power Drain — 900 μW Typical with 5-V Supply
- Operates from ±15 V or from a Single Supply as Low as 3 V
- Output Drive Capability of 25 mA
- Emitter Output Can Swing Below Negative Supply
- Response Time — 1.2 μs Typ
- Low Input Currents:
  Offset Current . . . 2 nA Typ
  Bias Current . . . 15 nA Typ
- Wide Common-Mode Input Range:
  −14.5 V to 13.5 V with ±15-V Supply
- Same Pinout as LM111, LM211, LM311
- Designed to be Interchangeable with National Semiconductor LP311

LP111 . . . JG DUAL-IN-LINE PACKAGE
LP211, LP311 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LP111 . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



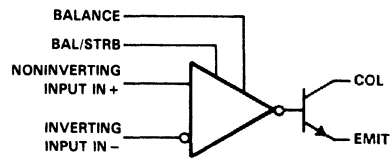
NC – No internal connection

description

The LP111, LP211, and LP311 are a low-power versions of the industry-standard LM111, LM211, and LM311. They take advantage of stable, high-value, ion-implanted resistors to perform the same function as the LM311 series, with a 30:1 reduction in power consumption but only a 6:1 slowdown in response time. Thus, they are well-suited for battery-powered applications and all other applications where fast response times are not needed. They operate over a wide range of supply voltages, from ±18 V down to a single 3-V supply with less than 300 μA current drain, but are still capable of driving a 25-mA load. The LP111, LP211, and LP311 are quite easy to apply free of oscillation if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins.

The LP111 is characterized for operation over the full military temperature range of −55°C to 125°C. The LP211 is characterized for operation from −25°C to 85°C, and the LP311 is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	−18 V
Differential input voltage (see Note 2)	±30 V
Input voltage (either input, see Notes 1 and 3)	±15 V
Voltage from emitter output to V_{CC-}	30 V
Voltage from collector output to V_{CC-}	40 V
Voltage from collector output to emitter output	40 V
Duration of output short-circuit (see Note 4)	40 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5):	
D and P packages	500 mW
FK package	1375 mW
JG package	1050 mW
Operating free-air temperature range: LP111	−55°C to 125°C
LP211	−25°C to 85°C
LP311	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages are at the noninverting input terminal with respect to the inverting terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage of ±15 V, whichever is less.
4. The output may be shorted to ground or to either power supply.
5. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE TA
D	500 mW	5.8 mW/°C	64°C
P	500 mW	8.0 mW/°C	87°C
FK	1375 mW	11.0 mW/°C	25°C
JG	1050 mW	8.4 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNITS
Input voltage ($\|V_{CC\pm}\| \leq 15$ V)	V_{CC-} +0.5		V_{CC+} −1.5	V
Supply voltage, $V_{CC+} - V_{CC-}$	3.5		30	V

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{ID}	Input offset voltage	RS < 100 kΩ, See Note 6	25°C			2	7.5	mV
			Full Range				10	
I_{IO}	Input offset current	See Note 6	25°C			2	25	nA
			Full Range				35	
I_{IB}	Input bias current		25°C			15	100	nA
			Full Range				150	
V_{OL}	Low-level output voltage	$V_{ID} > 10$ mV, $I_{OL} = 25$ mA, See Note 7	25°C			0.4	1.5	V
		$V_{CC} = 4.5$ V, $V_{CC-} = 0$, $V_{ID} < -10$ mV, $I_{OL} = 1.6$ mA, See Note 7	Full Range	LP111		0.1	0.7	
				LP211, LP311		0.1	0.4	
	Low-level strobe current	$V_{(strobe)} = 0.3$ V, $V_{ID} < -10$ mV, See Note 8	25°C			100	300	μA
$I_{O(off)}$	Output off-state current	$V_{ID} > 10$ mV, $V_{CE} = 35$ V	25°C			0.2	100	nA
A_{VD}	Large signal differential voltage amplification	$R_L = 5$ kΩ	25°C		40	100		V/mV
I_{CC+}	Supply current from V_{CC+}	$V_{ID} = -50$ mV, $R_L = \infty$	Full Range			150	300	μA
I_{CC-}	Supply current from V_{CC-}	$V_{ID} = 50$ mV, $R_L = \infty$	Full Range			−80	−180	μA

†All typical values are at $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$.

NOTES: 6. The offset voltages and offset currents given are the maximum values required to drive the output within 1 V of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.
7. Voltages are with respect to EMIT OUT and V_{CC-} tied together.
8. The strobe should not be shorted to ground; it should be current driven at 100 μA to 300 μA.

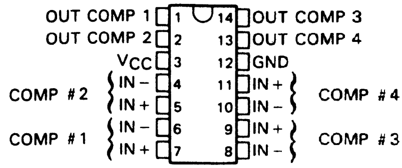
switching characteristics at $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETAER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	See Note 9		1.2		μs

NOTE 9: The response time is specified for a 100-mV input step with 5-mV overdrive.

- **Ultralow Power Supply Current Drain . . . Typically 60 μA**
- **Low Input Biasing Current . . . 3 nA**
- **Low Input Offset Current . . . ±0.5 nA**
- **Low Input Offset Voltage . . . ±2 mV**
- **Common-Mode Input Voltage Includes Ground**
- **Output Voltage Compatible with MOS and CMOS Logic**
- **High Output Sink-Current Capability (30 mA at V_O = 2 V)**
- **Power Supply Input Reverse-Voltage Protected**
- **Single-Power-Supply Operation**
- **Pin-for-Pin Compatible with LM239, LM339, LM2901**

LP239, LP339, LP2901
D, J, OR N PACKAGE
(TOP VIEW)



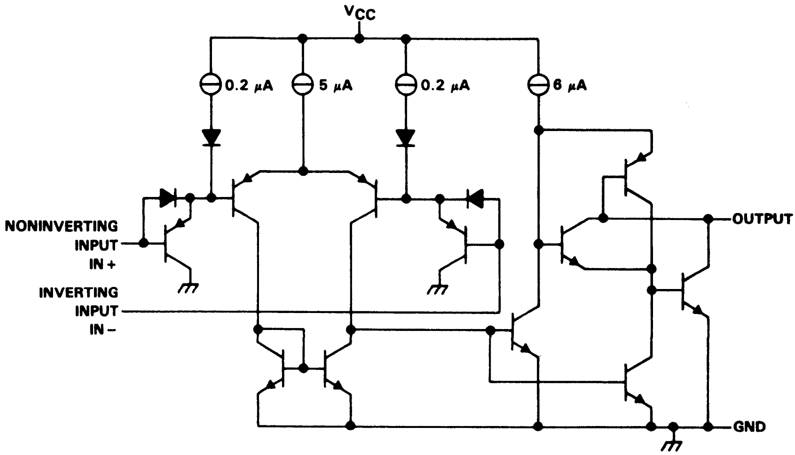
description

The LP239, LP339, and LP2901 are low-power quadruple differential comparators. Each device consists of four independent voltage comparators designed specifically to operate from a single power supply and typically to draw 60 μA of drain current over a wide range of voltages. Operation from split power supplies is also possible and the ultralow power supply drain current is independent of the power supply voltage.

Applications include limit comparators, simple analog-to-digital converters, pulse generators, squarewave generators, time delay generators, voltage controlled oscillators, multivibrators, and high-voltage logic gates. The LP239, LP339, and LP2901 were specifically designed to interface with the CMOS logic family. The ultralow power supply current makes these products desirable in battery-powered applications.

The LP239 is characterized for operation from −25°C to 85°C. The LP339 is characterized for operation from 0°C to 70°C. The LP2901 is characterized for operation from −40°C to 85°C.

schematic diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage, V_{ID} (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Input current, $V_I \leq -0.3$ V (see Note 3)	−50 mA
Duration of output short-circuit to ground (see Note 4)	unlimited
Continuous total dissipation (see Note 5)	See Dissipation Rating Table
Operating free-air temperature range: LP239	−25°C to 85°C
LP339	0°C to 70°C
LP2901	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. This input current only exists when the voltage at any of the inputs is driven negative. The current flows through the collector-base junction of the input clamping device. In addition to the clamping device action, there is lateral n-p-n parasitic transistor action. This action is not destructive and normal output states are re-established when the input voltage returns to a value more positive than −0.3 V at T_A = 25°C.
4. Short circuits between outputs to V_{CC} can cause excessive heating and eventual destruction.
5. If the output transistors are allowed to staturate, the low bias dissipation and the on-off characteristics of the outputs keep the dissipation very small (usually less than 100 mW).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	ABOVE T_A = 25°C See Note 6	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

4 Voltage Comparators

TEXAS INSTRUMENTS

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 2 V, RS = 0, See Note 6		25°C		±2	±5	mV
				Full range			±9	
I_{IO}	Input offset current			25°C		±0.5	±5	nA
				Full range		±1	±15	
I_{IB}	Input bias current	See Note 7		25°C		−2.5	−25	nA
				Full range		−4	−40	
V_{ICR}	Common-mode input voltage range	Single supply		25°C	0 to $V_{CC}-1.5$			V
				Full range	0 to $V_{CC}-2$			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, R_L = 15 kΩ				500		V/mV
	Output sink current	V_{I-} = 1 V, V_{I+} = 0	V_O = 2 V (see Note 8)	25°C	20	30		mA
				Full range	15			
			V_O = 0.4 V	25°C	0.2	0.7		
	Output leakage current	V_{I+} = 1 V, V_{I-} = 0	V_O = 5 V	25°C		0.1		nA
			V_O = 30 V	Full range			1	μA
V_{ID}	Differential input voltage	$V_I \leq 0$ (or V_{CC-} on split supplies)					36	V
I_{CC}	Supply current	$R_L = \infty$ all comparators				60	100	μA

NOTES: 6. V_{IO} is measured over the full common-mode input voltage range.
7. Because of the p-n-p input stage, the direction of the current is out of the device. This current is essentially constant (i.e., independent of the output state). Therefore, no loading change exists on the reference or input lines as long as the common-mode input voltage range is not exceeded.
8. The output sink current is a function of the output voltage. These devices have a bimodal output section that allows them to sink (via a Darlington connection) large currents at output voltages greater than 1.5 V and smaller currents at output voltages less than 1.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L connected to 5 V through 5.1 kΩ

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Large-signal response time	TTL logic swing, V_{ref} = 1.4 V		1.3		μs
Response time			8		μs

TYPICAL APPLICATION DATA

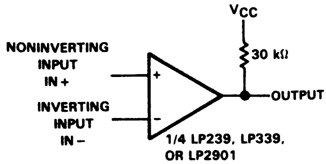


FIGURE 1. BASIC COMPARATOR

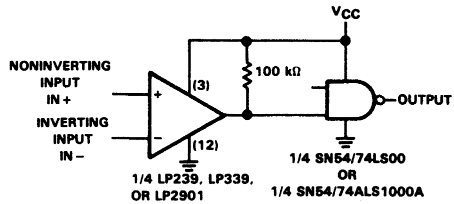


FIGURE 2. CMOS DRIVER

All pins of any unused comparators should be grounded. The bias network of the LP239, LP339, and LP2901 establishes a drain current that is independent of the magnitude of the power supply voltage over the range of 2 V to 30 V. It is usually necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative by more than −0.3 V. The output section has two distinct modes of operation: a Darlington mode and a grounded-emitter mode. This unique drive circuit permits the device to sink 30 mA at V_O = 2 V in the Darlington mode and 700 μA at V_O = 0.4 V in the ground-emitter mode. Figure 3 is a simplified schematic diagram of the output section. The output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough (above 1 V, Q1 is not saturated and the output current is limited only by the product of the h_{FE} of Q1, the h_{FE} of Q2, and I1 and by the 60-Ω saturation resistance of Q2. The devices are capable of driving LEDs, relays, etc., in this mode while maintaining an ultralow power supply current of 60 μA typically.

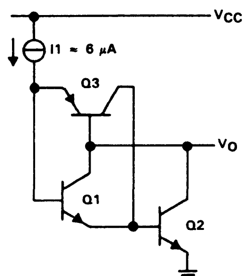


FIGURE 3. OUTPUT SECTION SCHEMATIC DIAGRAM

Without transistor Q3, if the output voltage were allowed to drop below 0.8 V, transistor Q1 would saturate and the output current would drop to zero. The circuit would be unable to pull low current loads down to ground or the negative supply, if used. Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the h_{FE} of Q2 (700 μA at V_O = 0.4 V). The output of the devices exhibit a bimodal characteristic with a smooth transition between modes.

In both cases, the output is an uncommitted collector. Therefore several outputs can be tied together to provide a dot logic function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range, and there is no restriction on this voltage based on the magnitude of the voltage that is applied to the V_{CC} terminal of the package.

MAY 1987

FEATURES

- Pin-Compatible with LM111 Series Devices
- Max. 0.5mV Input Offset Voltage
- Max. 25nA Input Bias Current
- Max. 3nA Input Offset Current
- Max. 250ns Response Time
- Min. 200,000 Voltage Gain
- 50mA Output Current Source or Sink
- ±30V Differential Input Voltage
- Fully Specified for Single +5V Operation

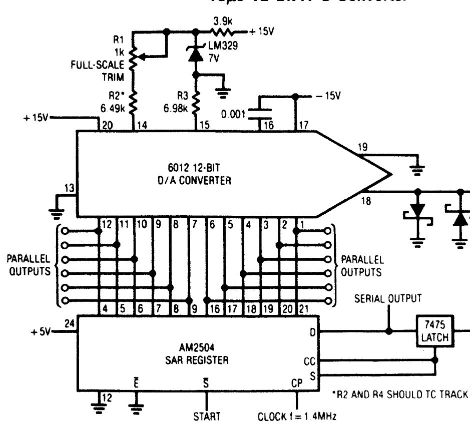
APPLICATIONS

- SAR A to D Converters
- Voltage to Frequency Converters
- Precision R/C Oscillator
- Peak Detector
- Motor Speed Control
- Pulse Generator
- Relay/Lamp Driver

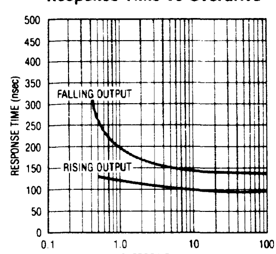
DESCRIPTION

The LT1011 is a general purpose comparator with significantly better input characteristics than the LM111. Although pin-compatible with the LM111, it offers four times lower bias current, six times lower offset voltage, and five times higher voltage gain. Offset voltage drift—a previously unspecified parameter—is 15μV/°C. Additionally, the supply current is lower by a factor of two with no loss in speed. The LT1011 is several times faster than the LM111 when subjected to large overdrive conditions. It is also fully specified for DC parameters and response time when operating on a single +5V supply. These parametric improvements allow the LT1011 to be used in high accuracy (≥ 12-bit) systems without trimming. In a 12-bit A to D application, for instance, using a 2mA DAC, the offset error introduced by the LT1011 is less than 1/2 LSB. The LT1011 retains all the versatile features of the LM111, including single 3V to ± 18V supply operation, and a floating transistor output with 50mA source/sink capability. It can drive loads referenced to ground, negative supply or positive supply, and is specified up to 50V between V⁻ and the collector output. A differential input voltage up to the full supply voltage is allowed, even with ± 18V supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

10μs 12-Bit A-D Converter



Response Time vs Overdrive



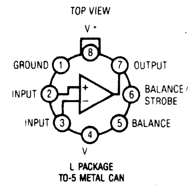
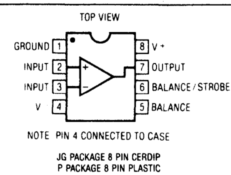
ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

TEXAS INSTRUMENTS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 8 to pin 4) 36V
Output to Negative Supply (pin 7 to pin 4)
  LT1011AM, LT1011M 50V
  LT1011AC, LT1011C 40V
Ground to Negative Supply
  (pin 1 to pin 4) 30V
Differential Input Voltage .... ±36V
Voltage at Strobe Pin (pin 6 to pin 8) 5V
Input Voltage (Note 1) .... Equal to Supplies
Output Short Circuit Duration .... 10 sec.
Operating Temperature Range (Note 2)
  LT1011AM/LT1011M .... −55°C to 125°C
  LT1011AC/LT1011C .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)........ 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1011AML LT1011ML LT1011ACL LT1011CL
	LT1011AMJG LT1011MJG LT1011ACJG LT1011CJG LT1011ACP LT1011CP

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $R_S = 0$, $T_J = 25°C$, $V_I = -15V$, output at pin 7 unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1011AM/LT1011AC MIN	TYP	MAX	LT1011M/LT1011C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Note 3			0.3	0.5		0.6	1.5	mV
			●			1.0			3.0	mV
V_{OS}	Input Offset Voltage	$R_S \le 50k\Omega$ (Note 4)				0.75			2.0	mV
			●			1.5			3.0	mV
I_{OS}	Input Offset Current	Note 4			0.2	3		0.2	4	nA
			●			5			6	nA
I_b	Input Bias Current	Note 3			15	25		20	50	nA
I_b	Input Bias Current	Note 4			20	35		25	65	nA
			●			50			80	nA
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 5)	$T_{MIN} \le T \le T_{MAX}$	●		4	15		4	25	μV/°C
A_{VOL}	Large Signal Voltage Gain	$R_L = 1k\Omega$ to +15V, $-10V \le V_{OUT} \le 14.5V$		200	500		200	500		V/mV
		$R_L = 500\Omega$ to +5V, $0.5V \le V_{OUT} \le 4.5V$		50	300		50	300		V/mV
CMRR	Common-Mode Rejection Ratio			94	115		90	115		dB
	Input Voltage Range (Note 8)	$V_S = \pm15V$	●	−14.5		13	−14.5		13	V
		V_S = Single +5V	●	0.5		3.0	0.5		3.0	V
T_d	Response Time	Note 6			150	250		150	250	ns
V_{OL}	Output Saturation Voltage	$V_{IN} = 5$ mV, $I_{SINK} = 8$mA	●		0.25	0.4		0.25	0.4	V
		$V_I = 0$, $I_{SINK} = 50$ mA	●		0.7	1.5		0.7	1.5	V
	Output Leakage Current	$V_{IN} = 5$mV, $V1 = -15V$			0.2	10		0.2	10	nA
		$V_{OUT} = 35V$ (25V for LT1011C)	●			500			500	nA
	Positive Supply Current				3.2	4.0		3.2	4.0	mA
	Negative Supply Current				1.7	2.5		1.7	2.5	mA
	Strobe Current	Minimum to Ensure Output Transistor is Off		500			500			μA
	Input Capacitance				6			6		pF

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection in applications section.

Note 2: T_J max = 150°C for the LT1011AM/LT1011M and 95°C for the LT1011AC/LT1011C.

Note 3: Output is sinking 1.5mA with $V_{OUT} = 0V$.

Note 4: These specifications apply for all supply voltages from a single +5V to ±15V, the entire input voltage range, and for both high and low output states. The high state is $I_{SINK} \geq 100\mu A$, $V_{OUT} \geq (V^+ - 1V)$ and the low state is $I_{SINK} \leq 8mA$, $V_{OUT} \leq 0.8V$. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

Note 5: Drift is calculated by dividing the offset voltage difference measured at min and max temperatures by the temperature difference.

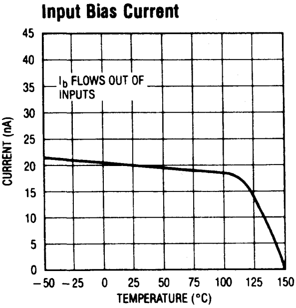
Note 6: Response time is measured with a 100mV step and 5mV overdrive. The output load is a 500Ω resistor tied to +5V. Time measurement is taken when the output crosses 1.4V.

Note 7: Do not short the strobe pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500μA will strobe the LT111A if speed is not important. External leakage on the strobe pin in excess of 0.2μA when the strobe is "off" can cause offset voltage shifts.

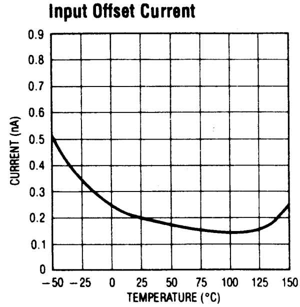
Note 8: See graph, Input Offset Voltage vs Common-Mode Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

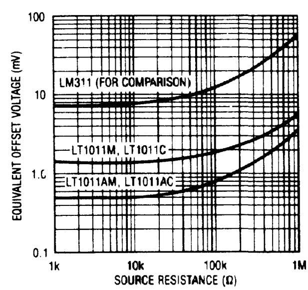
Input Bias Current



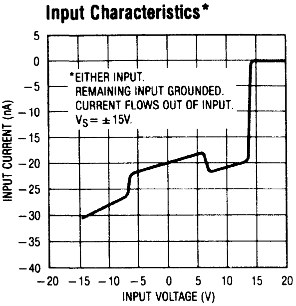
Input Offset Current



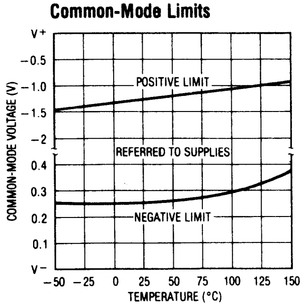
Worst-Case Offset Error



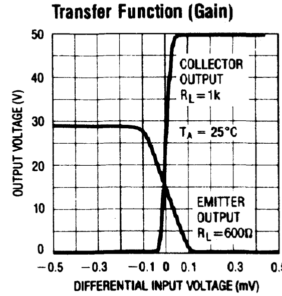
Input Characteristics*



Common-Mode Limits

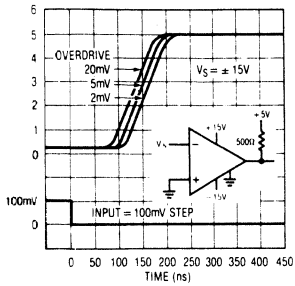


Transfer Function (Gain)

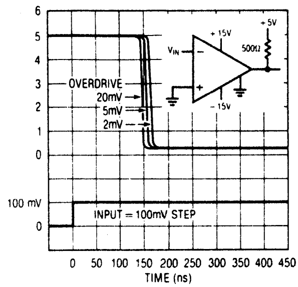


TYPICAL PERFORMANCE CHARACTERISTICS

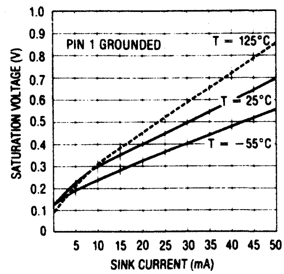
Response Time—Collector Output



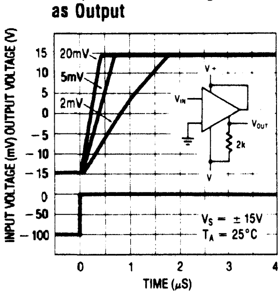
Response Time—Collector Output



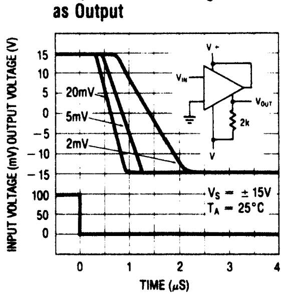
Collector Output Saturation Voltage



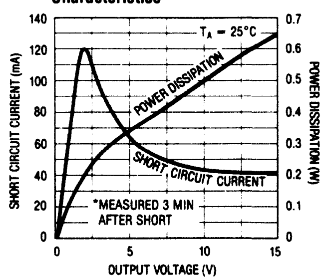
Response Time Using GND Pin as Output



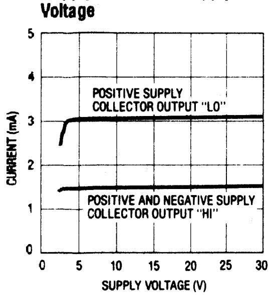
Response Time Using GND Pin as Output



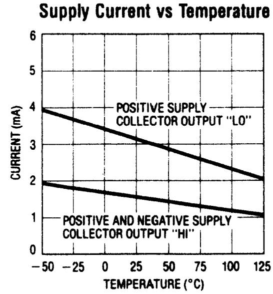
Output Limiting Characteristics*



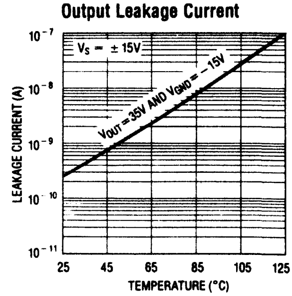
Supply Current vs Supply Voltage



Supply Current vs Temperature

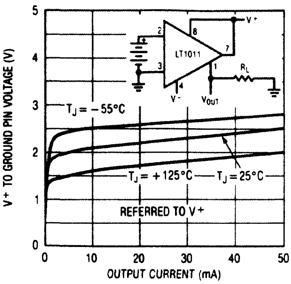


Output Leakage Current

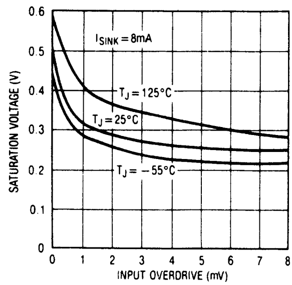


TYPICAL PERFORMANCE CHARACTERISTICS

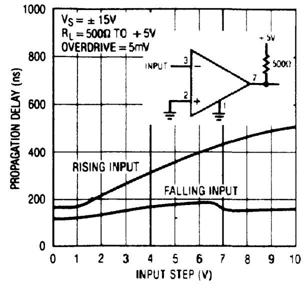
Output Saturation—Ground Output



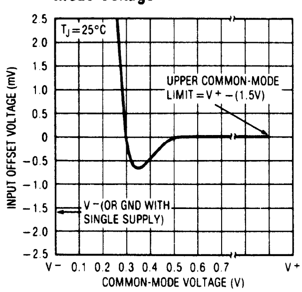
Output Saturation Voltage



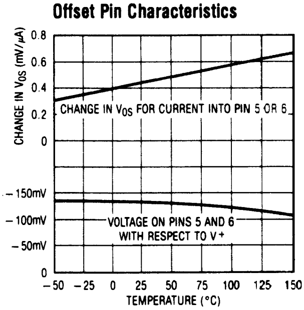
Response Time vs Input Step Size



Input Offset Voltage vs Common-Mode Voltage



Offset Pin Characteristics



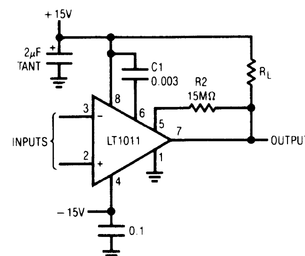
APPLICATIONS INFORMATION

Preventing Oscillation Problems

Oscillation problems in comparators are nearly always caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true with high gain-bandwidth comparators like the LT1011, which are designed for fast switching with millivolt input signal levels. The gain-bandwidth product of the LT1011 is over 10GHz. Oscillation problems tend to occur at frequencies around 5MHz, where the LT1011 has a gain of ≈2000. This implies that attenuation of output signals must be at least 2000:1 at 5MHz as measured at the inputs. If the source impedance is 1kΩ, the effective stray capacitance between output and input must have a reactance of more than (2000) (1kΩ) = 2MΩ, or less than 0.02pF. The actual interlead capacitance between input and output pins on the LT1011 is less than 0.002pF when cut to printed circuit mount length. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding. Additional steps to ensure oscillation-free operation are:

1. Bypass the strobe/balance pins with a 0.01μF capacitor connected from pin 5 to pin 6. This eliminates stray capacitive feedback from the output to the balance pins, which are nearly as sensitive as the inputs.
2. Bypass the negative supply (pin 4) with a 0.1μF ceramic capacitor close to the comparator. 0.1μF can also be used for the positive supply (pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to pin 8, use a 2μF solid tantalum bypass capacitor.
3. Bypass any slow moving or DC input with a capacitor (≥0.01μF) close to the comparator to reduce high frequency source impedance.
4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input to balance source impedances for DC accuracy, bypass it with a capacitor. The low input bias current of the LT1011 usually eliminates any need for source resistance balancing. A 5kΩ imbalance, for instance, will create only 0.25mV DC offset.
5. Use hysteresis. This consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either AC or DC. AC techniques do not shift the apparent offset voltage of the comparator, but require a *minimum* input signal slew rate to be effective. DC hysteresis works for all input slew rates, but creates a shift in offset voltage dependent on the previous condition of the input signal. The circuit shown below is an excellent compromise between AC and DC hysteresis.

Comparator with Hysteresis

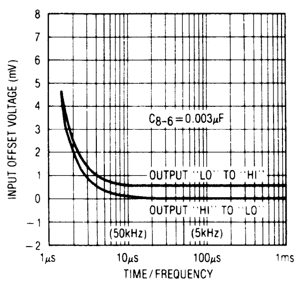


This circuit is especially useful for general purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the balance pins to provide extremely fast, clean output switching even with low frequency input signals in the millivolt range. The 0.003μF capacitor from pin 6 to pin 8 generates AC hysteresis because the voltage on the balance pins shifts slightly, depending on the state of the output. Both pins move about 4mV. If one pin (6) is bypassed, AC hysteresis is created. It is only a few millivolts referred to the inputs, but is sufficient to switch the output at nearly the maximum speed of which the comparator is capable. To prevent

APPLICATIONS INFORMATION

problems from low values of input slew rate, a slight amount of DC hysteresis is also used. The sensitivity of the balance pins to current is about 0.5mV input referred offset for each microampere of balance pin current. The 15mΩ resistor tied from output to pin 5 generates 0.5mV DC hysteresis. The combination of AC and DC hysteresis creates clean oscillation-free switching with very small input errors. The curve below plots input referred error versus switching frequency for the circuit as shown.

Input Offset Voltage vs Time to Last Transition

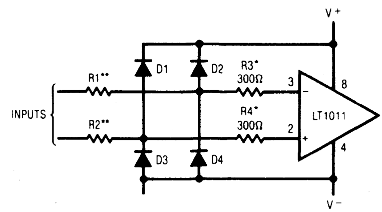


Note that at low frequencies, the error is simply the DC hysteresis, while at high frequencies, an additional error is created by the AC hysteresis. The high frequency error can be reduced by reducing C_H, but lower values may not provide clean switching with very low slew rate input signals.

Input Protection

The inputs to the LT1011 are particularly suited to general purpose comparator applications because large differential and/or common-mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40V above the negative supply, *independent of the positive supply voltage*. Internal forward biased diodes will conduct when the inputs are taken below the negative supply. In this condition, input current must be limited to 1mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used (see drawing below).

Limiting Fault Input Currents



D1-D4 1N4148
*MAY BE ELIMINATED FOR $I_{FAULT} \le 1mA$
**SELECT ACCORDING TO ALLOWABLE FAULT CURRENT AND POWER DISSIPATION

The input resistors should limit fault current to a reasonable value (0.1mA to 20mA). Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. And one final caution: lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1–D4.

R3 and R4 limit input current to the LT1011 to less than 1mA when the input signals are held below V^-. They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1mA.

Input Slew Rate Limitations

The response time of a comparator is typically measured with a 100mV step and a 5mV–10mV overdrive. Unfortunately, this does not simulate many real-world situations where the step size is typically much larger and overdrive can be significantly less. In the case of the LT1011, step size is important because the slew rate of internal nodes will limit response time for input step sizes larger than 1V. At 5V step size, for instance, response time increases from 150ns to 360ns. See the curve labeled Response Time vs Input Step Size for more detail.

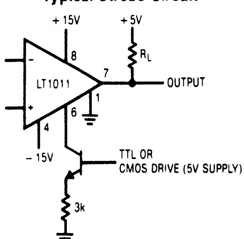
APPLICATIONS INFORMATION

If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. Maximum suggested common-mode slew rate is 10V/μs.

Strobing

The LT1011 can be strobed by pulling current out of the strobe pin. The output transistor is forced to an "off" state, giving a "hi" output at the collector (pin 7). Currents as low as 250μA will cause strobing, but at low strobe currents strobe delay will be 200ns–300ns. If strobe current is increased to 3mA, strobe delay drops to about 60ns. The voltage at the strobe pin is about 150mV below V^+ at zero strobe current and about 2V below V^+ for 3mA strobe current. *Do not ground the strobe pin. It must be current driven.* The drawing below shows a typical strobe circuit.

Typical Strobe Circuit



Note that there is no bypass capacitor between pins 5 and 6. This maximizes strobe speed, but leaves the comparator more sensitive to oscillation problems for slow, low level inputs. A 1pF capacitor between the output and pin 5 will greatly reduce oscillation problems without reducing strobe speed.

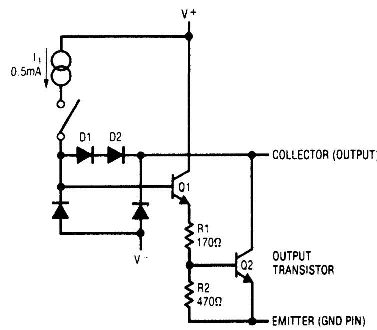
DC hysteresis can also be added by placing a resistor from output to pin 5. See step number 5 under "Preventing Oscillation Problems".

The pin (6) used for strobing is also one of the offset adjust pins. Current flow into or out of pin 6 must be kept very low (<0.2μA) when not strobing to prevent input offset voltage shifts.

Output Transistor

The LT1011 output transistor is truly floating in the sense that no current flows into or out of either the collector or emitter when the transistor is in the "off" state. The equivalent circuit is shown in the drawing below.

Output Transistor Circuitry



In the "off" state, I_1 is switched off and both Q1 and Q2 turn off. The collector of Q2 can be now held at any voltage above V^- without conducting current, including voltages above the positive supply level. Maximum voltage above V^- is 50V for the LT1011 and 40V for the LT1011C. The emitter can be held at any voltage between V^+ and V^- as long as it is negative with respect to the collector.

In the "on" state, I_1 is connected, turning on Q1 and Q2. Diodes D1 and D2 prevent deep saturation of Q2 to improve speed and also limit the drive current of Q1. The R1/R2 divider sets the saturation voltage of Q2 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between V^+ and V^-. This allows the remaining pin to drive the load. In typical applications, the emitter is connected to V^- or ground and the collector drives a load tied to V^+ or a separate positive supply.

APPLICATIONS INFORMATION

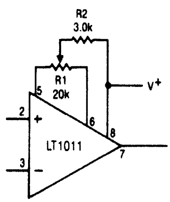
When the emitter is used as the output, the collector is typically tied to V^+ and the load is connected to ground or V^-. Note that the emitter output is phase reversed with respect to the collector output so that the "+" and "−" input designations must be reversed. When the collector is tied to V^+, the voltage at the emitter in the "on" state is about 2V below V^+ (see curves).

Input Signal Range

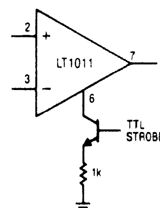
The common-mode input voltage range of the LT1011 is about 300mV above the negative supply and 1.5V below the positive supply, independent of the actual supply voltages (see curve in typical performance characteristics). This is the voltage range over which the output will respond correctly when the common-mode voltage is applied to one input and a higher or lower signal is applied to the remaining input. *If one input is inside the common-mode range and one is outside, the output will be correct. If the inputs are outside the common-mode range in opposite directions, the output will still be correct. If both inputs are outside the common-mode range in the same direction, the output will not respond to the differential input; it will remain unconditionally high* (collector output).

TYPICAL APPLICATIONS

Offset Balancing

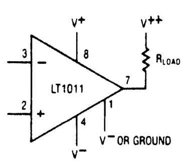


Strobing



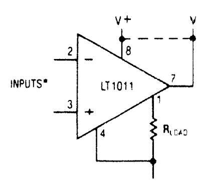
NOTE: DO NOT GROUND STROBE PIN.

Driving Load Referenced to Positive Supply



V^{++} CAN BE GREATER OR LESS THAN V^+

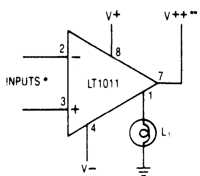
Driving Load Referenced to Negative Supply



* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

TYPICAL APPLICATIONS

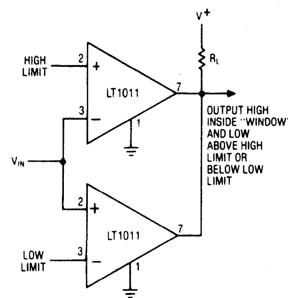
Driving Ground Referred Load



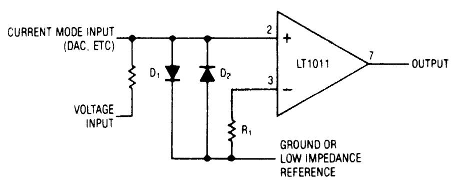
* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

**V++ MAY BE ANY VOLTAGE ABOVE V−. PIN 1 SWINGS TO WITHIN ≈2V OF V++

Window Detector

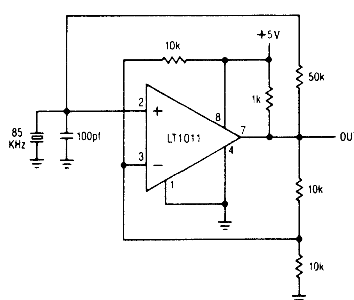


Using Clamp Diodes to Improve Frequency Response*



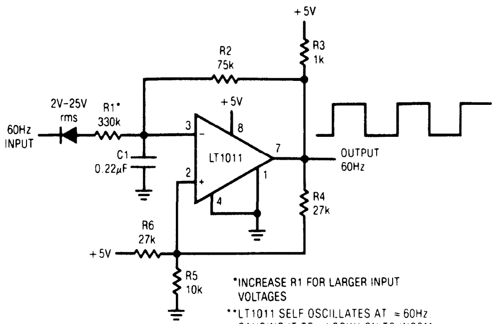
*SEE CURVE, "RESPONSE TIME VS INPUT STEP SIZE"

Crystal Oscillator



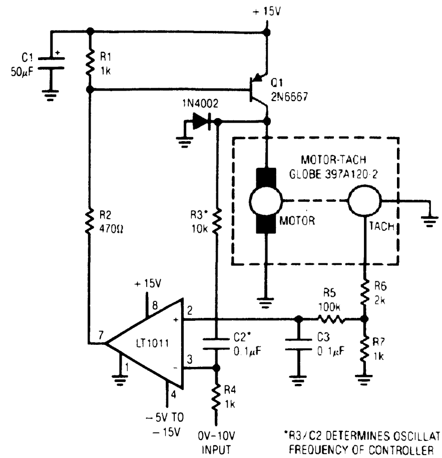
TYPICAL APPLICATIONS

Noise Immune 60Hz Line Sync**



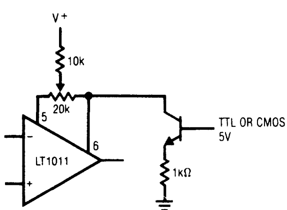
*INCREASE R1 FOR LARGER INPUT VOLTAGES
**LT1011 SELF OSCILLATES AT ≈ 60Hz CAUSING IT TO "LOCK" ON TO INCOMING LINE SIGNAL

High Efficiency**Motor Speed Controller

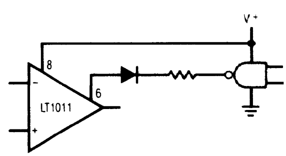


*R3/C2 DETERMINES OSCILLATION FREQUENCY OF CONTROLLER
**Q1 OPERATES IN SWITCH MODE

Combining Offset Adjust and Strobe

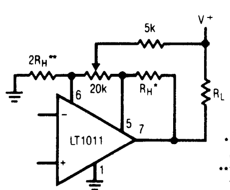


Direct Strobe Drive when CMOS* Logic Uses Same V+ Supply as LT1011



*NOT APPLICABLE FOR TTL LOGIC

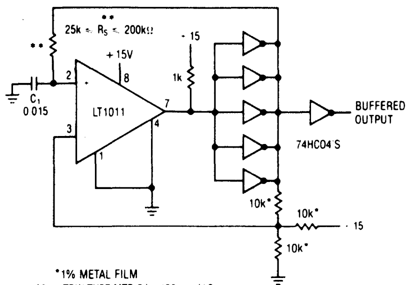
Combining Offset Adjustment and Hysteresis



*HYSTERESIS IS ≈ 0.45mV/μA OF CURRENT CHANGE IN R_H
**THIS RESISTOR CAUSES HYSTERESIS TO BE CENTERED AROUND V_{OS}

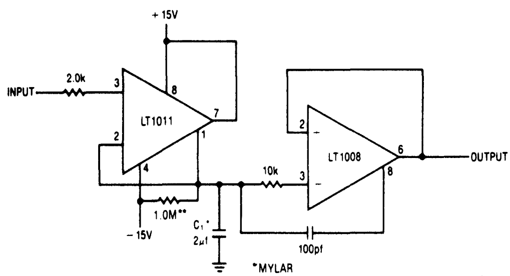
TYPICAL APPLICATIONS

Low Drift R/C Oscillator†



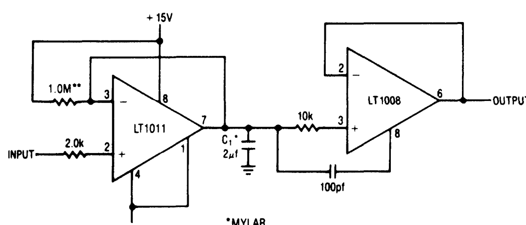
*1% METAL FILM
** = TRW TYPE MTR-5/ + 120ppm/°C
C_1 = .015 = POLYSTYRENE − 120ppm/°C ± 30ppm WESCO TYPE 32-P
NOTE: COMPARATOR CONTRIBUTES ≤ 10ppm/°C DRIFT FOR FREQUENCIES BELOW 10kHz.
†LOW DRIFT AND ACCURATE FREQUENCY ARE OBTAINED BECAUSE THIS CONFIGURATION REJECTS EFFECTS DUE TO INPUT OFFSET VOLTAGE AND BIAS CURRENT OF THE COMPARATOR.

Positive Peak Detector



*MYLAR
**SELECT FOR REQUIRED RESET TIME CONSTANT

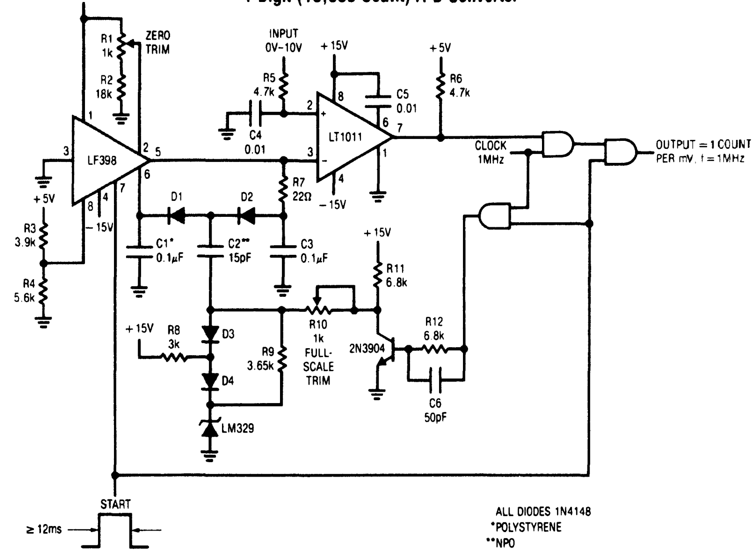
Negative Peak Detector



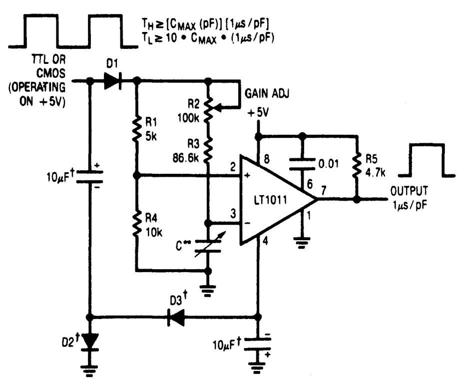
*MYLAR
**SELECT FOR REQUIRED RESET TIME CONSTANT

TYPICAL APPLICATIONS

4-Digit (10,000 Count) A-D Converter



Capacitance to Pulse Width Converter



*PW = (R2 + R3) (C) $\left(\frac{R1 + R4}{R1}\right)$. INPUT CAPACITANCE OF LT1011 IS ≈ 6pF. THIS IS AN OFFSET TERM.

†THESE COMPONENTS MAY BE ELIMINATED IF NEGATIVE SUPPLY IS AVAILABLE (–1V TO –15V).

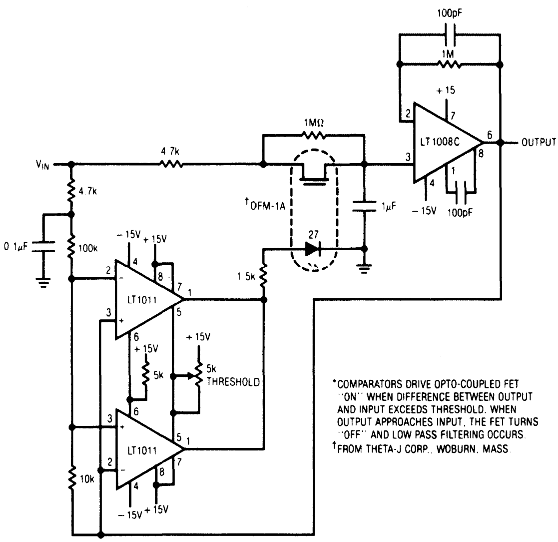
**TYPICAL 2 SECTIONS OF 365pF VARIABLE CAPACITOR WHEN USED AS SHAFT ANGLE INDICATION.

4

Voltage Comparators

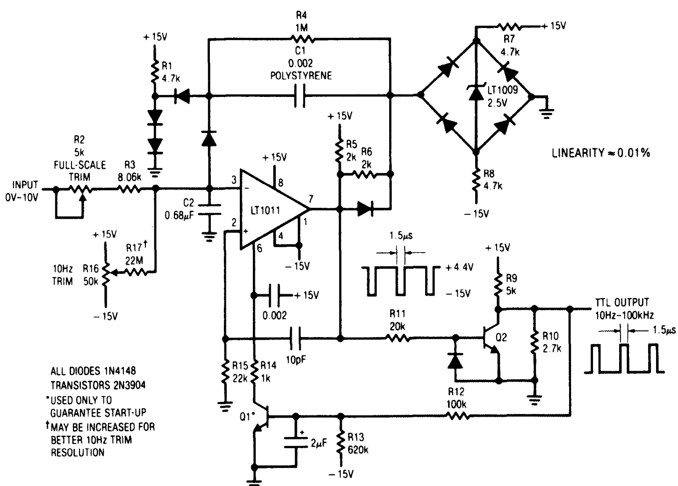
TYPICAL APPLICATIONS

Fast Settling* Filter



*COMPARATORS DRIVE OPTO-COUPLED FET "ON" WHEN DIFFERENCE BETWEEN OUTPUT AND INPUT EXCEEDS THRESHOLD. WHEN OUTPUT APPROACHES INPUT, THE FET TURNS "OFF" AND LOW PASS FILTERING OCCURS.
†FROM THETA-J CORP., WOBURN, MASS.

10Hz to 100kHz Voltage to Frequency Converter

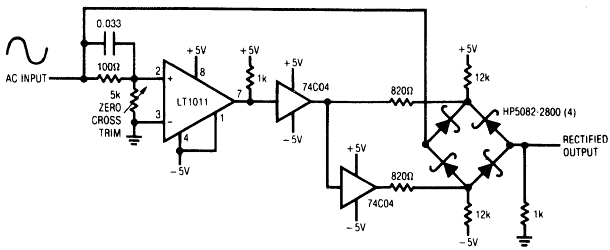


ALL DIODES 1N4148
TRANSISTORS 2N3904
*USED ONLY TO GUARANTEE START-UP
†MAY BE INCREASED FOR BETTER 10Hz TRIM RESOLUTION

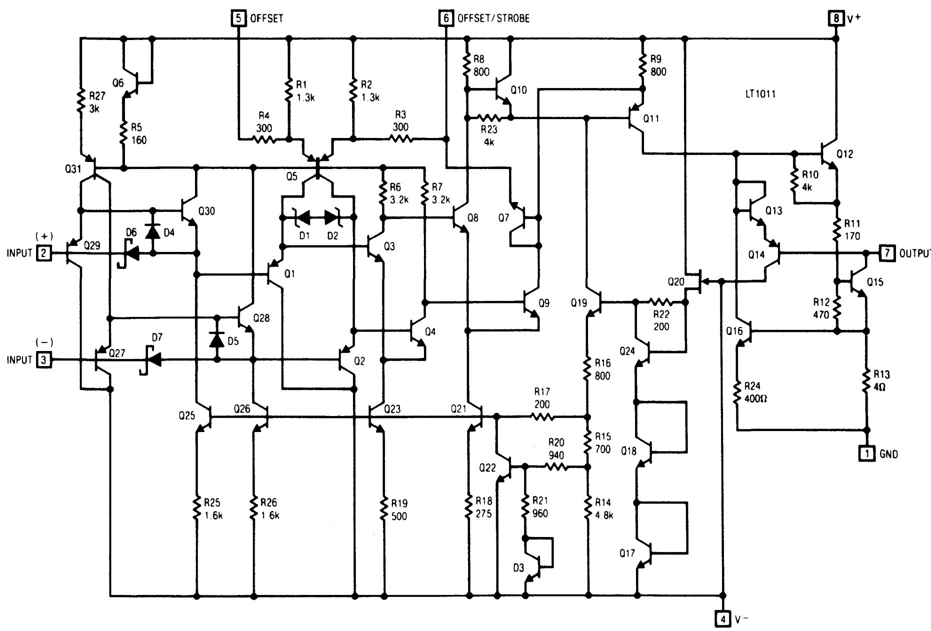
TEXAS INSTRUMENTS

TYPICAL APPLICATIONS

100kHz Precision Rectifier

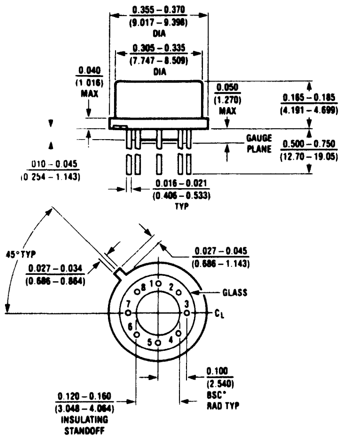


SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

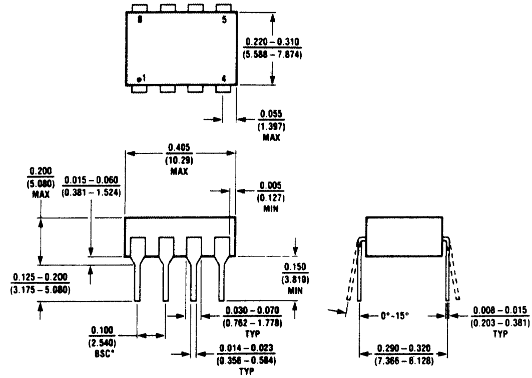
L Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T_jmax	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

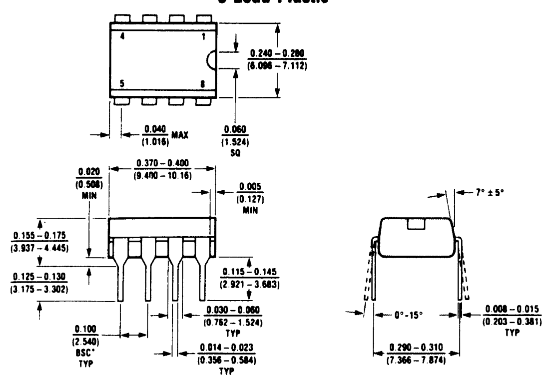
JG Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_jmax	θ_{ja}
150°C	100°C/W

P Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_jmax	θ_{ja}
100°C	130°C/W

MAY 1988

FEATURES

- Ultra Fast (10ns typ)
- Operates Off **Single** +5V Supply, or ±5V
- Complementary Output to TTL
- Low Offset Voltage
- No Minimum Input Slew Rate Requirement
- No Power Supply Current Spiking
- Output Latch Capability

APPLICATIONS

- High Speed A to D Converters
- High Speed Sampling Circuits
- Line Receiver
- Extended Range V to F Converters
- Fast Pulse Height/Width Discriminators

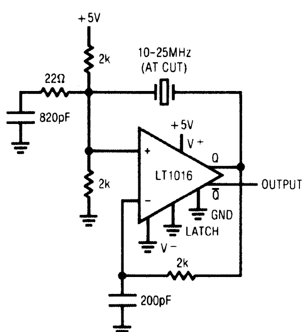
DESCRIPTION

The LT1016 is an ultra fast (10ns) comparator specifically designed to interface directly to TTL logic while operating off either a dual ±5V supply or a single +5V supply. Tight offset voltage specifications and high gain allow the LT1016 to be used in precision applications. Matched complementary outputs further extend the versatility of this new comparator.

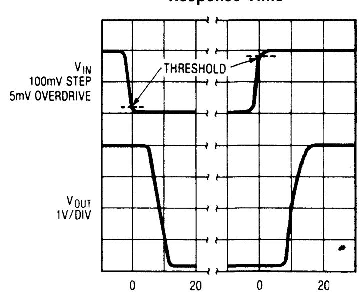
A unique output stage is featured on the LT1016. It provides active drive in both directions for maximum speed into TTL logic or passive loads, yet does not exhibit the large current spikes normally found in "totem pole" output stages. This eliminates the need for a minimum input slew rate typical of other very fast comparators. The ability of the LT1016 to remain stable with the outputs in the active region greatly reduces the problem of output "glitching" when the input signal is slow moving or is low level.

The LT1016 has a true latch pin for retaining input data at the outputs. The outputs will remain latched as long as the latch pin is held high. Quiescent negative power supply current is only 3mA—about ten times lower than competitive units. This reduces die temperature and allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

10-25MHz Crystal Oscillator



Response Time

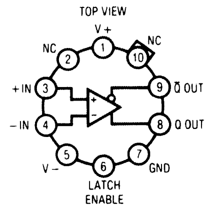
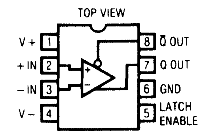


TEXAS INSTRUMENTS

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (Note 4) 7V
Negative Supply Voltage 7V
Differential Input Voltage .... ±5V
Input Voltage (Either Input) .... Equal to Supplies
Latch Pin Voltage .... Equal to Supplies
Output Current (Continuous) .... ±20mA
Operating Temperature Range
  LT1016M .... −55°C to +125°C
  LT1016C .... 0°C to +70°C
Storage Temperaure Range ...... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 METAL CAN L PACKAGE	LT1016ML LT1016CL
 HERMETIC DIP JG PACKAGE PLASTIC DIP D OR P PACKAGE	LT1016MJG LT1016CJG LT1016CP LT1016CD

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = 5V$, $V_{OUT}(Q) = 1.4V$, $V_{LATCH} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS			LT1016M MIN	LT1016M TYP	LT1016M MAX	LT1016C MIN	LT1016C TYP	LT1016C MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$ (Note 1)				0.8	±2		1.0	±3	mV
				●			3			3.5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift			●		4			4		μV/°C
I_{OS}	Input Offset Current	(Note 1)				0.3	1		0.3	1	μA
				●			1.3		0.3	1.3	μA
I_B	Input Bias Current	(Note 2)				5	10		5	10	μA
				●			13			13	μA
	Input Voltage Range	(Note 5)		●	−3.75		+3.5	−3.75		+3.5	V
		Single +5V Supply		●	+1.25		+3.5	+1.25		+3.5	V
CMRR	Common-Mode Rejection	$-3.75V \leq V_{CM} \leq +3.5V$		●	80	96		80	96		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \leq V^+ \leq 5.4V$		●	60	75		60	75		dB
		Negative Supply $2V \leq V^- \leq 7V$		●	80	100		80	100		dB
A_V	Small Signal Voltage Gain	$1V \leq V_{OUT} \leq 2V$			1400	3000		1400	3000		V/V
V_{OH}	Output High Voltage	$V^+ \leq 4.6V$,	$I_{OUT} = 1mA$	●	2.7	3.1		2.7	3.1		V
			$I_{OUT} = 10mA$	●	2.4	3.0		2.4	3.0		V
V_{OL}	Output Low Voltage		$I_{SINK} = 4mA$	●		0.3	0.5		0.3	0.5	V
			$I_{SINK} = 10mA$			0.4			0.4		V
I^+	Positive Supply Current			●		25	35		25	35	mA
I^-	Negative Supply Current			●		3	5		3	5	mA
V_{IH}	Latch Pin Hi Input Voltage			●	2.0			2.0			V
V_{IL}	Latch Pin Lo Input Voltage			●			0.8			0.8	V
I_{IL}	Latch Pin Current	$V_{LATCH} = 0V$		●			500			500	μA

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = 5V$, $V_{OUT}(Q) = 1.4V$, $V_{LATCH} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS		LT1016M MIN	LT1016M TYP	LT1016M MAX	LT1016C MIN	LT1016C TYP	LT1016C MAX	UNITS
t_{PD}	Propagation Delay	$\Delta V_{IN} = 100mV$, OD = 5mV			10	14		10	14	ns
	(Note 3)		●			16			16	ns
		$\Delta V_{IN} = 100mV$, OD = 20mV			9	12		9	12	ns
			●			15			15	ns
Δt_{PD}	Differential Propagation Delay	(Note 3) $\Delta V_{IN} = 100mV$; OD = 5mV				3			3	ns
	Latch Setup Time				2			2		ns

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

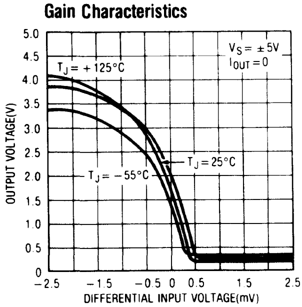
Note 3: t_{PD} and Δt_{PD} cannot be measured in automatic-handling test equipment with low values of overdrive. The LT1016 is tested with a 1-V step and 500-mV overdrive. Correlation testing has indicated that t_{PD} and Δt_{PD} limits shown can be met with this test. For low overdrive conditions, V_{OS} is added to the overdrive.

Note 4: Electrical specifications apply only up to 5.4V.

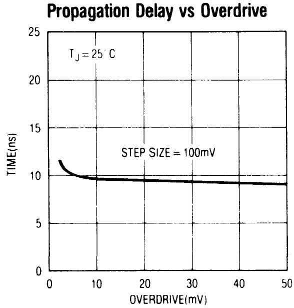
Note 5: See text for discussion of input voltage range for supplies other than ±5V, or +5V.

TYPICAL PERFORMANCE CHARACTERISTICS

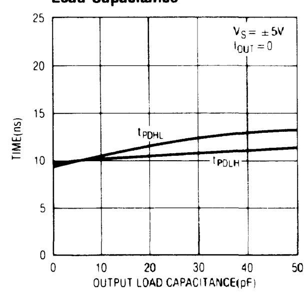
Gain Characteristics



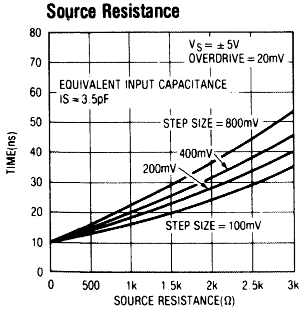
Propagation Delay vs Overdrive



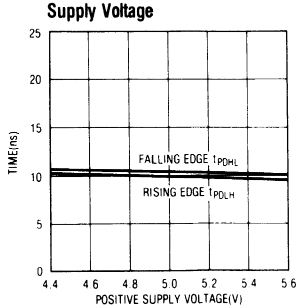
Propagation Delay vs Load Capacitance



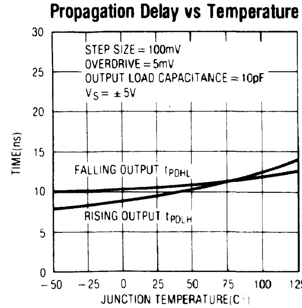
Propagation Delay vs Source Resistance



Propagation Delay vs Supply Voltage

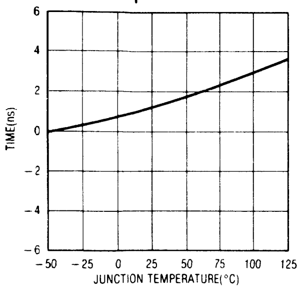


Propagation Delay vs Temperature

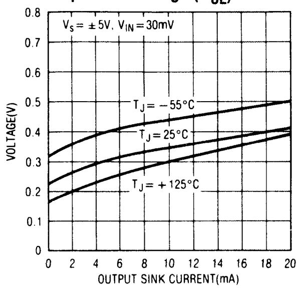


TYPICAL PERFORMANCE CHARACTERISTICS

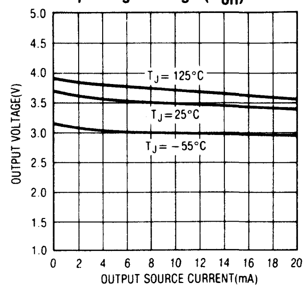
Latch Set-Up Time



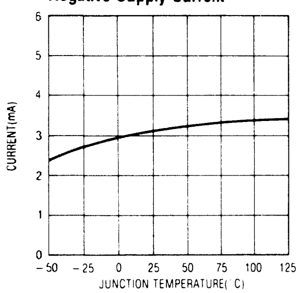
Output Low Voltage (V_{OL})



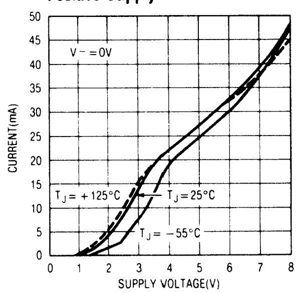
Output High Voltage (V_{OH})



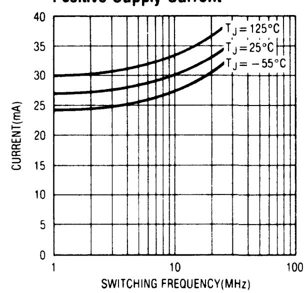
Negative Supply Current



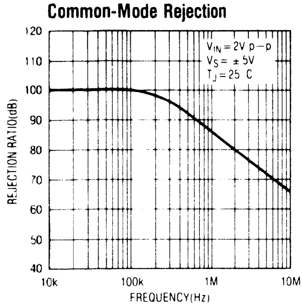
Positive Supply Current



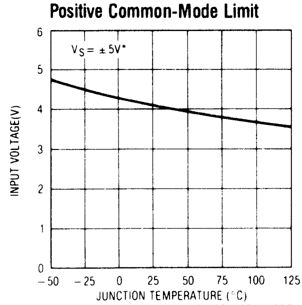
Positive Supply Current



Common-Mode Rejection

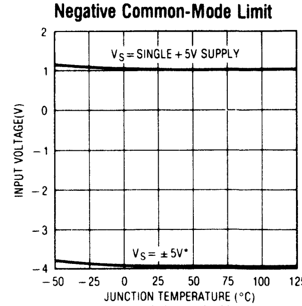


Positive Common-Mode Limit



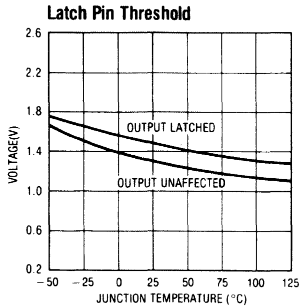
*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE

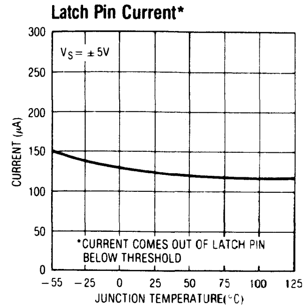
Negative Common-Mode Limit



*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE.

TYPICAL PERFORMANCE CHARACTERISTICS





APPLICATIONS INFORMATION

Common-Mode Considerations

The LT1016 is specified for a common-mode range of −3.75V to +3.5V with supply voltages of ±5V. A more general consideration is that the common-mode range is 1.25V above the negative supply and 1.5V below the positive supply, independent of the actual supply voltage. The criteria for common-mode limit is that the output still responds correctly to a small differential input signal. Either input may be outside the common-mode limit (up to the supply voltage) as long as the remaining input is within the specified limit, and the output will still respond correctly. There is one consideration, however, for inputs which exceed the positive common-mode limit. Propagation delay will be increased by up to 10ns if the signal input is more positive than the upper common-mode limit and then switches back to within the common-mode range. This effect is not seen for signals more negative than the lower common-mode limit.

Input Impedance and Bias Current

Input bias current is measured with the output held at 1.4V. As with any simple NPN differential input stage, the LT1016 bias current will go to zero on an input which is low and double on the input which is high. If both inputs are less than 0.8V above V^-, both input bias currents will go to zero. If either input exceeds the positive common-mode limit, input bias current will increase rapidly, approaching several milliamperes at $V_{IN} = V^+$.

Differential input resistance at zero differential input voltage is about 10kΩ, rapidly increasing as larger DC differential input signals are applied. Common-mode input resistance is about 4MΩ with zero differential input voltage. With large differential input signals, the high input will have an input resistance of about 2MΩ and the low input, greater than 20MΩ.

Input capacitance is typically 3.5pF. This is measured by inserting a 1kΩ resistor in series with the input and measuring the resultant change in propagation delay.

Latch Pin Dynamics

The latch pin is intended to retain input data (output latched) when the latch pin goes high. This pin will float to a high state when disconnected, so a flow-through condition requires that the latch pin be grounded. To ensure data retention, the input signal must be valid at least 5ns before the latch goes high (set-up time) and must remain valid at least 3ns after the latch goes high (hold time). When the latch goes low, new data will appear at the output in approximately 8–10ns. The latch pin is designed to be driven with TTL or CMOS gates. It has no built-in hysteresis.

APPLICATIONS INFORMATION

Measuring Response Time

The LT1016 is able to respond quickly to fast low level signals because it has a very high gain-bandwidth product ($\approx$50GHz), even at very high frequencies. To properly measure the response of the LT1016 requires an input signal source with very fast rise times and exceptionally clean settling characteristics. This last requirement comes about because the standard comparator test calls for an input step size that is large compared to the overdrive amplitude. Typical test conditions are 100mV step size with only 5mV overdrive. This requires an input signal that settles to within 1% (1mV) of final value in only a few nanoseconds with no ringing or "long tailing". Ordinary high speed pulse generators are not capable of generating such a signal, and in any case, no ordinary oscilloscope is capable of diplaying the waveform to check its fidelity. Some means must be used to inherently generate a fast, clean edge with known final value.

The circuit shown in Figure 1 is the best *electronic* means of generating a known fast, clean step to test comparators. It uses a very fast transistor in a common base configuration. The transistor is switched "off" with a fast edge from the generator and the collector voltage settles to exactly 0V in just a few nanoseconds. The most important feature of this circuit is the lack of feedthrough from the generator to the comparator input. This prevents overshoot on the comparator input which would give a false fast reading on comparator response time.

To adjust this circuit for exactly 5mV overdrive, V_1 is adjusted so that the LT1016 output under test settles to 1.4V (in the linear region). Then V_1 is *changed* 5V to set overdrive at 5mV.

The test circuit shown measures low to high transition on the "+" input. For opposite polarity transitions on the output, simply reverse the inputs of the LT1016.

High Speed Design Techniques

A substantial amount of design effort has made the LT1016 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1016 is stable in its linear region, a feature no other high speed comparator has. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. These features make the application of the 50GHz gain-bandwidth LT1016 considerably easier than other fast comparators. Unfortunately, laws of physics dictate that the circuit *environment* the LT1016 works in must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance, and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1016 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1016's (Trace B)

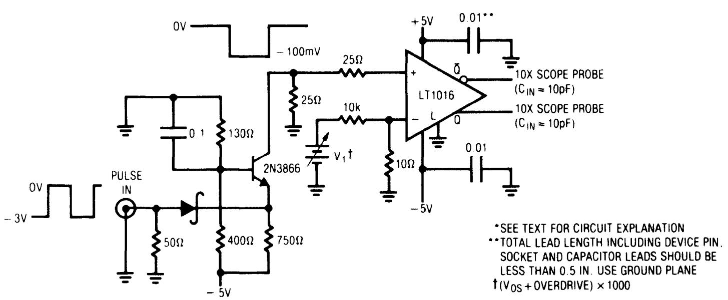


Figure 1. Response Time Test Circuit

APPLICATIONS INFORMATION

response to the pulse generator (Trace A) is as fast as a TTL inverter (Trace C) even when the LT1016 has only millivolts of input signal! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully. An unbypassed LT1016 is shown responding to a pulse input in Figure 3. The power supply the LT1016 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1016, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

In Figure 4 the LT1016's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount*

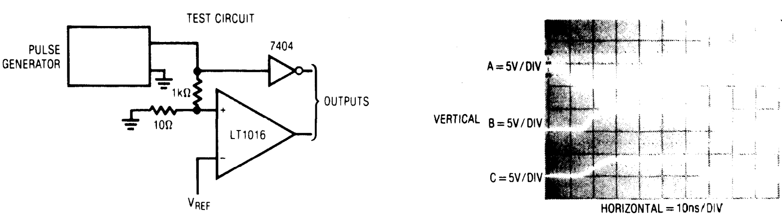


Figure 2. LT1016 vs a TTL Gate

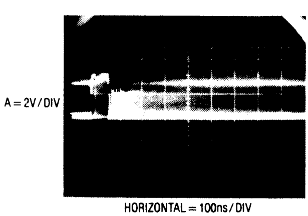


Figure 3. Unbypassed LT1016 Response

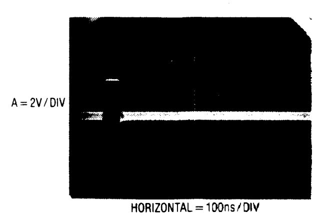


Figure 4. LT1016 Response with Poor Bypassing

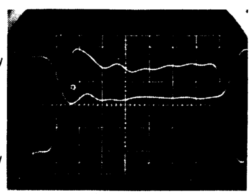
APPLICATIONS INFORMATION

them as close as possible to the LT1016. An inch of wire between the capacitor and the LT1016 can cause problems. If operation in the linear region is desired, the LT1016 must be over a ground plate with good RF bypass capacitors (≥ 0.01μF) having lead lengths less than 0.2 inches. Do not use sockets.

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V — quite a trick for a device running from a +5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly.* Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 10ns response time LT1016 appears to have 50ns edges! In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

In Figure 7 the probes are properly selected and applied but the LT1016's output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. *Keep the probe ground connection as short as possible.*

A = 2V/DIV

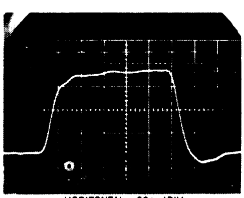


B = 2V/DIV

HORIZONTAL = 10ns/DIV

Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

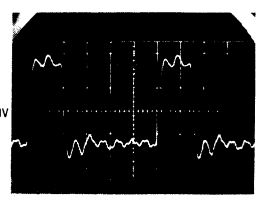
VERTICAL = 1V/DIV



HORIZONTAL = 50ns/DIV

Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

VERTICAL = 1V/DIV



HORIZONTAL = 20ns/DIV

Figure 7. Typical Results Due to Poor Probe Grounding

APPLICATIONS INFORMATION

Figure 8 shows the LT1016's output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1016's ground pin connection is 1 inch long. The ground lead of the LT1016 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1016's ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1016's ground pin connection as short (typically ¼ inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

Figure 9 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1016 without a "ground plane." A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1016, when input signal levels are low or slow moving.*

"Fuzz" on the edges is the difficulty in Figure 10. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3kΩ input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedances as low as possible, preferably 1kΩ or less. Route output and input pins and components away from each other.*

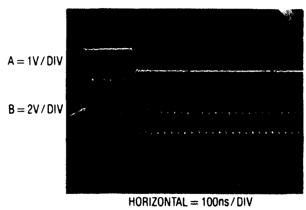


Figure 8. Excessive LT1016 Ground Path Resistance Causes Oscillation

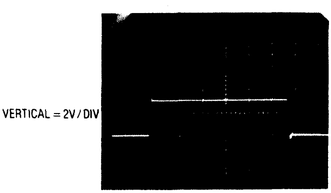


Figure 9. Transition Instabilities Due to No Ground Plane

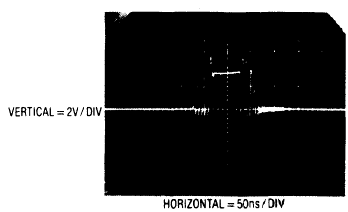


Figure 10. 3pF Stray Capacitive Feedback with 3kΩ Source Can Cause Oscillation

APPLICATIONS INFORMATION

The opposite of stray-caused oscillations appears in Figure 11. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input, and output delay occurs. An RC combination of 2kΩ source resistance and 10pF to ground gives a 20ns time constant — significantly longer than the LT1016's response time. *Keep source impedances low and minimize stray input capacitance to ground.*

Figure 12 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few circumstances it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.*

Another output-caused fault is shown in Figure 13. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead which is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω–400Ω).*

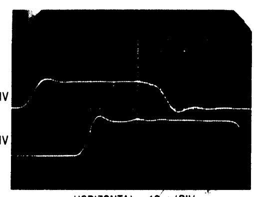


Figure 11. Stray 5pF Capacitance from Input to Ground Causes Delay

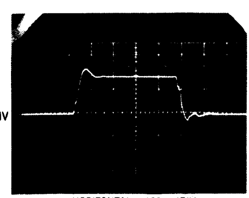


Figure 12. Excessive Load Capacitance Forces Edge Distortion

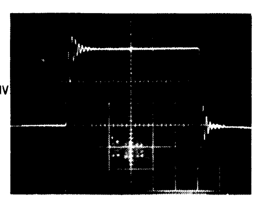


Figure 13. Lengthy, Unterminated Output Lines Ring from Reflections

APPLICATIONS INFORMATION

200ns-0.01% Sample-and-Hold Circuit

Figure 14's circuit uses the LT1016's high speed to improve upon a standard circuit function. The 200ns acquisition time is well beyond monolithic sample-and-hold capabilities. Other specifications exceed the best commercial unit's performance. This circuit also gets around many of the problems associated with standard sample-and-hold approaches, including FET switch errors and amplifier settling time. To achieve this, the LT1016's high speed is used in a circuit which completely abandons traditional sample-and-hold methods.

Important specifications for this circuit include:

Acquisition Time	<200ns
Common-Mode Input Range	±3V
Droop	1μV/μs
Hold Step	2mV
Hold Settling Time	15ns
Feedthrough Rejection	>>100dB

When the sample-hold line goes low, a linear ramp starts just below the input level and ramps upward. When the ramp voltage reaches the input voltage, A1 shuts off the ramp, latches itself off, and sends out a signal indicating sampling is complete.

1.8μs, 12-Bit A-D Converter

The LT1016's high speed is used to implement a very fast 12-bit A-D converter in Figure 15. The circuit is a modified form of the standard successive approximation approach and is faster than most commercial SAR 12-bit units. In this arrangement the 2504 successive approximation register (SAR), A1 and C1 test each bit, beginning with the MSB, and produce a digital word representing V_{IN}'s value. To get faster conversion time, the clock is controlled by the window comparator monitoring the DAC-input summing junction. Additionally, the DMOS FET clamps the DAC output to ground at the beginning of each clock cycle, shortening DAC settling time. After the fifth bit is converted, the clock runs at maximum speed.

1Hz-10MHz V→F Converter

The LT1016 and the LT1012 low drift amplifier combine to form a high speed V→F converter in Figure 16. A variety of circuit techniques is used to achieve a 1Hz to 10MHz output. Overrange to 12MHz (V_{IN} = 12V) is provided. This circuit has a wider dynamic range (140dB, or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V→F's. The theory of operation is based on the identity Q = CV.

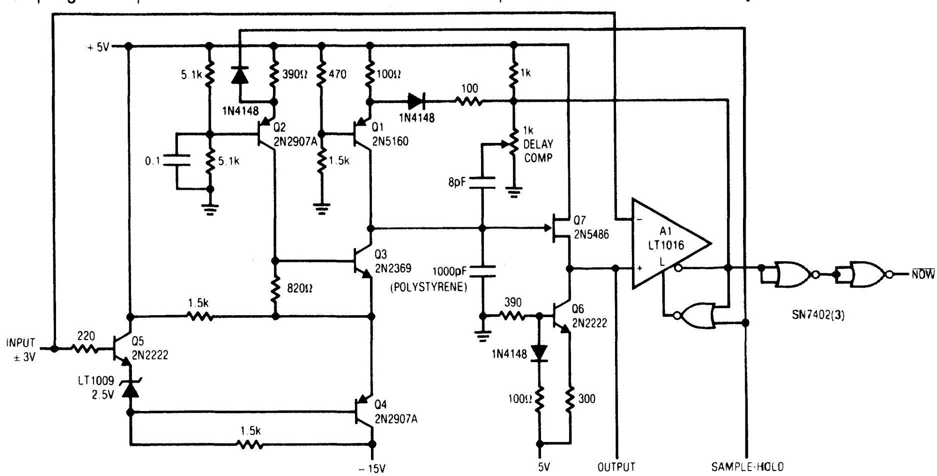


Figure 14. 200ns Sample-and Hold

APPLICATIONS INFORMATION

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

To trim this circuit, ground the input and adjust the 1k pot for 1Hz output. Next, apply 10.000V and set the 2kΩ unit for 10.000MHz output. The transfer linearity of the circuit is 0.06%. Full-scale drift is typically 50ppm/°C and zero point error about 0.2μV/°C (0.2Hz/°C).

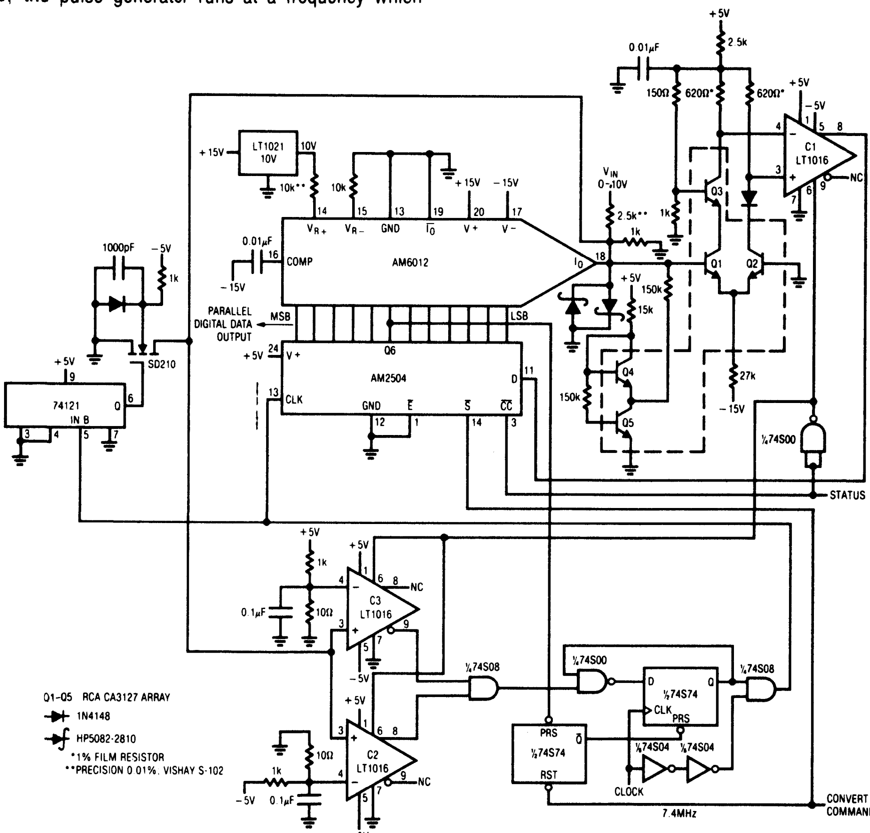


Figure 15. 12-Bit 1.8μs SAR A→D

TEXAS INSTRUMENTS

APPLICATIONS INFORMATION

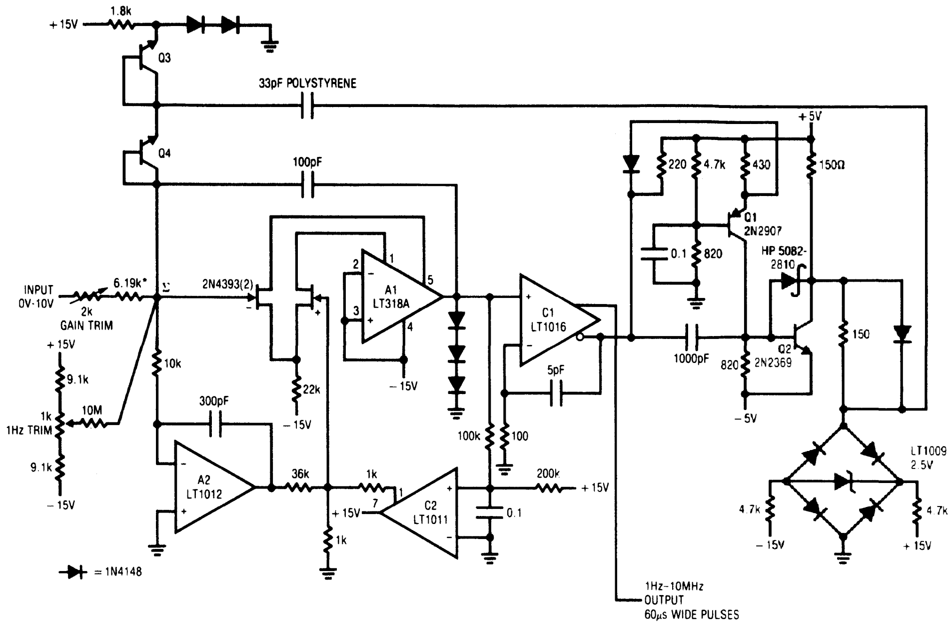
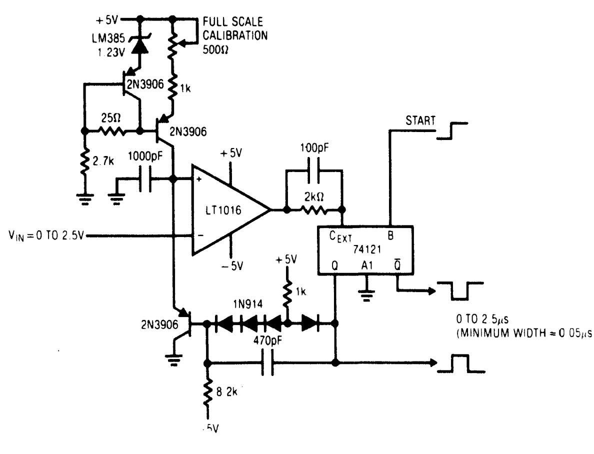


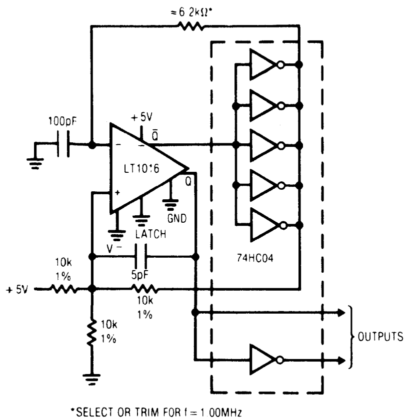
Figure 16. 1Hz-10MHz V to F Converter

Voltage Controlled Pulse Width Generator

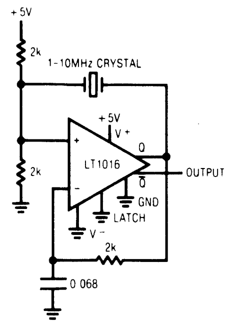


APPLICATIONS INFORMATION

Single Supply Precision RC 1MHz Oscillator



1-10MHz Crystal Oscillator



APPENDIX A

About Level Shifts

The TTL output of the LT1016 will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1016-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1016 is a sink-source pair (Figure A1) with good ability to drive capacitance (such as feedforward capacitors).

Figure A2 shows a non-inverting voltage gain stage with a 15V output. When the LT1016 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

Figure A3 is a very versatile stage. It features a bipolar swing which may be programmed by varying the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1016 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1016's output transition (Trace A, Figure A4), but Q2's switching is clean (Trace B, Figure A4) with 3ns delay on the rise and fall of the pulse.

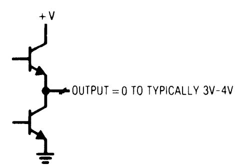


Figure A1

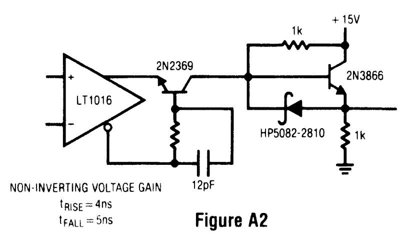


Figure A2

TEXAS INSTRUMENTS

APPENDIX A

Figure A5 is similar to A2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET which switches 1A at 15V. Most of the 7ns–9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T's. To get the kind of results shown, switching times in the ns range and f_T's approaching 1GHz are required.

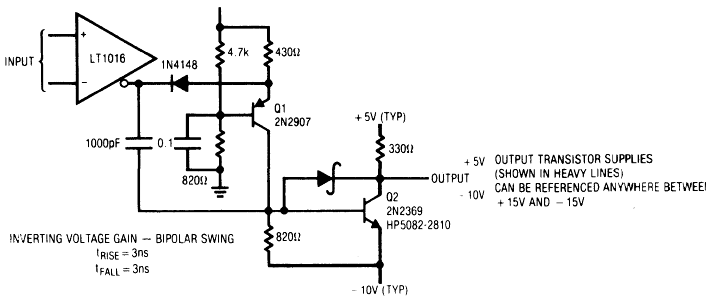


Figure A3

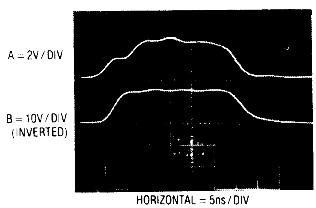


Figure A4. Figure A3's Waveforms

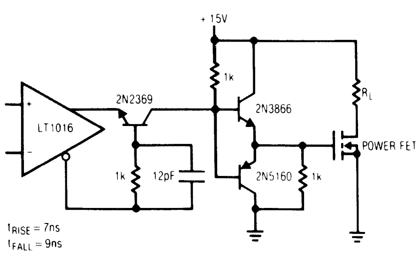
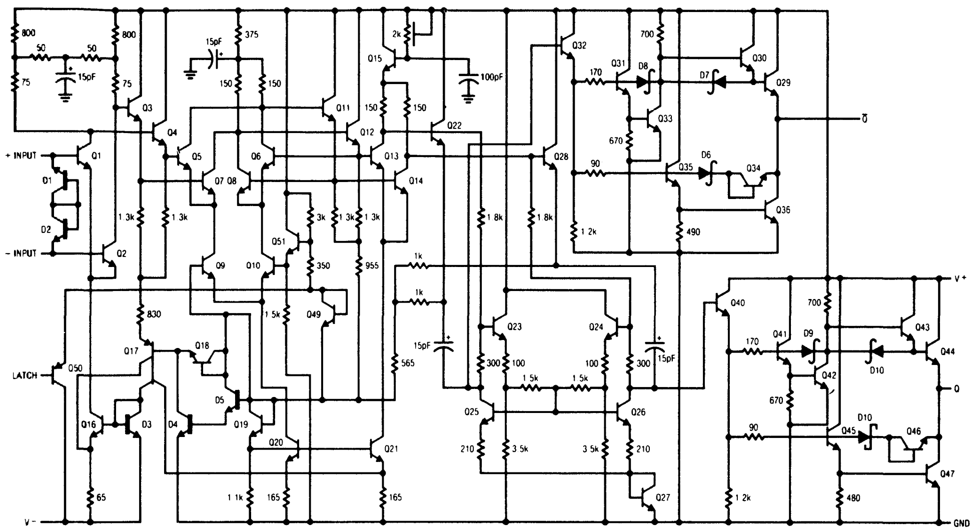


Figure A5

4 Voltage Comparators

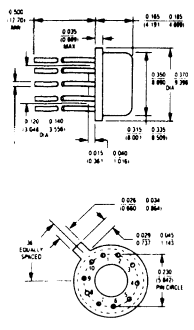
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

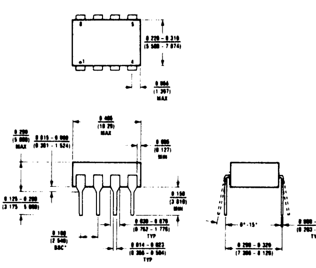
Dimensions in inches (millimeters) unless otherwise noted.

10 Lead TO-5 Metal Can (L)



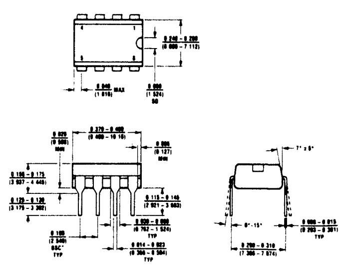
	T_j MAX	Θ_{ja}	Θ_{jc}
LT119AH LM119H	150°C	150°C/W	45°C/W
LT319AH LM319H	85°C	150°C/W	45°C/W

JG Package 8 Lead Hermetic Dip



$T_j$max	Θ_{ja}
150°C	100°C/W

P Package 8 Lead Plastic

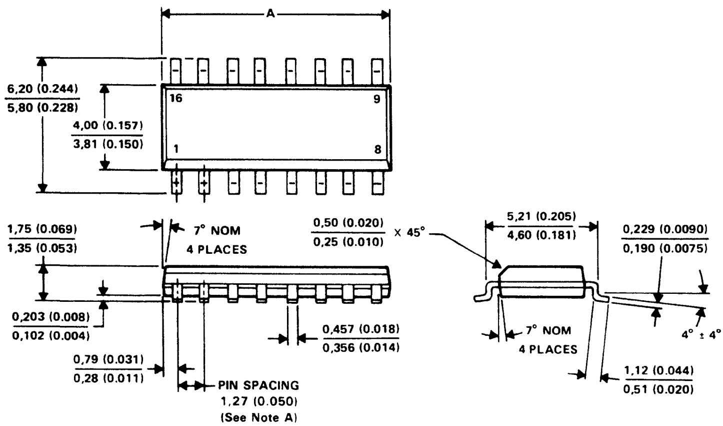


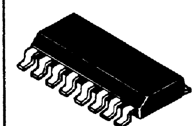
$T_j$max	Θ_{ja}
100°C	130°C/W

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)





DIM \ PINS		8	14	16
A MIN		4,80	8,55	9,80
		(0.189)	(0.337)	(0.386)
A MAX		5,00	8,74	10,00
		(0.197)	(0.344)	(0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

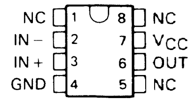
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

TYPES TL331M, TL331I, TL331C DIFFERENTIAL COMPARATORS

D2344, APRIL 1977 – REVISED AUGUST 1983

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (TL331M)
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

D, JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



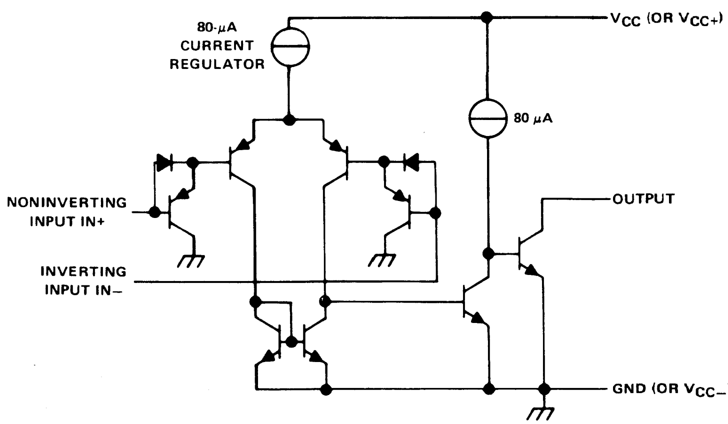
NC – No internal connection

description

The TL331 is a voltage comparator that is designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 volts to 36 volts and pin 7 is at least 1.5 volts more positive than the input common-mode voltage. Current drain is independent of the supply voltage.

The TL331M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL331I is characterized for operation from −25°C to 85°C. The TL331C is characterized for operation from 0°C to 70°C.

schematic



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	680 mW
Operating free-air temperature range: TL331M	−55°C to 125°C
TL331I	−25°C to 85°C
TL331C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the JG package, TL331M chips are alloy-mounted; TL331I and TL331C chips are glass-mounted.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TL331M, TL331I			TL331C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		25°C		2	5		2	5	mV
				Full range			9			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		5	50	nA
				Full range			100			150	
I_{IB}	Input bias current			25°C		−25	−100		−25	−250	nA
				Full range			−300			−400	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 30 V		25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
				Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L = 15 kΩ to V_{CC}		25°C		200			200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 30 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6			6			mA
I_{CC}	Supply current	V_O = 2.5 V,	No load	25°C		0.5	0.8		0.5	0.8	mA

† Full range (MIN to MAX) for TL331M is −55°C to 125°C, for the TL311I is −25°C to 85°C, and for the TL331C is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 5	100-mV input step with 5-mV overdrive		1.3		μs
		TTL-level input step		0.3		

‡ C_L includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

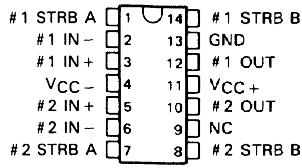
TEXAS INSTRUMENTS

TYPES TL506M, TL506C
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

D1208, MARCH 1971—REVISED AUGUST 1983

- **Each Comparator Identical to LM106 or LM306 with Common V_{CC+}, V_{CC-}, and Ground Connections**
- **Improved Gain and Accuracy**
- **Fan-Out to 10 Series 54/74 TTL Loads**
- **Strobe Capability**
- **Short-Circuit and Surge Protection**
- **Fast Response Times**

TL506M . . . J OR W PACKAGE
TL506C . . . J OR N PACKAGE
(TOP VIEW)



NC—No internal connection

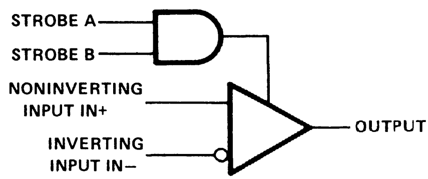
description

The TL506 is a dual high-speed comparator, with each half having differential inputs, a low-impedance output with high-sink-current capability (100 mA), and two strobe inputs. This device detects low-level analog or digital signals and can drive digital logic or lamps and relays directly. Short-circuit protection and surge-current limiting is provided.

The circuit is similar to a TL810 with gated output. A low-level input at either strobe causes the output to remain high regardless of the differential input. When both strobe inputs are either open or at a high logic level, the output voltage is controlled by the differential input voltage. The circuit will operate with any negative supply voltage between −3 V and −12 V with little difference in performance.

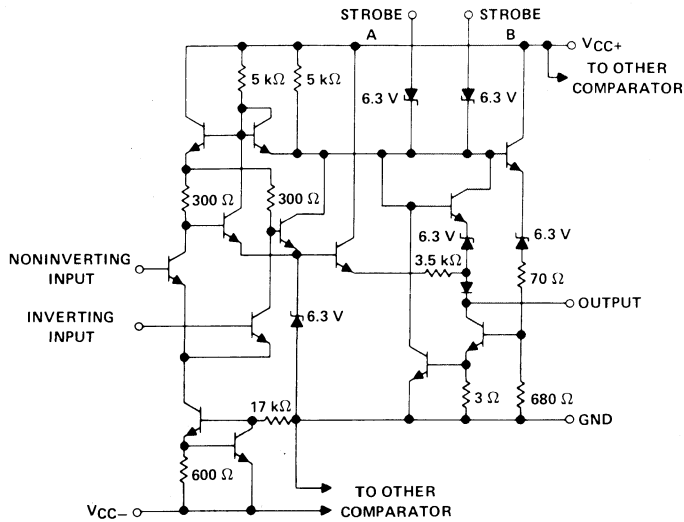
The TL506M is characterized for operation over the full military temperature range of −55 °C to 125 °C; the TL506C is characterized for operation from 0 °C to 70 °C.

functional block diagram (each comparator)



Not recommended for new design

schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless othewise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-} (see Note 1)	−15 V
Differential input voltage (see Note 2)	±5 V
Input voltage (any input, see Notes 1 and 3)	±7 V
Strobe voltage range (see Note 1)	0 V to V_{CC+}
Output voltage (see Note 1)	24 V
Voltage from output to V_{CC-}	30 V
Duration of output short-circuit (see Note 4)	10 s
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5):	
J package (TL506MJ)	1375 mW
J package (TL506CJ)	1025 mW
N package	875 mW
W package	1000 mW
Operating free-air temperature range: TL506M	−55°C to 125°C
TL506C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages and the voltage from the output to V_{CC-}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 7 V, whichever is less.
4. One output at a time may be shorted to ground or either power supply.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, TL506M chips are alloy mounted; TL506C chips are glass mounted.

electrical characteristics at specified free-air temperature, $V_{CC+} = 12$ V, $V_{CC-} = -3$ V to -12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL506M MIN	TL506M TYP	TL506M MAX	TL506C MIN	TL506C TYP	TL506C MAX	UNIT
V_{IO}	Input offset voltage	See Note 6	25°C		0.5‡	2		1.6‡	5	mV
			Full range			3			6.5	
α_{VIO}	Average temperature coefficient of * input offset voltage	See Note 6	Full range		3	10		5	20	μV/°C
I_{IO}	Input offset current	See Note 6	25°C		0.7‡	3		1.8‡	5	μA
			MIN		2	7		1	7.5	
			MAX		0.4	3		0.5		
α_{IIO}	Average temperature coefficient of input * offset current	See Note 6	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	$V_O = 0.5$ V to 5 V	25°C		7‡	20		16‡	25	μA
			Full range			45			40	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)} = 0.4$ V	Full range		−1.7‡	−3.3		1.7‡	3.3	mA
$V_{IH(S)}$	High-level strobe voltage		Full range	2.5			2.5			V
$V_{IL(S)}$	Low-level strobe voltage		Full range			0.9			0.9	V
V_{ICR}	Common-mode input voltage range	$V_{CC-} = -7$ V to -12 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, $V_O = 0.5$ V to 5 V	25°C		40 000‡			40 000‡		
V_{OH}	High-level output voltage	$V_{ID} = 5$ mV, $I_{OH} = -400$ μA	Full range	2.5		5.5	2.5		5.5	V
V_{OL}	Low-level output voltage	$V_{ID} = -5$ mV, $I_{OL} = 100$ mA	25°C		0.8‡	1.5		0.8‡	2	V
		$V_{ID} = -5$ mV, $I_{OL} = 50$ mA	Full range			1			1	
		$V_{ID} = -5$ mV, $I_{OL} = 16$ mA	Full range			0.4			0.4	
I_{OH}	High-level output current	$V_{ID} = 5$ mV, $V_{OH} = 8$ V to 24 V	25°C		0.02‡	1		0.02‡	2	μA
			Full range			100			100	
I_{CC+}	Supply current from V_{CC+}	$V_{ID} = -5$ mV, See Note 7	Full range		13.9‡	20		13.9‡	20	mA
I_{CC-}	Supply current from V_{CC-}	See Note 7	Full range		6.4	14.4		6.4	14.4	mA

†Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for TL506M is −55°C to 125°C and for the TL506C is 0°C to 70°C.

‡These typical values are at $V_{CC+} = 12$ V, $V_{CC-} = -6$ V, $T_A = 25$°C.

NOTES: 6. The offset voltages and offset currents given are the maximum values required to drive the output down to the low range (V_{OL}) or up to the high range (V_{OH}). Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

7. Power supply currents are measured with the respective noninverting inputs and inverting inputs of both comparators connected in parallel. The outputs are open.

switching characteristics, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V, $T_A = 25$°C

PARAMETER	TEST CONDITIONS†	TL506M MIN	TL506M TYP	TL506M MAX	TL506C MIN	TL506C TYP	TL506C MAX	UNIT
Response time, low-to-high-level output *	$R_L = 390\ \Omega$ to 5 V, $C_L = 15$ pF, See Note 8		28	40		28		ns

NOTE 8: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

*For TL506M these parameters are guaranteed but not tested.

4 Voltage Comparators

TYPICAL CHARACTERISTICS§

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

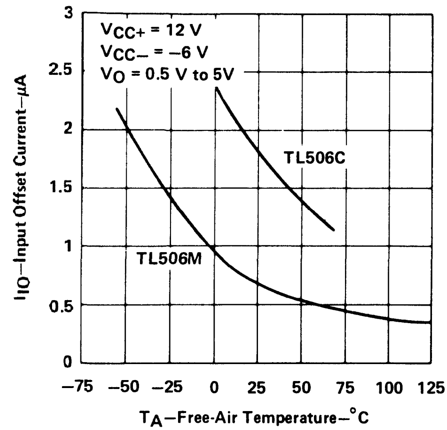


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

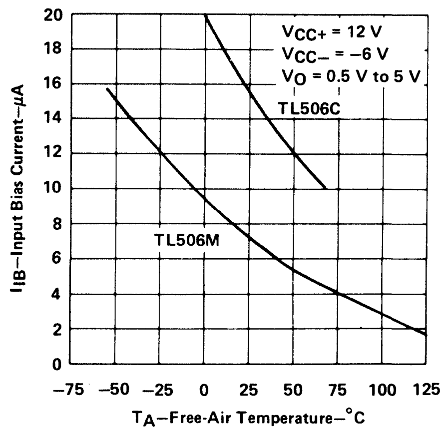


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

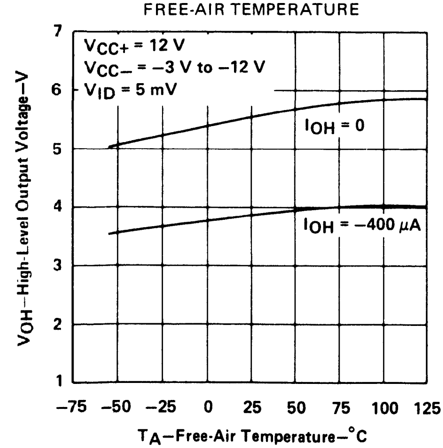


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

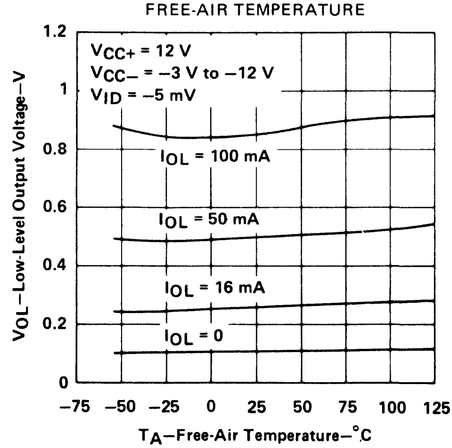


FIGURE 4

§Data for temperatures below 0°C and above 70°C is applicable to TL506M circuits only.

TYPICAL CHARACTERISTICS§

VOLTAGE TRANSFER CHARACTERISTICS

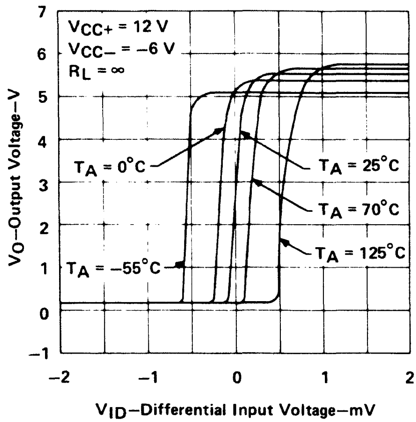


FIGURE 5

OUTPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

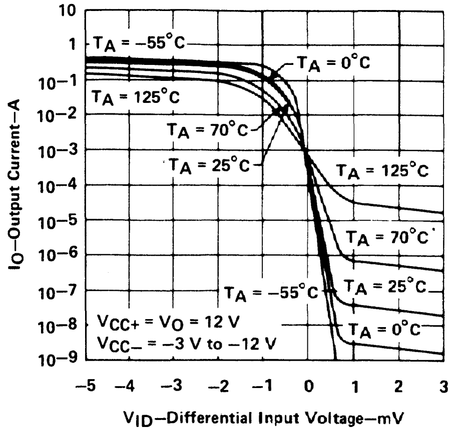


FIGURE 6

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

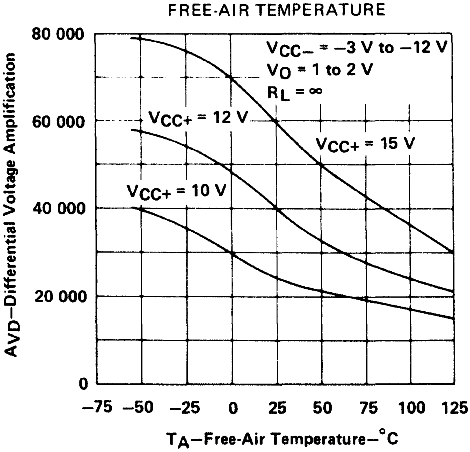


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

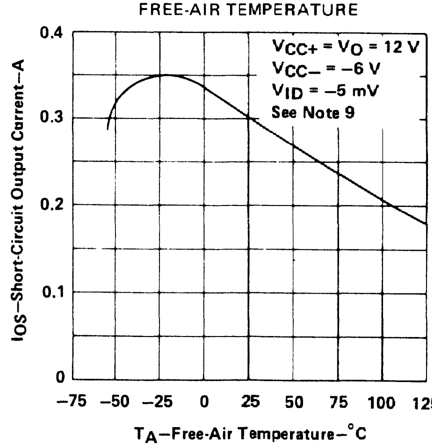


FIGURE 8

§Data for temperatures below 0°C and above 70°C is applicable to TL506M circuits only.

NOTE 9: This parameter was measured using a single 5-ms pulse.

TYPICAL CHARACTERISTICS§

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

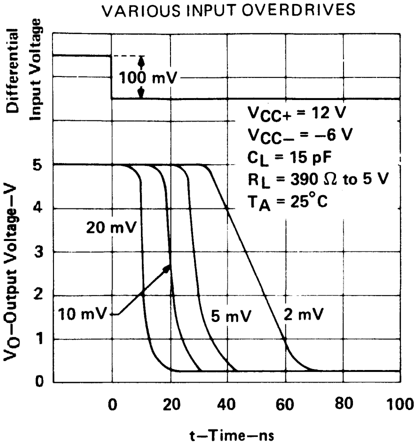


FIGURE 9

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

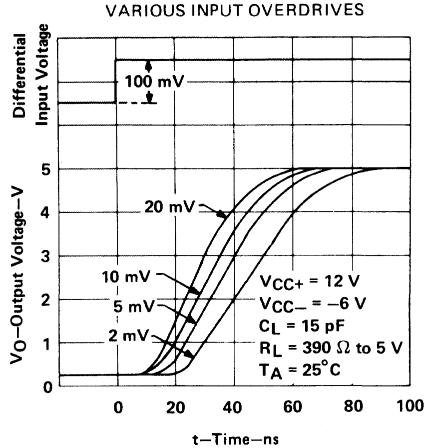


FIGURE 10

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

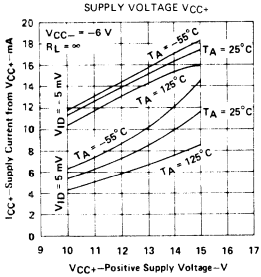


FIGURE 11

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

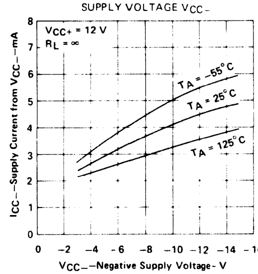


FIGURE 12

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

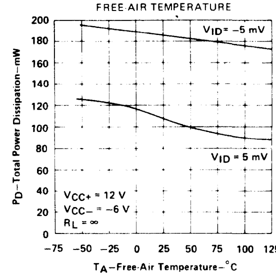


FIGURE 13

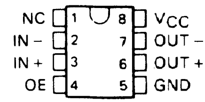
§Data for temperatures below 0°C and above 70°C is applicable to TL506M circuits only.

TL712
DIFFERENTIAL COMPARATOR

D2741, JUNE 1983 REVISED NOVEMBER 1985

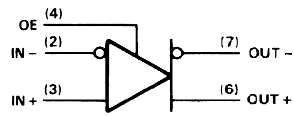
- Operates from a 5-V Supply
- 0 to 5 V Common-Mode Input Voltage Range
- Self-Biased Inputs
- Complementary 3-State Outputs
- Enable Capability
- Hysteresis . . . 5 mV Typ
- Response Times . . . 25 ns Typ

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC - No internal connection

symbol (positive logic)

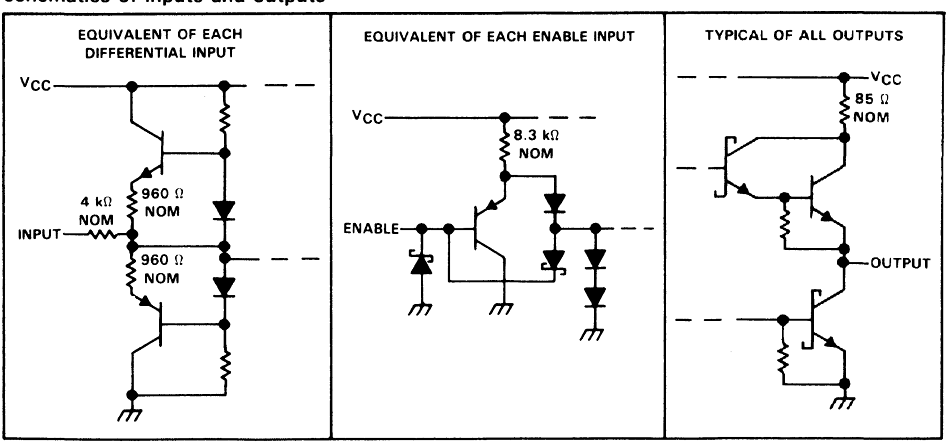


description

The TL712 is a high-speed comparator fabricated with bipolar Schottky† process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable, OE, is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

The TL712 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, any differential input	±25 V
Differential input voltage (see Note 2)	±25 V
Enable input voltage	7 V
Low-level output current	50 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±15	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{CC} = −5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	V_{ICR} = 0 to 5 V	−100†		100	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV, I_{OH} = −1 mA	2.7	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 16 mA		0.4	0.5	V
I_{OZ}	Off-state output current	V_O = 2.4 V			−20	μA
I_I	Enable current	V_I = 5.5 V			100	μA
I_{IH}	High-level enable current	V_{IH} = 2.7 V			20	μA
I_{IL}	Low-level enable current	V_{IL} = 0.4 V			−360	μA
r_i	Differential input resistance		4			kΩ
r_o	Output resistance				100	Ω
I_{OS}	Short-circuit output current		−15		−85	mA
I_{CC}	Supply current	V_{ID} = 0, No load		17	20	mA

† The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TTL load (see Figure 1), See Note 3		25		ns
t_{PHL}	Propagation delay time, high-to-low-level output			25		ns

NOTE 3: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total), and is the interval between the input step function and the instant when the output crosses 2.5 V.

PARAMETER MEASUREMENT INFORMATION

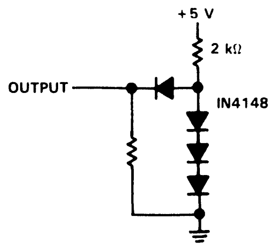


FIGURE 1. TTL OUTPUT LOAD CIRCUIT

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

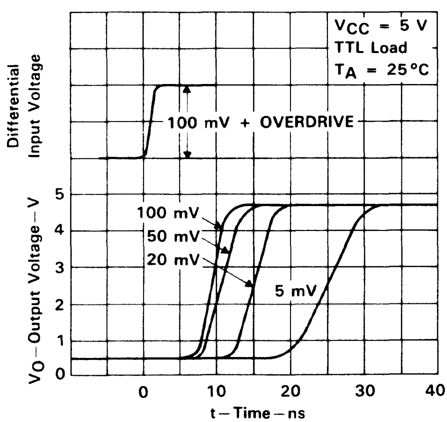


FIGURE 2

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

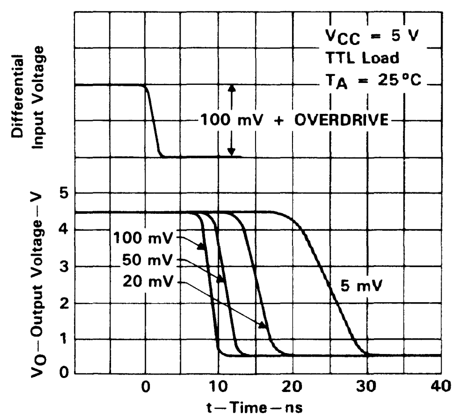


FIGURE 3

TYPICAL CHARACTERISTICS

COMMON-MODE
PULSE RESPONSE

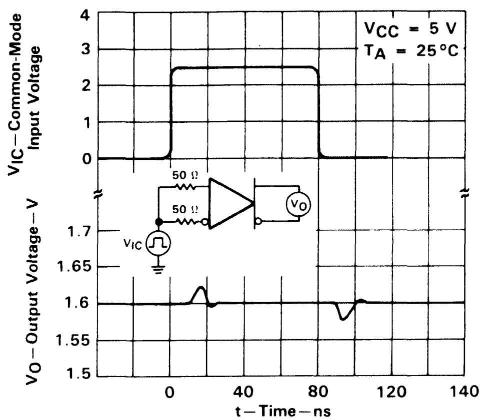


FIGURE 4

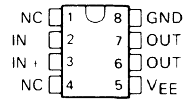
ADVANCE INFORMATION

TL721 DIFFERENTIAL COMPARATOR

D2781 FEBRUARY 1984 REVISED NOVEMBER 1985

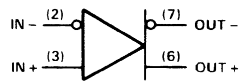
- Operates from a −5.2-V Power Supply
- Self-Biased Inputs
- Common-Mode Input Voltage Range 0 to −5.2 V
- MECL III and MECL 10 000 Compatible
- Complementary ECL-Compatible Outputs
- Hysteresis . . . 5 mV Typ
- Response Times . . . 10 ns Typ

D, JG, OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



NC — No internal connection

symbol



description

The TL721 is a high-speed voltage comparator fabricated with bipolar Schottky† process technology. The circuit has differential analog inputs and complementary ECL-compatible logic outputs with symmetrical switching characteristics. The device operates from a single −5.2-volt supply and is useful as a disk memory read-chain data comparator.

The TL721 is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{EE} (see Note 1) . . . . −7 V
Input voltage, any differential input . . . . ±25 V
Differential input voltage (see Note 2) . . . . ±25 V
Low-level output current . . . . 50 mA
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{EE}		−5.2		V
Common-mode input voltage, V_{IC}			±7	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at T_A = 25°C, V_{EE} = −5.2 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	$V_{IC} = V_{ICR}$ min		−100†		100	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 50 Ω to −2 V	0.96†		0.81	V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	R_L = 50 Ω to −2 V	1.85†		1.65	V
V_{ICR}	Common-mode input voltage range			0 to 5.2			V
r_{in}	Input resistance			4			kΩ
I_{EE}	Supply current	V_{ID} = 0,	No load		13	17	mA

† The algebraic convention, in which the more negative limit is designated as minimum, is used in this data sheet for input threshold and output voltage levels only.

switching characteristics at T_A = 25°C, V_{EE} = −5.2 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	ΔV_{ID} = +200 mV to −200 mV or −200 mV to +200 mV, R_L = 50 Ω to −2 V			12	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	ns

TYPICAL CHARACTERISTICS

OUTPUT RESPONSES FOR VARIOUS INPUT OVERDRIVES

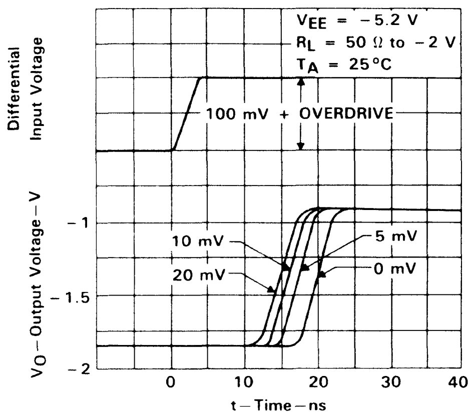


FIGURE 1

OUTPUT RESPONSES FOR VARIOUS INPUT OVERDRIVES

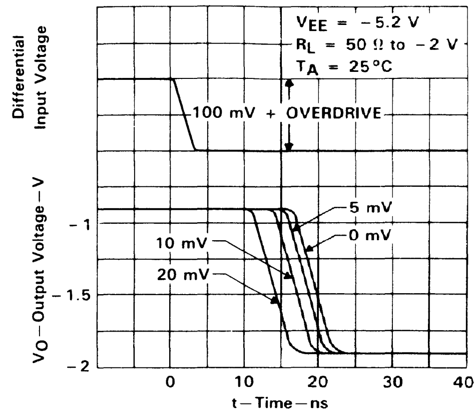


FIGURE 2

COMMON-MODE PULSE RESPONSE

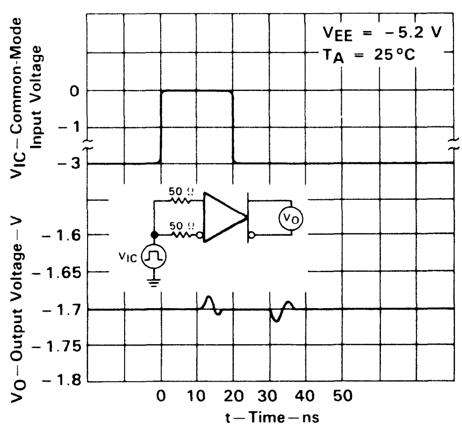


FIGURE 3

4

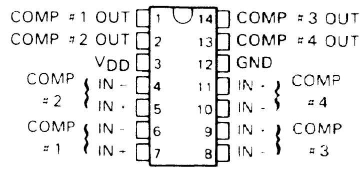
Voltage Comparators

TLC339M, TLC339I, TLC339C QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

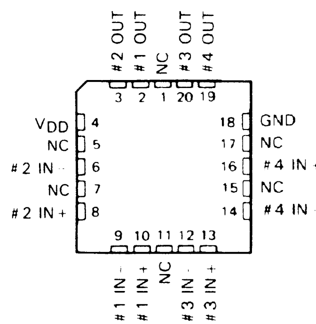
DECEMBER 1986

- Very Low Power ... 200 μW Typ at 5 V
- Fast Response Time ... 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  TLC339M ... 4 V to 16 V
  TLC339I ... 3 V to 16 V
  TLC339C ... 3 V to 16 V
- High Input Impedance ... $10^{12}\,\Omega$ Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC339M ... J PACKAGE
TLC339I ... D, J, OR N PACKAGE
TLC339C ... D, J, OR N PACKAGE
(TOP VIEW)



TLC339M ... FK PACKAGE
(TOP VIEW)

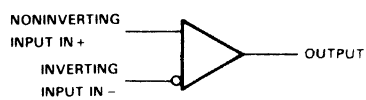


NC – No internal connection

description

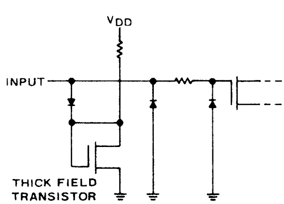
The TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

symbol (each comparator)

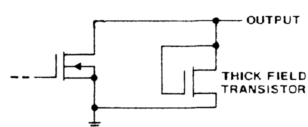


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



LinCMOS is a trademark of Texas Instruments

Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC339M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC339I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)		−0.3 V to 18 V
Differential input voltage (see Note 2)		±18 V
Input voltage, V_I		−0.3 V to V_{DD}
Output voltage, V_O		−0.3 V to V_{DD}
Input current, I_I		±5 mA
Output current, I_O (each output)		20 mA
Total supply current into V_{DD} terminal		40 mA
Total current out of ground terminal		60 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	D package	950 mW
	FK or J package (alloy mount)	1375 mW
	J package (glass mount)	1025 mW
	N package	875 mW
Operating free-air temperature range:	TLC339M	−55°C to 125°C
	TLC339I	−40°C to 85°C
	TLC339C	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or J package		300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For the TLC339M in the J package, use the alloy mount derating factor; for the TLC339I and TLC339C in the J package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
J (alloy mount)	1375 mW	11 mW/°C	25°C
J (glass mount)	1025 mW	6.6 mW/°C	25°C
N	875 mW	7 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}min$, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C		84		dB
			125°C		84		
			-55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			-55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	µA
			Full range			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC339M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			-40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	μA
I_{DD}	Supply current (four comparators)	No load	25°C		44	80	μA
			Full range			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC339I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	μA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	μA
			Full range			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC339C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		μs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+ pin			0.10		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		μs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.1		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		20		ns

4 Voltage Comparators

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

The TLC339 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

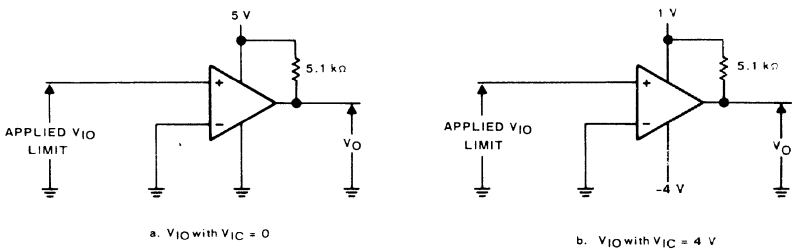


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

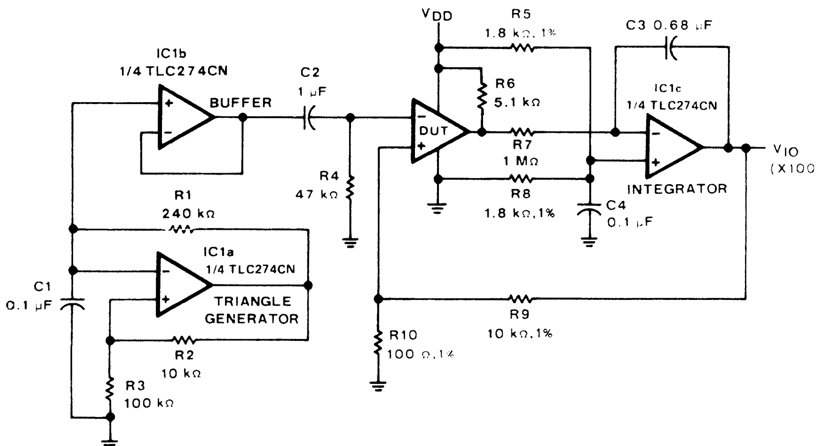
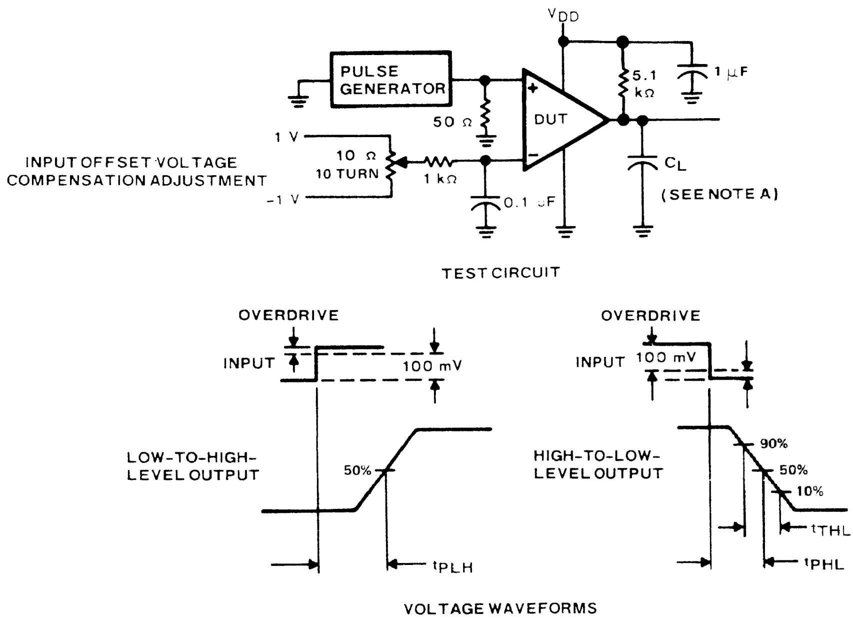


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF INPUT OFFSET VOLTAGE

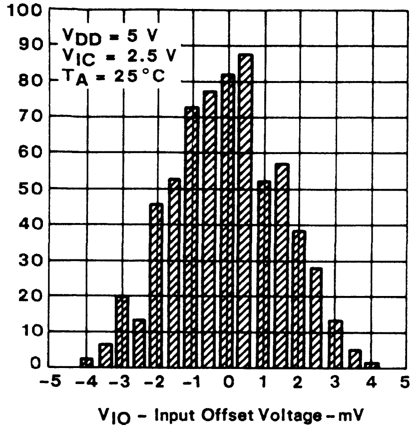


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

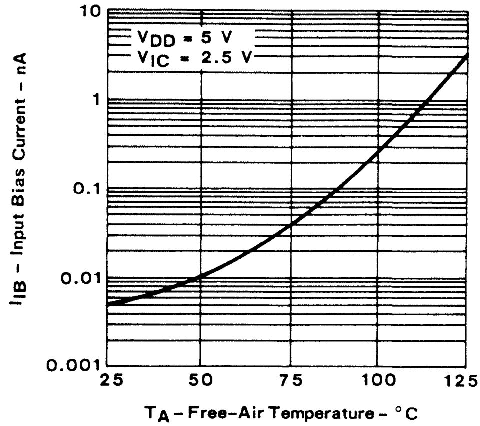


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

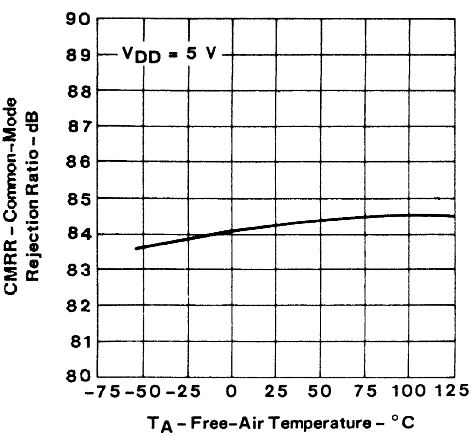


FIGURE 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

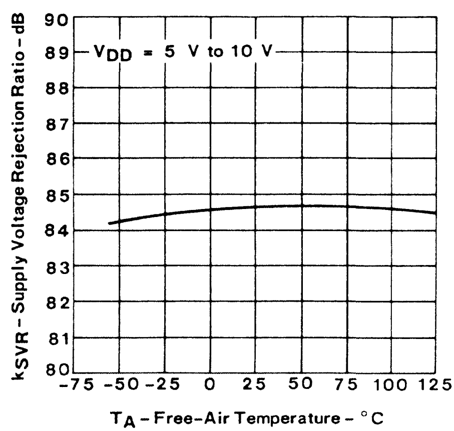


FIGURE 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

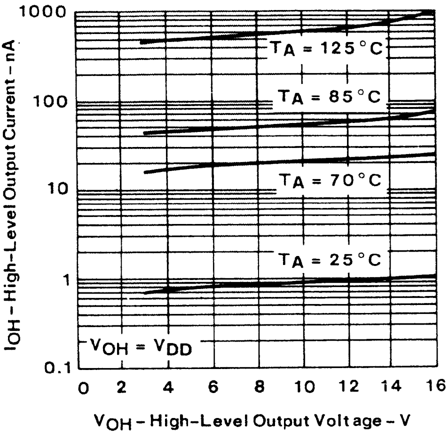


FIGURE 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

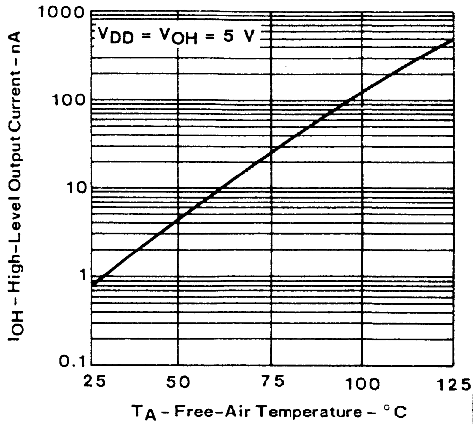


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

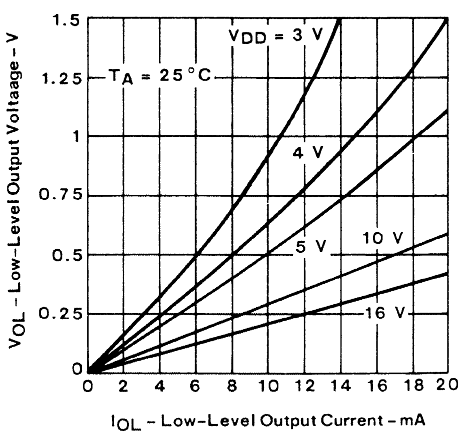


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

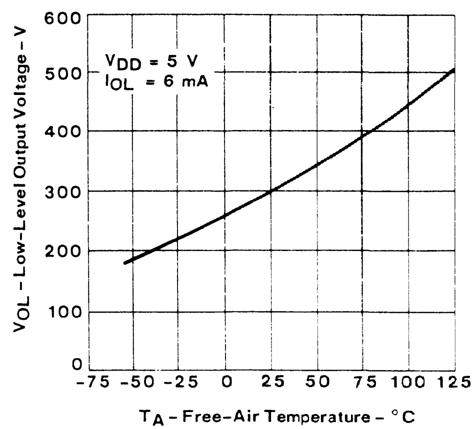


FIGURE 11

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

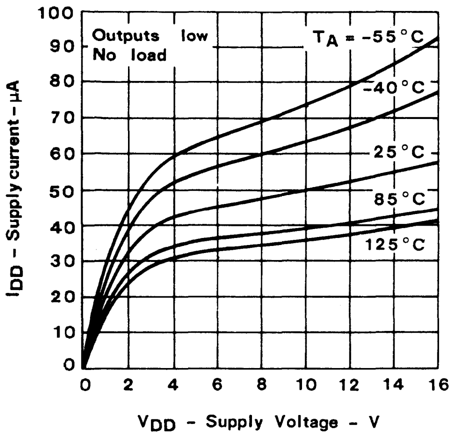


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

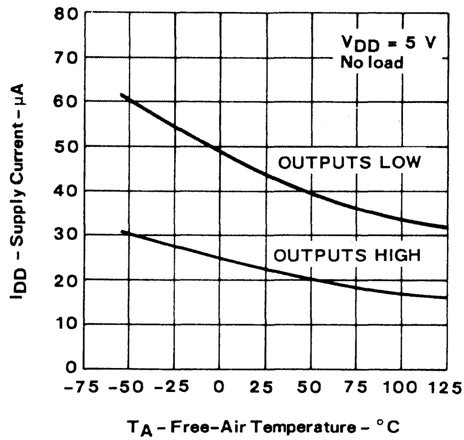


FIGURE 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

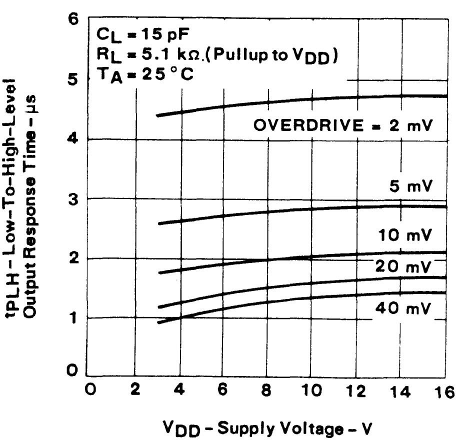


FIGURE 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

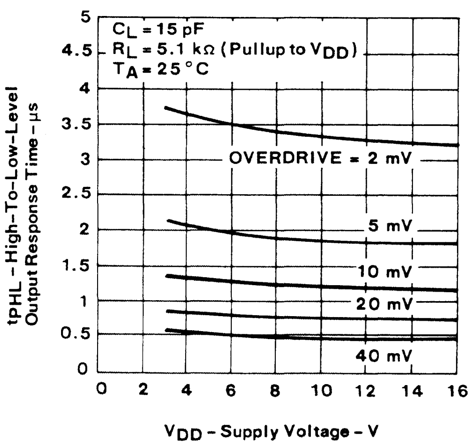


FIGURE 15

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

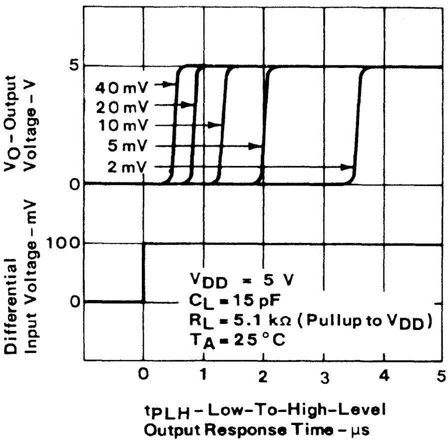


FIGURE 16

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

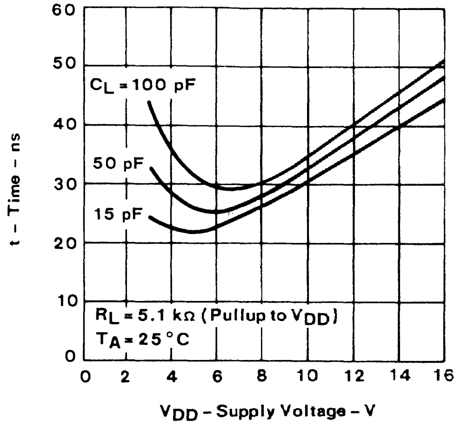


FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

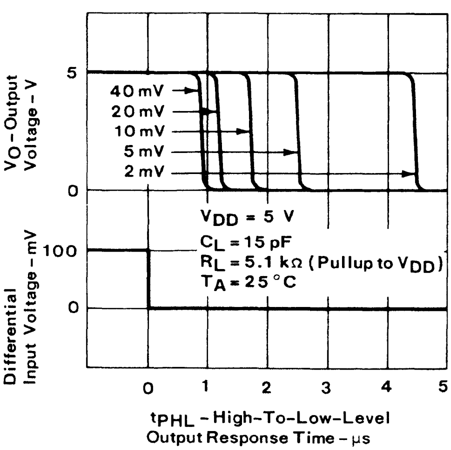


FIGURE 18

4
Voltage Comparators

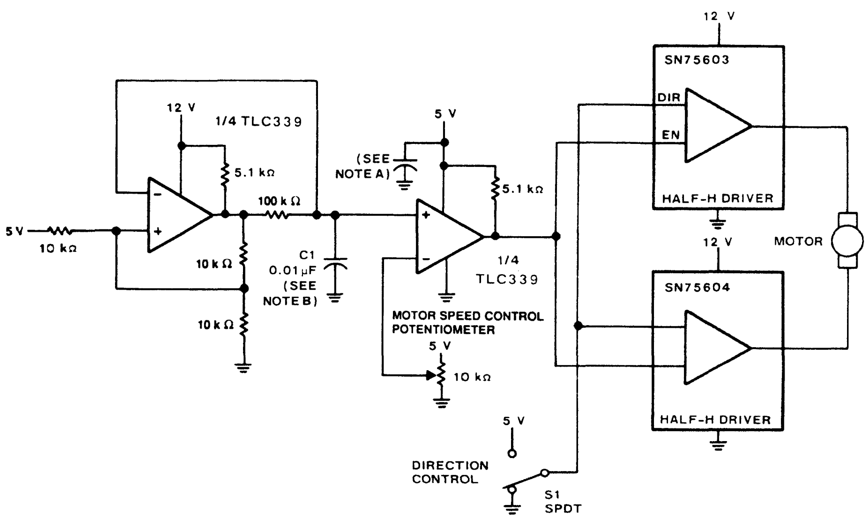
TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between −0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 milliamperes; however, the total current to ground can only be an absolute maximum of 60 milliamperes. This prohibits sinking 20 milliamperes from each of the four outputs simultaneously since the total current to ground would be 80 milliamperes.

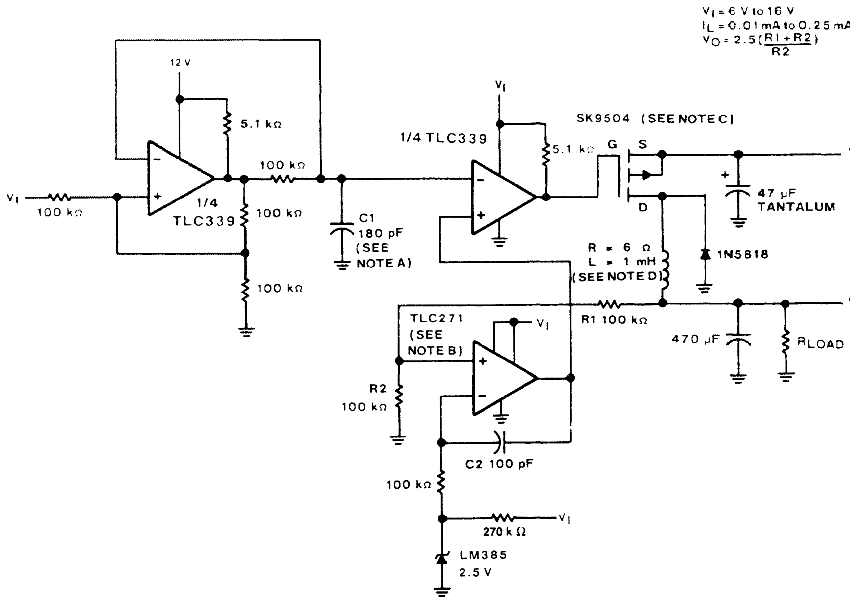
The TLC339 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

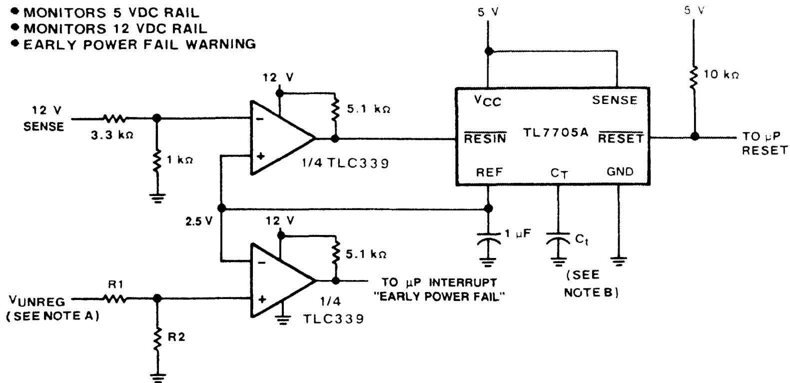
TYPICAL APPLICATION DATA



NOTES: A. Select C1 for a change in oscillator frequency.
B. TLC271 – Tie pin 8 to pin 7 for low bias operation.
C. SK9504 – $V_{DS} = 40$ V
$I_{DS} = 1$ A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

FIGURE 20. MICROPOWER SWITCHING REGULATOR

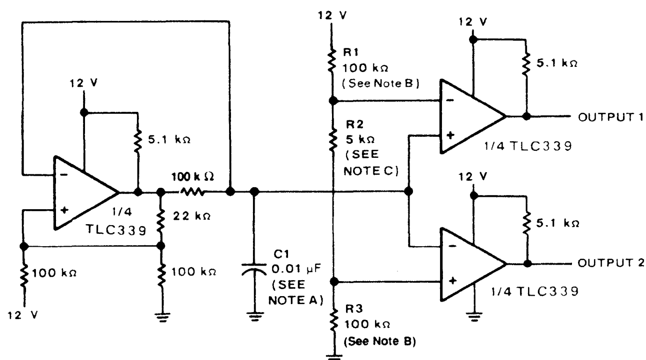
TYPICAL APPLICATION DATA

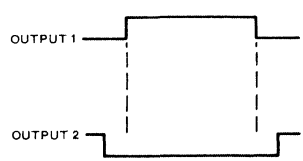


NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1+R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 21. ENHANCED SUPPLY SUPERVISOR





NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85(100\,k\Omega)C1$

B. Select R1 and R3 to change duty cycle.

C. Select R2 to change deadtime.

FIGURE 22. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

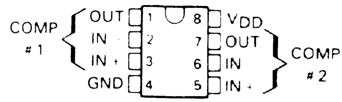
4 Voltage Comparators

TLC3702M, TLC3702I, TLC3702C
DUAL MICROPOWER LinCMOS™ COMPARATORS

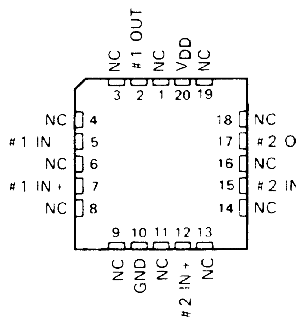
NOVEMBER 1986

- Push-Pull CMOS Output Drives Capacitive Loads without Pull-up Resistor, $I_O = \pm 8$ mA
- Very Low Power ... 100 μW Typ at 5 V
- Fast Response Time ... 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  TLC3702M ... 4 V to 16 V
  TLC3702I ... 3 V to 16 V
  TLC3702C ... 3 V to 16 V
- High Input Impedance ... 10^{12} Ω Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC3702M ... JG PACKAGE
TLC3702I ... D, JG, OR P PACKAGE
TLC3702C ... D, JG, OR P PACKAGE
(TOP VIEW)



TLC3702M ... FK PACKAGE
(TOP VIEW)

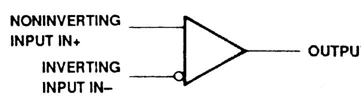


NC – No internal connection

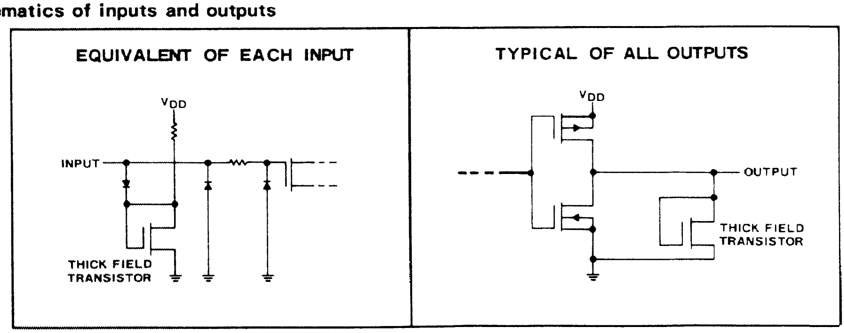
description

The TLC3702 consists of two independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

symbol (each comparator)



schematics of inputs and outputs



LinCMOS is a trademark of Texas Instruments

Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3702M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC3702I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . −0.3 V to 18 V
Differential input voltage (see Note 2) . . . . ±18 V
Input voltage, V_I . . . . −0.3 V to V_{DD}
Output voltage, V_O . . . . −0.3 V to V_{DD}
Input current, I_I . . . . ±5 mA
Output current, I_O (each output) . . . . ±20 mA
Total supply current into V_{DD} terminal . . . . 40 mA
Total current out of ground terminal . . . . 40 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . 725 mW
FK . . . . 1375 mW
JG package (alloy mount) 1025mW
JG package (glass mount) . . . . 825 mW
P package . . . . 725 mW
Operating free-air temperature range: TLC3702M . . . . −55°C to 125°C
TLC3702I . . . . −40°C to 85°C
TLC3702C . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or JG package . . . . . 300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For the TLC3702M in the JG package, use the alloy mount derating factor; for TLC3702I and TLC3702C in the JG package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
JG (alloy mount)	1050 mW	8.4 mW/°C	25°C
JG (glass mount)	825 mW	6.6 mW/°C	25°C
P	725 mW	5.8 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		83		
			-55°C		82		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			-55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	No load	25°C		18	40	μA
			Full range			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC3702M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			-40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (both comparators)	No load	25°C		18	40	μA
			Full range			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC3702I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}min$, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (both comparators)	No load	25°C		18	40	μA
			Full range			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC3702C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

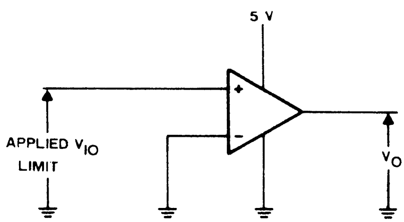
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.0		μs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+ pin			0.15		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		μs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.3		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_{TLH}	Transition time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

PARAMETER MEASUREMENT INFORMATION

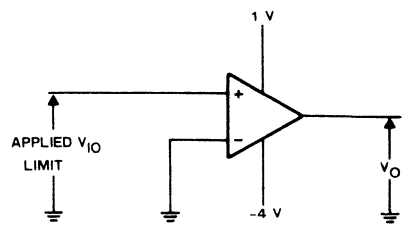
The TLC3702 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



a. V_{IO} with V_{IC} = 0 V



b. V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

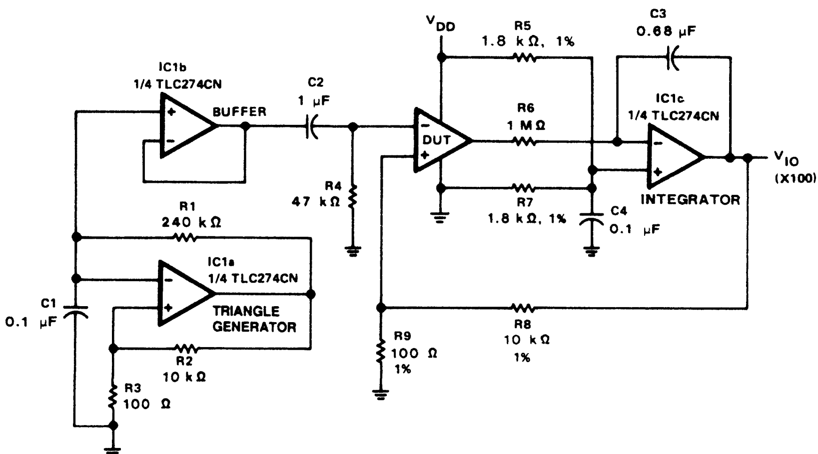


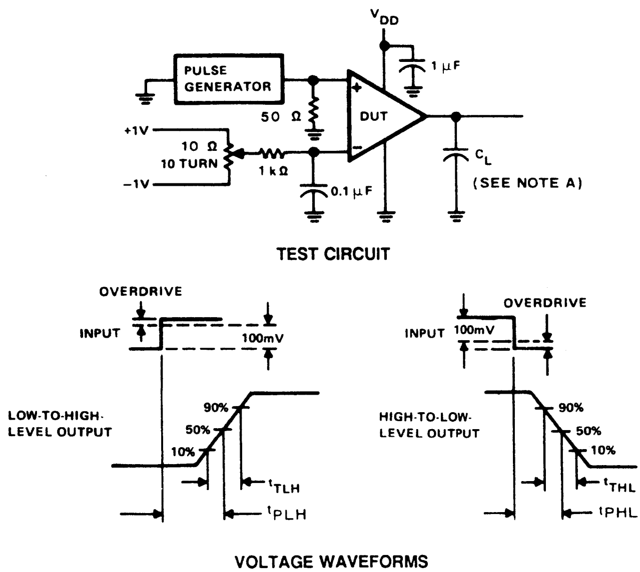
FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.

Rise time is defined as the time required for the output to change from 10% to 90% of its final value. Similarly, fall time is defined as the time required for the output voltage to change from 90% to 10% of its final value (see Figure 3).



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF INPUT OFFSET VOLTAGE

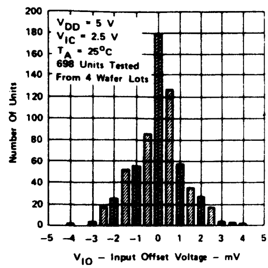


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

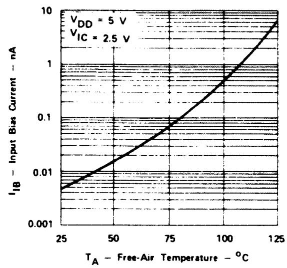


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

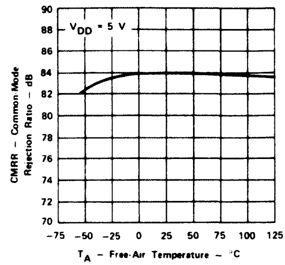


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

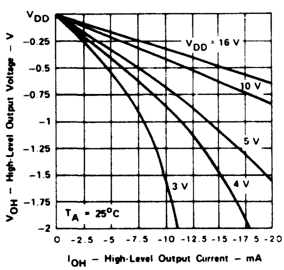


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

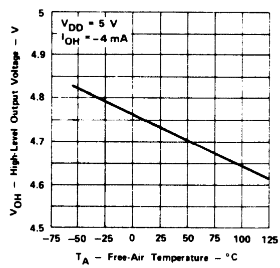


FIGURE 8

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

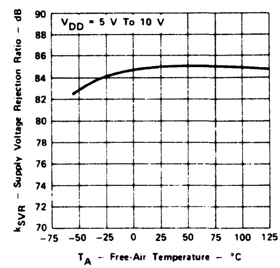


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

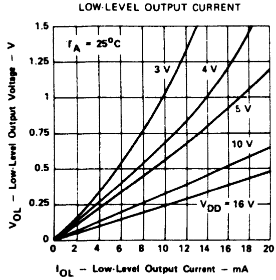


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

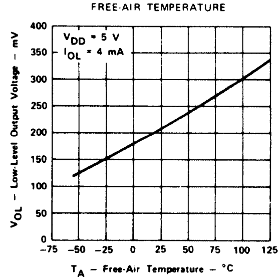


FIGURE 11

OUTPUT TRANSITION TIME vs LOAD CAPACITANCE

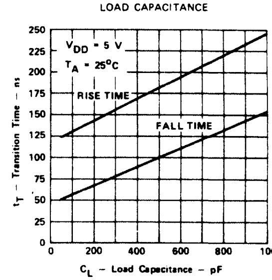


FIGURE 12

TYPICAL CHARACTERISTICS

SUPPLY CURRENT RESPONSE TO AN OUTPUT VOLTAGE TRANSITION

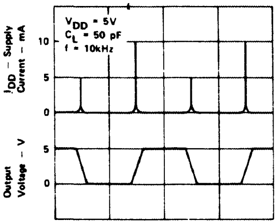


FIGURE 13

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

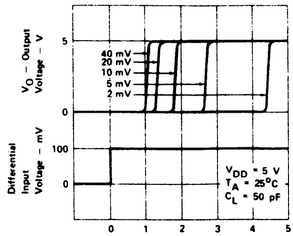


FIGURE 14

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

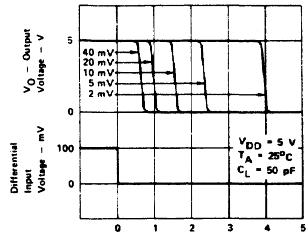


FIGURE 15

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE TIME vs SUPPLY VOLTAGE

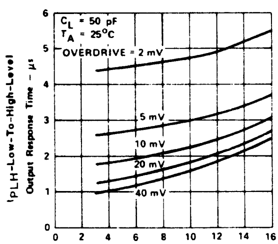


FIGURE 16

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE TIME vs SUPPLY VOLTAGE

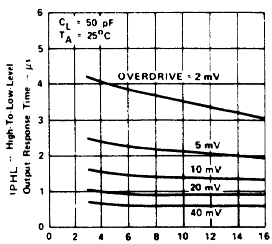


FIGURE 17

AVERAGE SUPPLY CURRENT (PER COMPARATOR) vs FREQUENCY

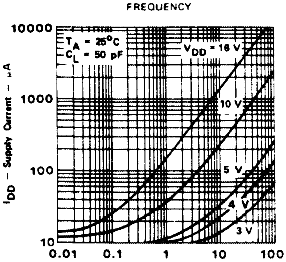


FIGURE 18

SUPPLY CURRENT vs SUPPLY VOLTAGE

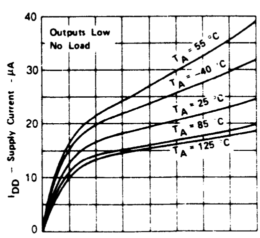


FIGURE 19

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

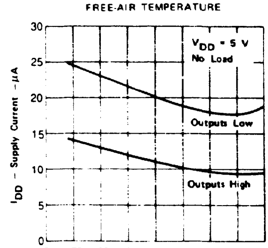


FIGURE 20

4

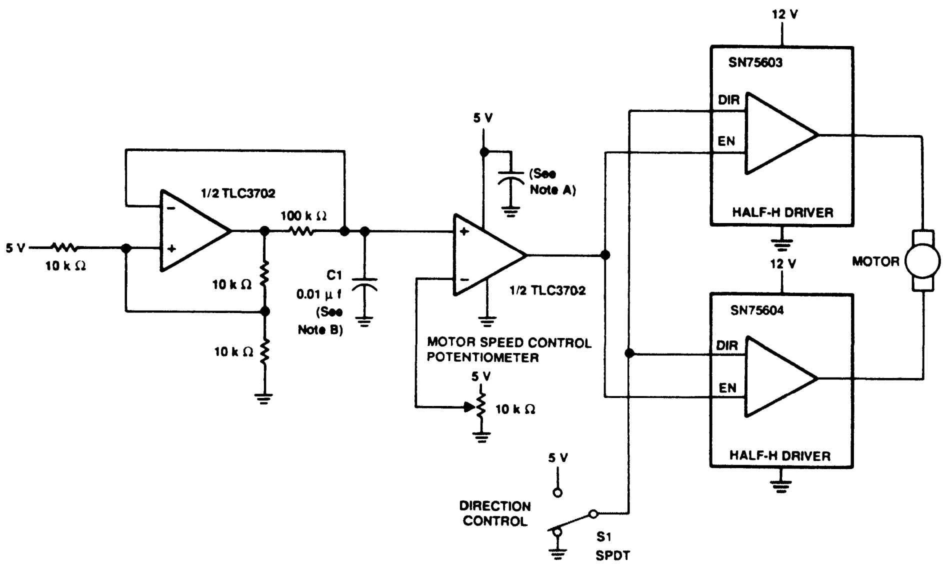
Voltage Comparators

TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

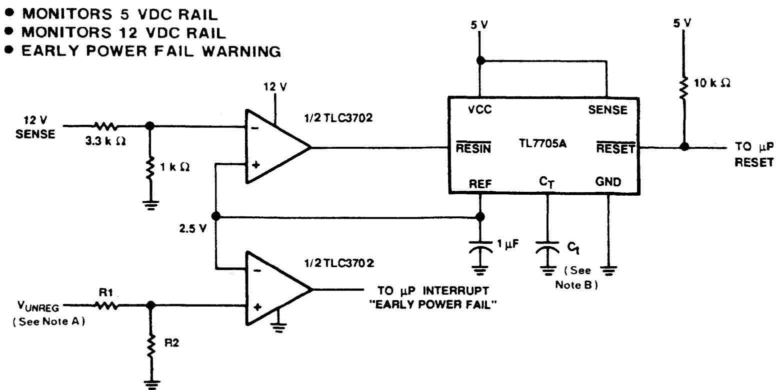
The TLC3702 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



NOTES A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frenquency

FIGURE 21. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

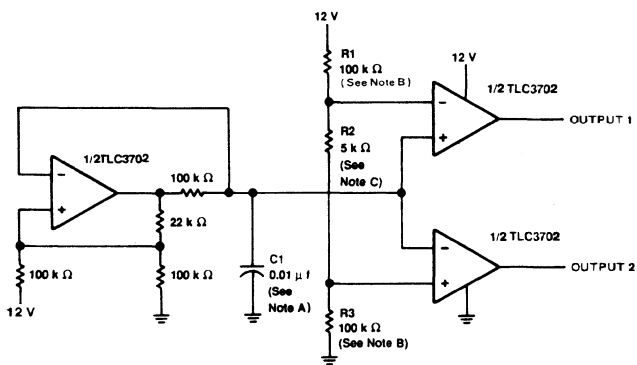
TYPICAL APPLICATION DATA

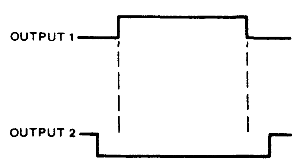


NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1 + R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 22. ENHANCED SUPPLY SUPERVISOR





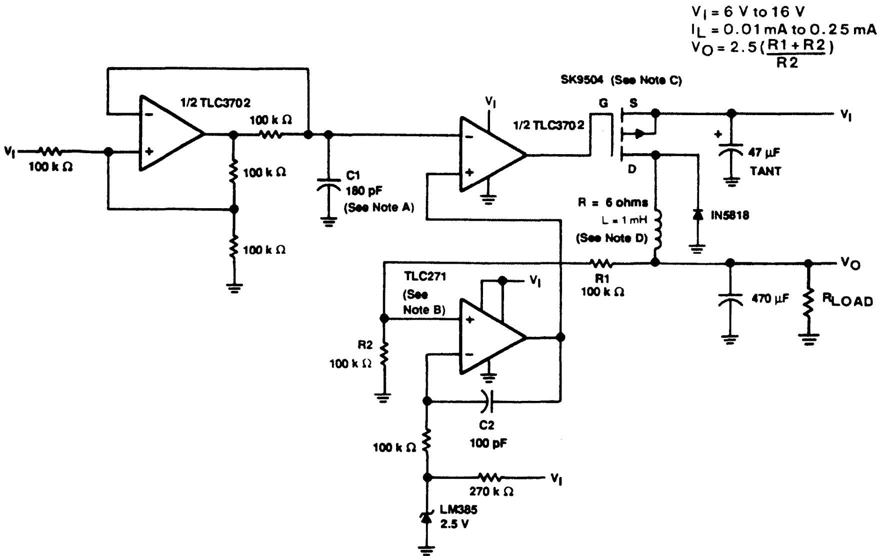
NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\ k\Omega)C1$

B. Adjust R1 and R3 to change duty cycle

C. Adjust R2 to change deadtime

FIGURE 23. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TYPICAL APPLICATION DATA



NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 — Tie pin 8 to pin 7 for low bias operation
C. SK9504 — VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

FIGURE 24. MICROPOWER SWITCHING REGULATOR

4 Voltage Comparators

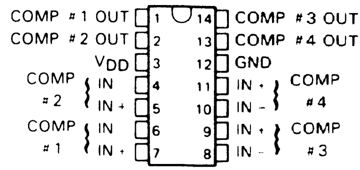
TEXAS INSTRUMENTS

TLC3704M, TLC3704I, TLC3704C QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

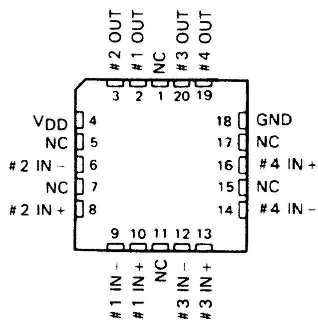
NOVEMBER 1986

- Push-Pull CMOS Output Drives Capacitive Loads without Pull-up Resistor, $I_O = \pm 8$ mA
- Very Low Power ... 200 μW Typ at 5 V
- Fast Response Time ... 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  TLC3704M ... 4 V to 16 V
  TLC3704I ... 3 V to 16 V
  TLC3704C ... 3 V to 16 V
- High Input Impedance ... 10^{12} Ω Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC3704M ... J PACKAGE
TLC3704I ... D, J, OR N PACKAGE
TLC3704C ... D, J, OR N PACKAGE
(TOP VIEW)



TLC3704M ... FK PACKAGE
(TOP VIEW)

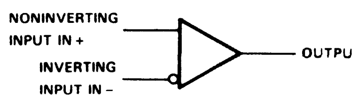


NC – No internal connection

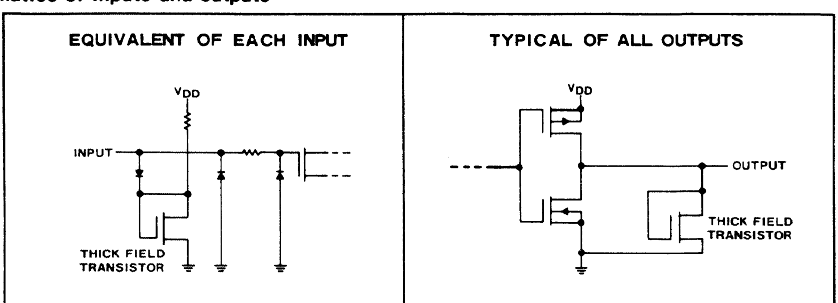
description

The TLC3704 consists of four independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

symbol (each comparator)



schematics of inputs and outputs



Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3704M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC3704I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC3704C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)		−0.3 V to 18 V
Differential input voltage (see Note 2)		±18 V
Input voltage, V_I		−0.3 V to V_{DD}
Output voltage, V_O		−0.3 V to V_{DD}
Input current, I_I		±5 mA
Output current, I_O (each output)		±20 mA
Total supply current into V_{DD} terminal		40 mA
Total current out of ground terminal		60 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	D package	950 mW
	FK or J package (alloy mount)	1375 mW
	J package (glass mount)	1025 mW
	N package	875 mW
Operating free-air temperature range:	TLC3704M	−55°C to 125°C
	TLC3704I	−40°C to 85°C
	TLC3704C	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or J package		300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For TLC3704M in the J package, use the alloy mount derating factor; for TLC3704I and TLC3704C in the J package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
J (alloy mount)	1375 mW	11 mW/°C	25°C
J (glass mount)	1025 mW	6.6 mW/°C	25°C
N	875 mW	7 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		83		
			-55°C		82		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			-55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (four comparators)	No load	25°C		35	80	μA
			Full range			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC3704M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			-40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (four comparators)	No load	25°C		35	80	μA
			Full range			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC3704I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
High-level output current, I_{OH}		-8	-20	mA
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.2	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = -4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (four comparators)	No load	25°C		35	80	μA
			Full range			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC3704C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4,5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.0		μs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+ pin			0.15		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		μs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.3		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_{TLH}	Transition time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

4

Voltage Comparators

PARAMETER MEASUREMENT INFORMATION

The TLC3704 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

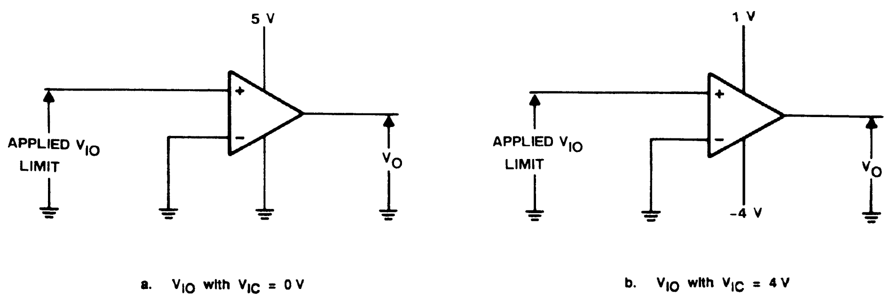


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

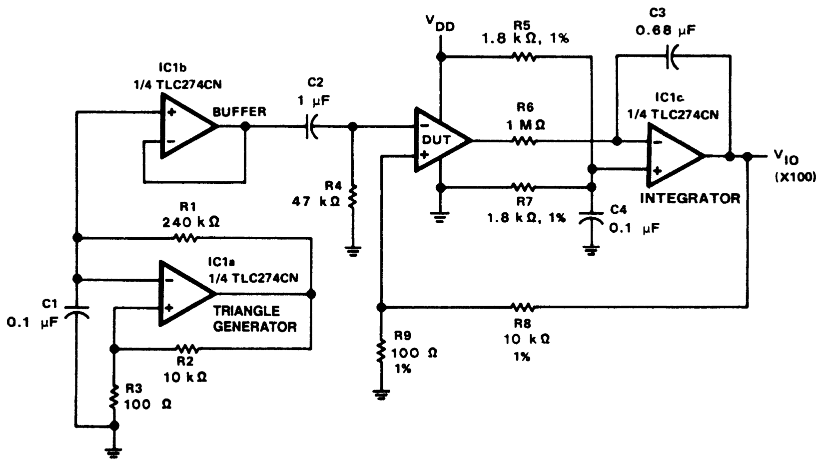


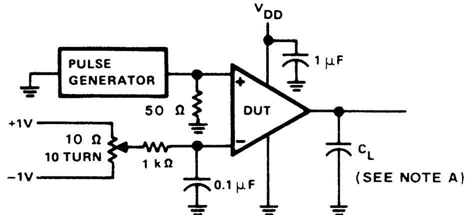
FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

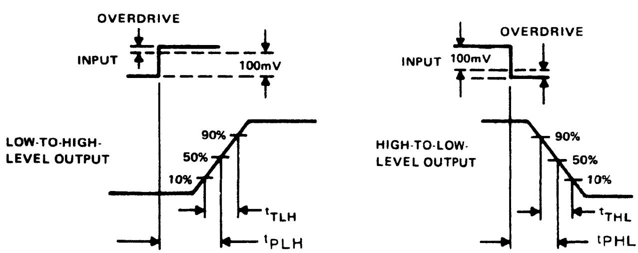
PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.

Rise time is defined as the time required for the output to change from 10% to 90% of its final value. Similarly, fall time is defined as the time required for the output voltage to change from 90% to 10% of its final value (see Figure 3).



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF INPUT OFFSET VOLTAGE

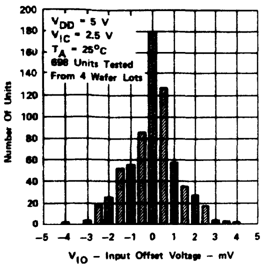


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

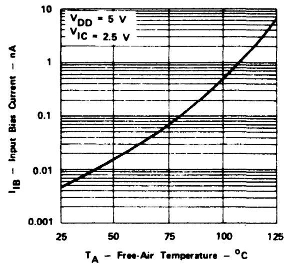


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

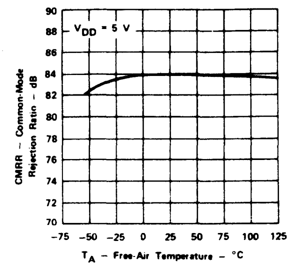


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

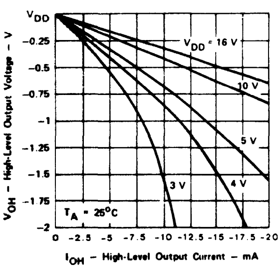


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

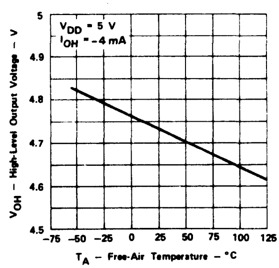


FIGURE 8

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

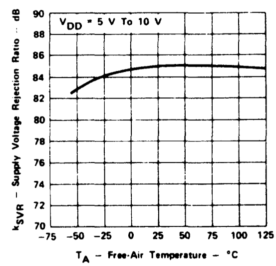


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

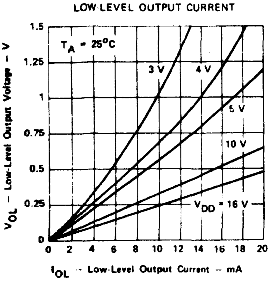


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

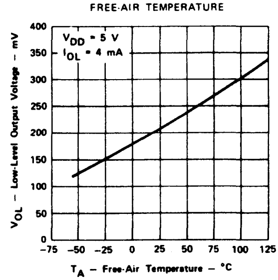


FIGURE 11

OUTPUT TRANSITION TIME vs LOAD CAPACITANCE

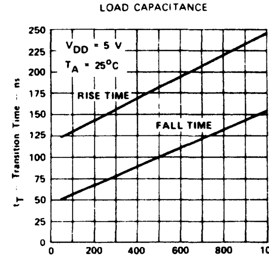


FIGURE 12

TYPICAL CHARACTERISTICS

SUPPLY CURRENT RESPONSE
TO AN OUTPUT VOLTAGE TRANSITION

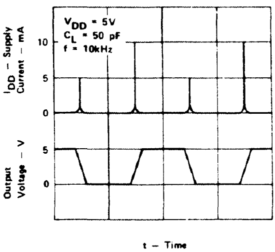


FIGURE 13

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

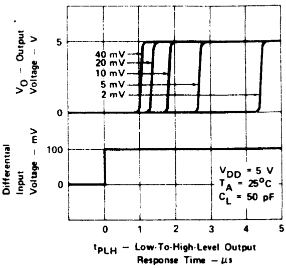


FIGURE 14

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

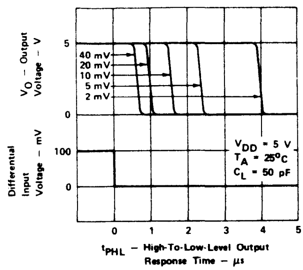


FIGURE 15

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

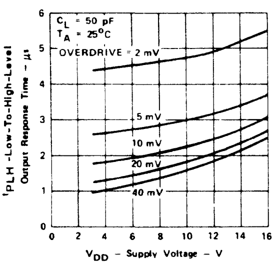


FIGURE 16

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

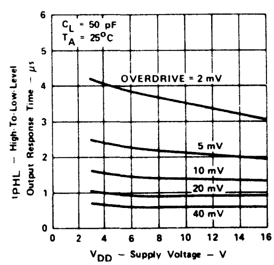


FIGURE 17

AVERAGE SUPPLY CURRENT
(PER COMPARATOR)
vs
FREQUENCY

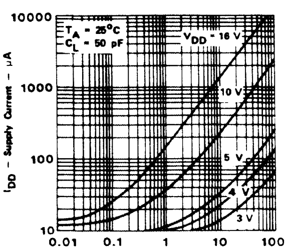


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

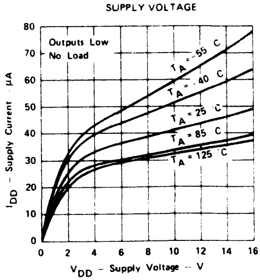


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

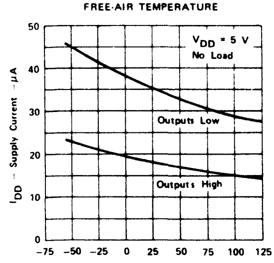


FIGURE 20

4
Voltage Comparators

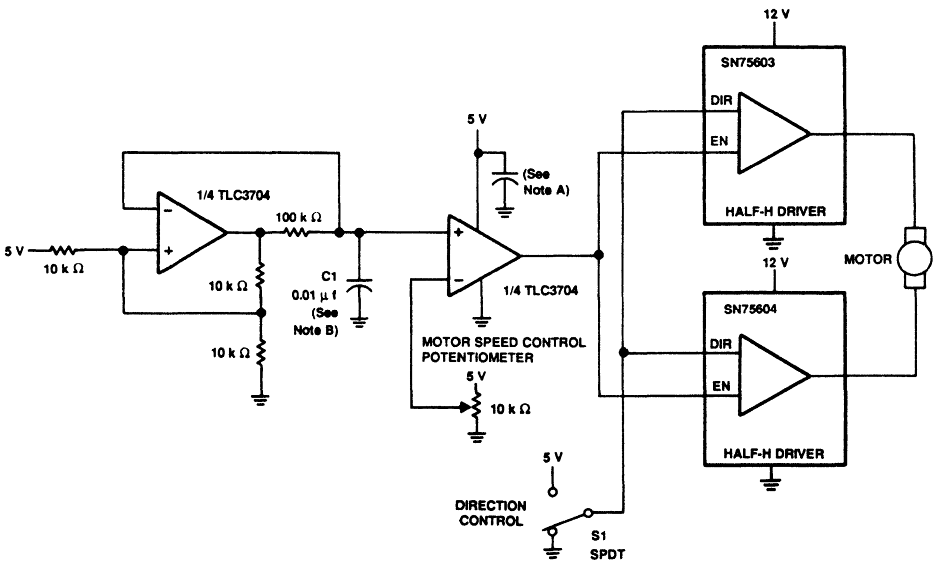
TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between −0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC3704 does not provide current protection. For example, each output can source or sink a maximum of 20 milliamperes; however, the total current to ground can only be an absolute maximum of 60 milliamperes. This prohibits sinking 20 milliamperes from each of the four outputs simultaneously since the total current to ground would be 80 milliamperes.

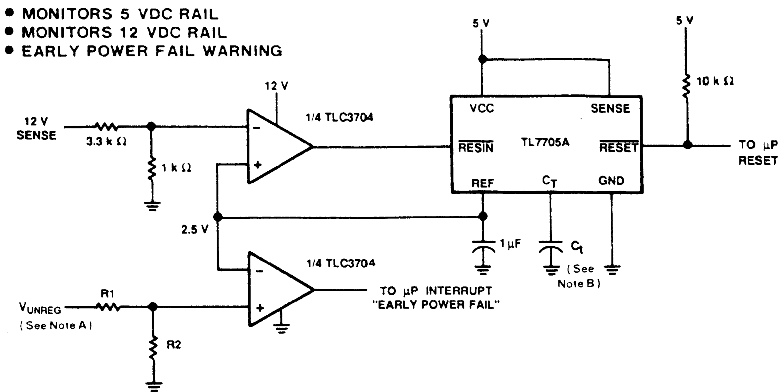
The TLC3704 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frenquency.

FIGURE 21. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

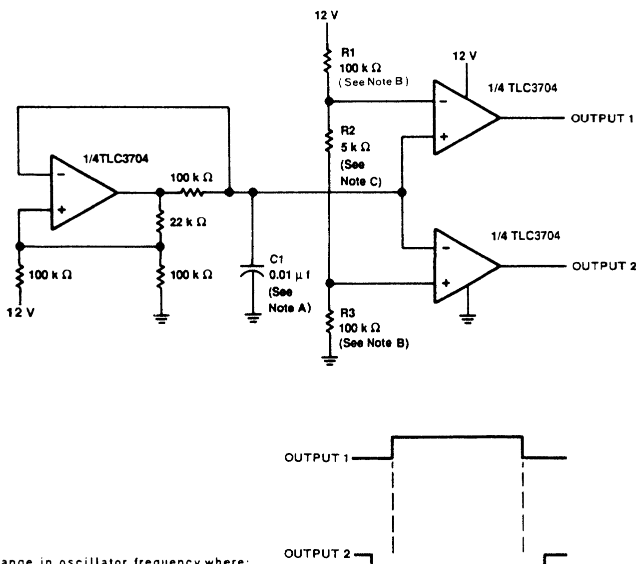
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1 + R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 22. ENHANCED SUPPLY SUPERVISOR



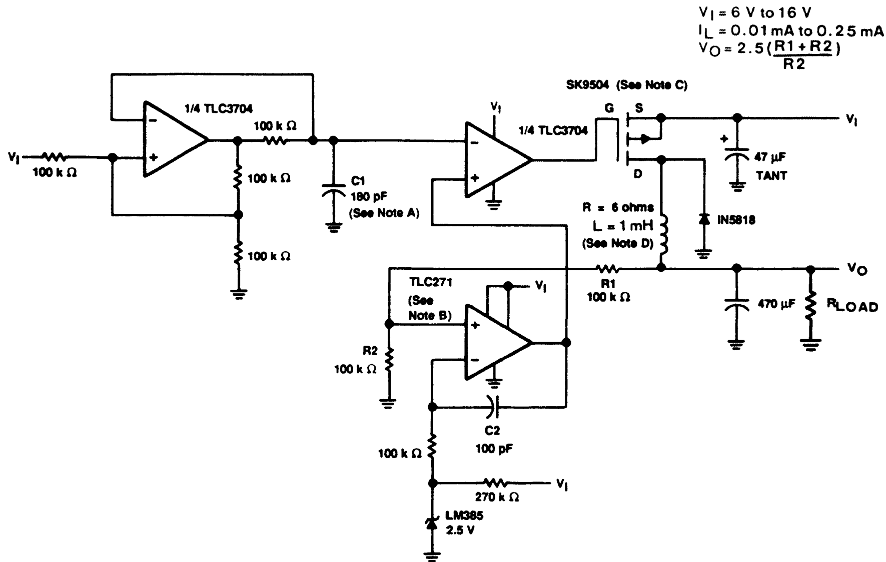
NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\,k\Omega)C1$

B. Adjust R1 and R3 to change duty cycle

C. Adjust R2 to change deadtime

FIGURE 23. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TYPICAL APPLICATION DATA



NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 — Tie pin 8 to pin 7 for low bias operation
C. SK9504 — VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

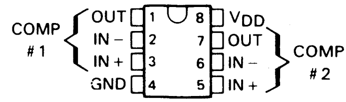
FIGURE 24. MICROPOWER SWITCHING REGULATOR

LinCMOS™ DUAL DIFFERENTIAL COMPARATORS

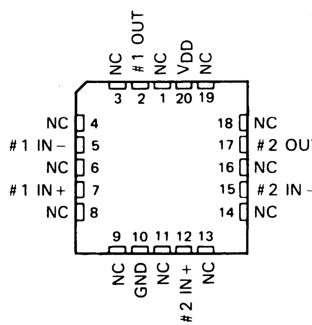
D2821, NOVEMBER 1983—REVISED OCTOBER 1985

- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 2 V to 18 V**
- **Very Low Supply Current Drain 0.3 mA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM393**

TLC372M . . . JG
TLC372I, TLC372C . . . D, JG, OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

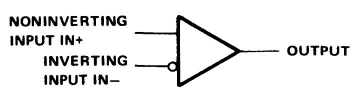


TLC372M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each device features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-volt ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372I is characterized for operation from −40°C to 85°C. The TLC372C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)		18 V
Differential input voltage, V_{ID} (see Note 2)		±18 V
Input voltage, V_I		V_{DD}
Output voltage, V_O		18 V
Output current, I_O		20 mA
Duration of output short-circuit to ground (see Note 3)		unlimited
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)		300 mW
Free-air temperature range:	TLC372M	−55°C to 125°C
	TLC372I	−40°C to 85°C
	TLC372C	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, FK or JG package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package		260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.
4. For operation of the TLC372M in the JG package above 114°C free-air temperature, derate linearly at the rate of 8.4 mW/°C to 210 mW at 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC372M			TLC372I			TLC372C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min,	See Note 5	25°C		2	10		2	10		2	10	mV
				Full range			12			13			12	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			V
				Full range	0 to $V_{DD}-2$			0 to $V_{DD}-2$			0 to $V_{DD}-2$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		0.3	0.75		0.3	0.75		0.3	0.75	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC372M, 0°C to 70°C for TLC372C, and −40°C to 85°C for TLC372I. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The TLC372 must not be tested in the servo-loop configuration often used for operational amplifiers. This device has a digital output stage. Attempts to force the device into the linear region of the transfer curve can cause damage. Test equipment should operate in accordance with the following recommendations and no attempt should be made to measure the gain of the device on an automatic tester.

To verify that V_{IO} falls within the limits specified, the limit value is applied to the input as shown in Figure 1. With IN+ positive with respect to IN−, the output should be high. With the input polarity reversed, the output should be low. If it is desired to measure the actual value of V_{IO}, a binary search method can be used to vary the input potential and check the output states until a good approximation of the critical point is obtained.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current or, at least, compensating for the leakage of test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket and the reading subtracted from that obtained with a device in the socket.

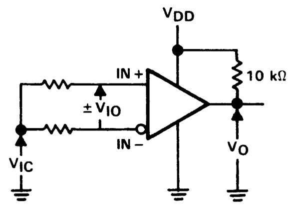


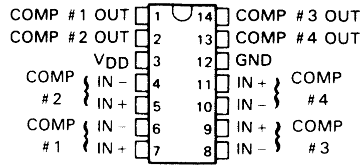
FIGURE 1. TEST CIRCUIT

LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATOR

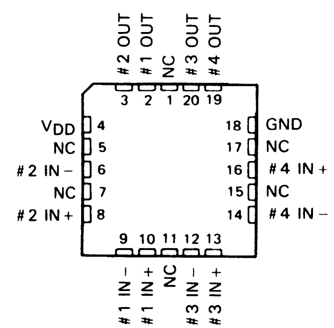
D2783, NOVEMBER 1983—REVISED OCTOBER 1985

- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 2 V to 18 V**
- **Very Low Supply Current Drain 0.6 mA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM339**

TLC374M . . . J
TLC374I, TLC374C . . . D, J, OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



TLC374M . . . FK PACKAGE
(TOP VIEW)

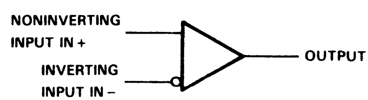


NC—No internal connection

description

This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each device features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



The TLC374 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-volt ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC374M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC374I is characterized for operation from −40°C to 85°C. The TLC374C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	±18 V
Input voltage, V_I	V_{DD}
Output voltage, V_O	18 V
Output current, I_O	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)	300 mW
Free-air temperature range: TLC374M	−55°C to 125°C
TLC374I	−40°C to 85°C
TLC374C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, J or FK package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or N package	260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.
4. For operation of the TLC374M in the J package above 114°C free-air temperature, derate linearly at the rate of 8.4 mW/°C to 210 mW at 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC374M MIN	TLC374M TYP	TLC374M MAX	TLC374I MIN	TLC374I TYP	TLC374I MAX	TLC374C MIN	TLC374C TYP	TLC374C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min,	See Note 5	25°C		2	10		2	10		2	10	mV
				Full range			12			13			12	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			0 to $V_{DD}-1.75$			V
				Full range	0 to $V_{DD}-2$			0 to $V_{DD}-2$			0 to $V_{DD}-2$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		0.6	1		0.6	1		0.6	1	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC374M, −40°C to 85°C for TLC374I, and 0°C to 70°C for TLC374C. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The TLC374 must not be tested in the servo-loop configuration often used for operational amplifiers. This device has a digital output stage. Attempts to force the device into the linear region of the transfer curve can cause damage. Test equipment should operate in accordance with the following recommendations and no attempt should be made to measure the gain of the device on an automatic tester.

To verify that V_{IO} falls within the limits specified, the limit value is applied to the input as shown in Figure 1. With IN+ positive with respect to IN−, the output should be high. With the input polarity reversed, the output should be low. If it is desired to measure the actual value of V_{IO}, a binary search method can be used to vary the input potential and check the output states until a good approximation of the critical point is obtained.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current or, at least, compensating for the leakage of test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket and the reading subtracted from that obtained with a device in the socket.

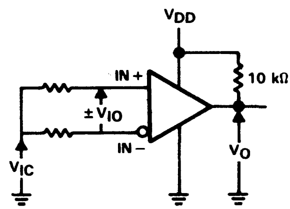


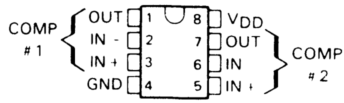
FIGURE 1. TEST CIRCUIT

TLC393M, TLC393I, TLC393C DUAL MICROPOWER LinCMOS™ COMPARATORS

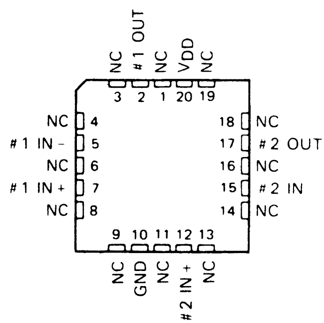
DECEMBER 1986

- Very Low Power . . . 100 μW Typ at 5 V
- Fast Response Time . . . 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:
  - TLC393M . . . 4 V to 16 V
  - TLC393I . . . 3 V to 16 V
  - TLC393C . . . 3 V to 16 V
- High Input Impedance . . . $10^{12}\Omega$ Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

TLC393M . . . JG PACKAGE
TLC393I . . . D, JG, OR P PACKAGE
TLC393C . . . D, JG, OR P PACKAGE
(TOP VIEW)



TLC393M . . . FK PACKAGE
(TOP VIEW)

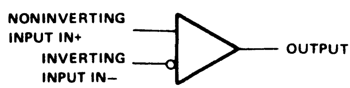


NC – No internal connection

description

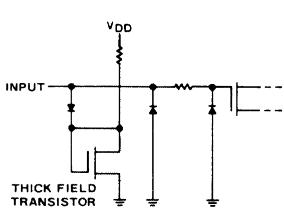
The TLC393 consists of two independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3702 data sheet.

symbol (each comparator)

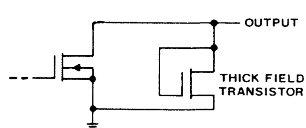


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



Texas Instruments LinCMOS process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC393M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC393I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC393C is characterized for operation over the commercial temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)		−0.3 V to 18 V
Differential input voltage (see Note 2)		±18 V
Input voltage, V_I		−0.3 V to V_{DD}
Output voltage, V_O		−0.3 V to V_{DD}
Input current, I_I		±5 mA
Output current, I_O (each output)		20 mA
Total supply current into V_{DD} terminal		40 mA
Total current out of ground terminal		40 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	D package	725 mW
	FK	1375 mW
	JG package (alloy mount)	1025mW
	JG package (glass mount)	825 mW
	P package	725 mW
Operating free-air temperature range:	TLC393M	−55°C to 125°C
	TLC393I	−40°C to 85°C
	TLC393C	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: FK or JG package		300°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or P package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. For the TLC393M in the JG package, use the alloy mount derating factor; for the TLC393I and TLC393C in the JG package, use the glass mount derating factor.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
JG (alloy mount)	1050 mW	8.4 mW/°C	25°C
JG (glass mount)	825 mW	6.6 mW/°C	25°C
P	725 mW	5.8 mW/°C	25°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		84		
			-55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			-55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			Full range			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -55°C to 125°C for the TLC393M.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	-40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			84°C		84		
			-40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			-40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			Full range			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is -40°C to 85°C for the TLC393I.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	-0.2		V_{DD}-1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}min$, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			Full range			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}-1			V
			Full range	0 to V_{DD}-1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = -1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			Full range			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC393C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching charactistics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Response time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		μs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+ pin			0.10		
t_{PLH}	Response time, low-to-high-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		μs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.1		
t_{THL}	Transition time, high-to-low-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1a. With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1b for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

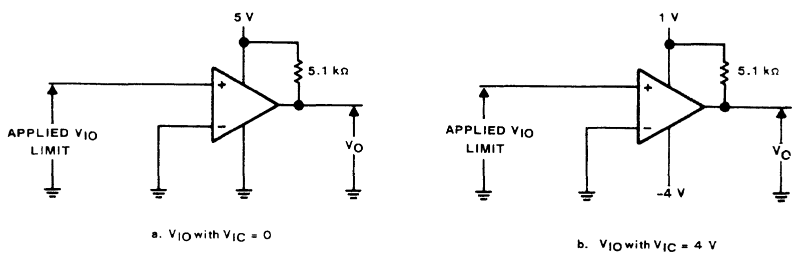


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct d.c. measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20 mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

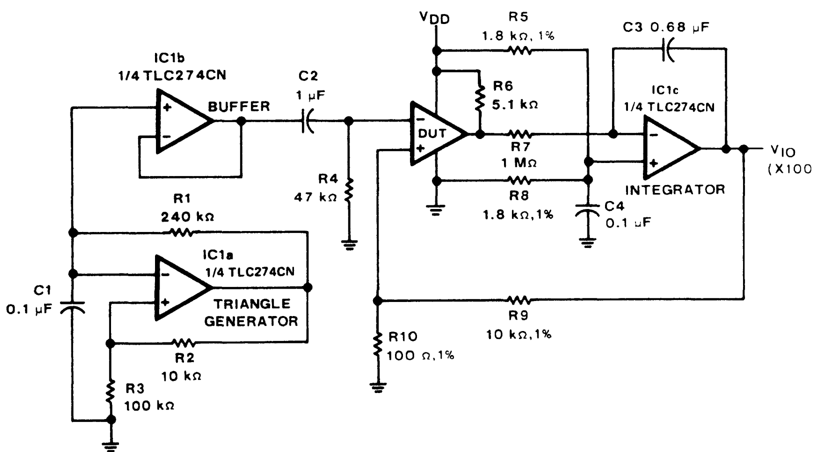
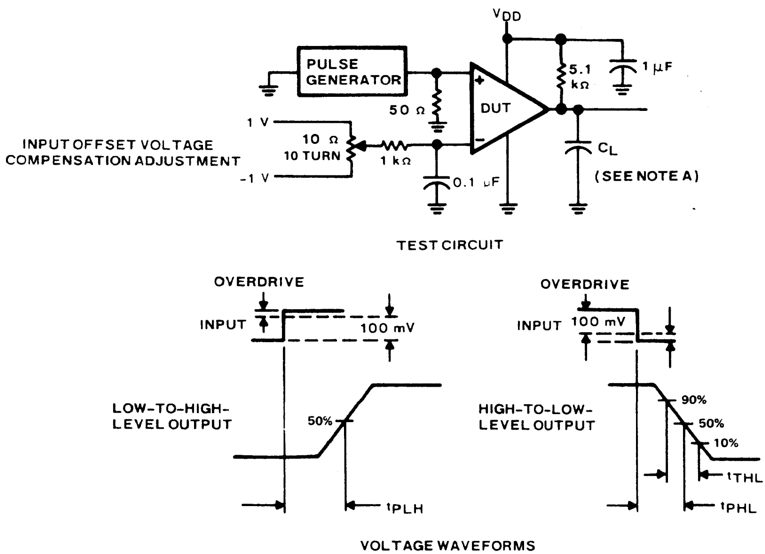


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

DISTRIBUTION OF INPUT OFFSET VOLTAGE

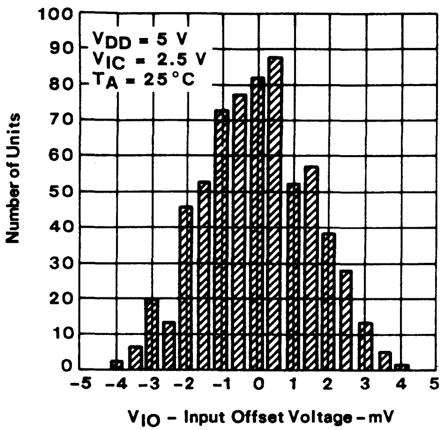


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

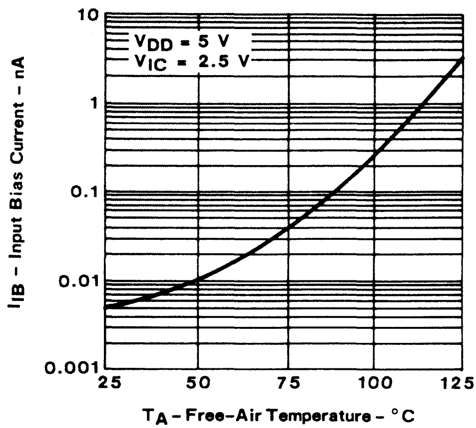


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

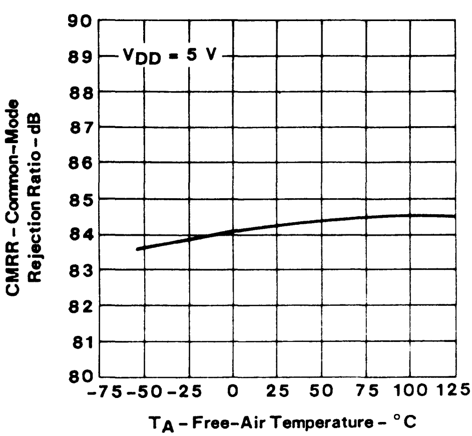


FIGURE 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

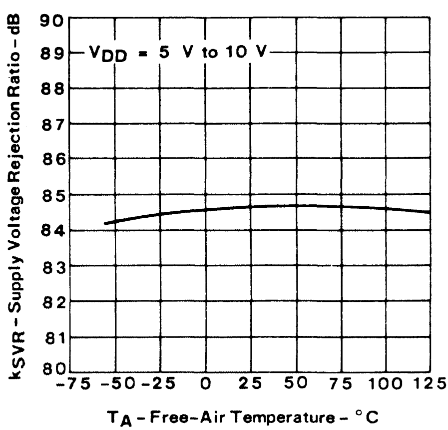


FIGURE 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

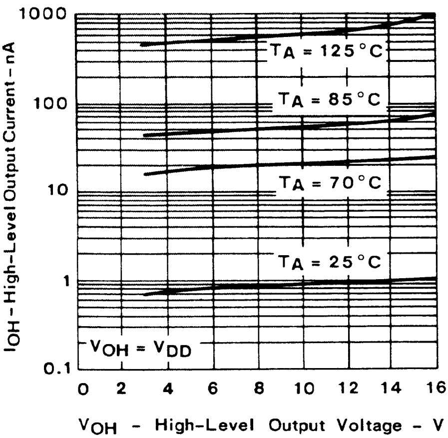


FIGURE 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

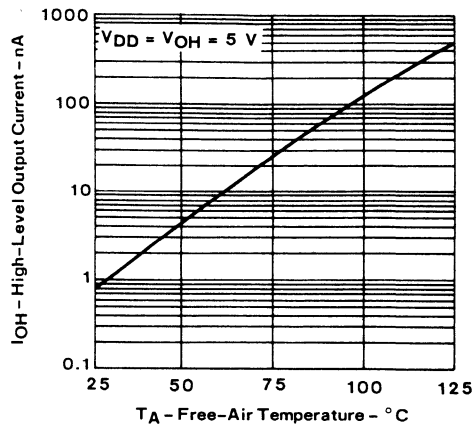


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

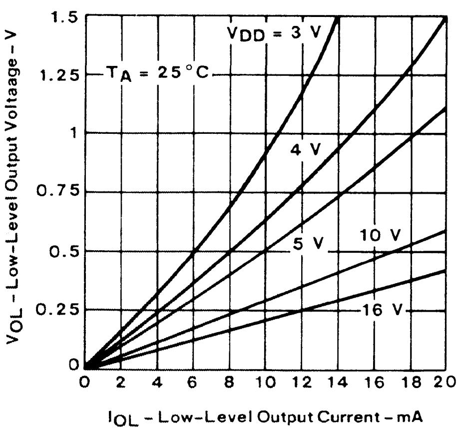


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

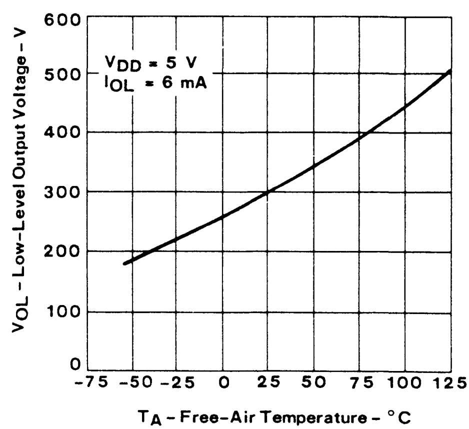


FIGURE 11

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

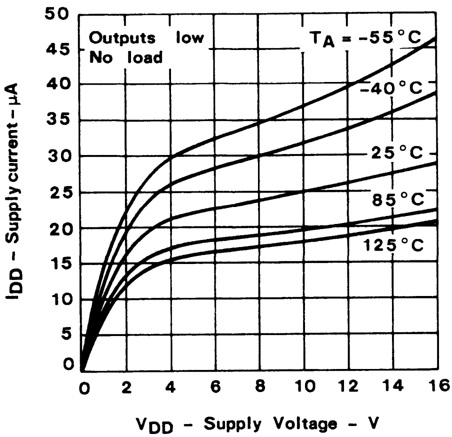


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

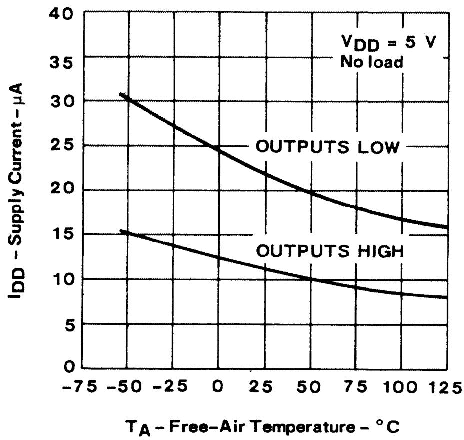


FIGURE 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

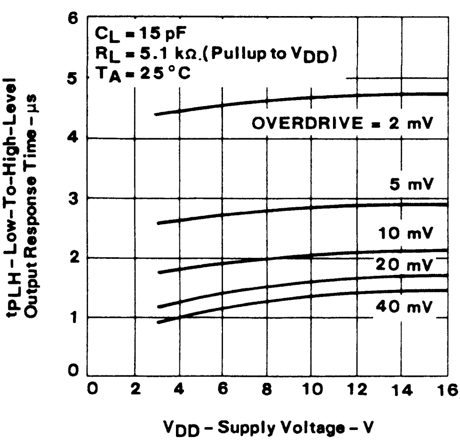


FIGURE 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

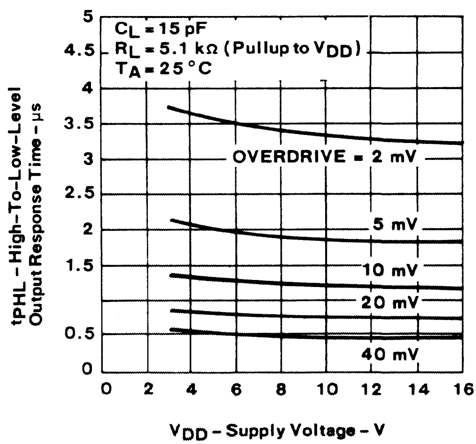


FIGURE 15

4 Voltage Comparators

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

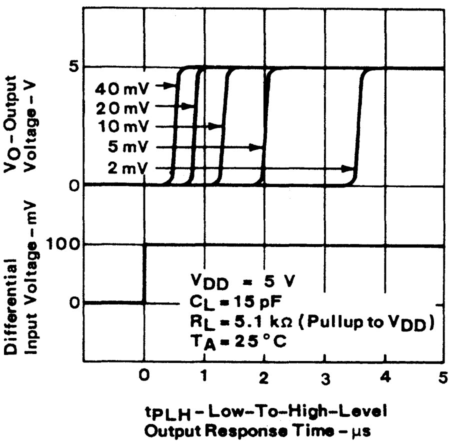


FIGURE 16

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

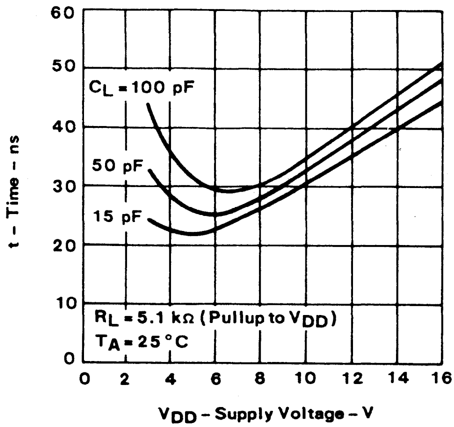


FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS OVERDRIVE VOLTAGES

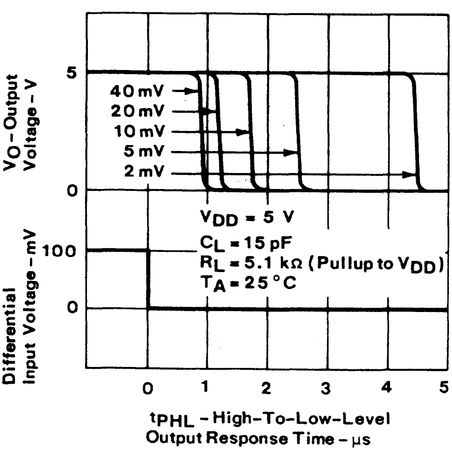


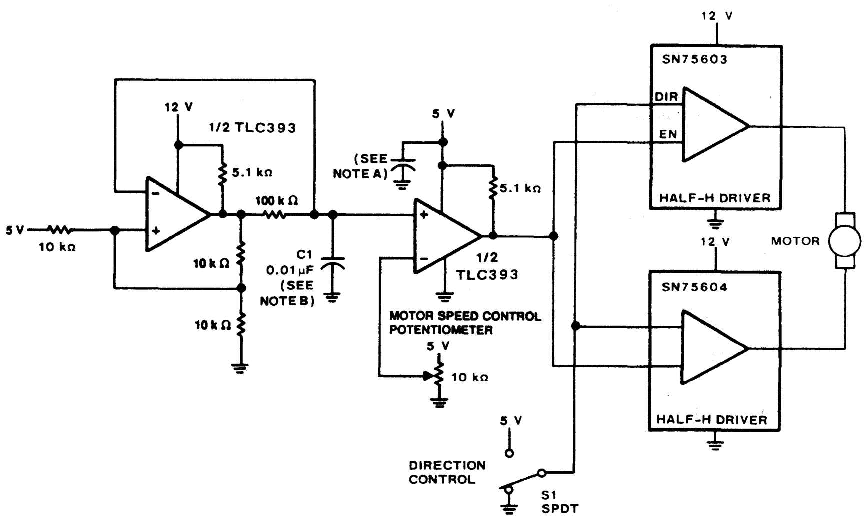
FIGURE 18

TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 milliamperes. to maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) positioned as close to the device as possible.

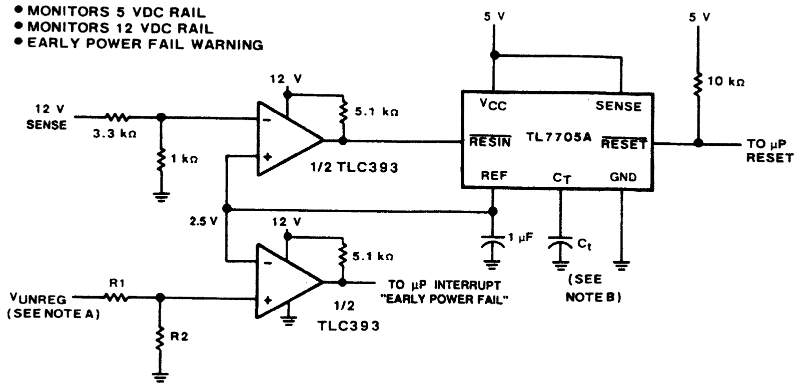
The TLC393 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

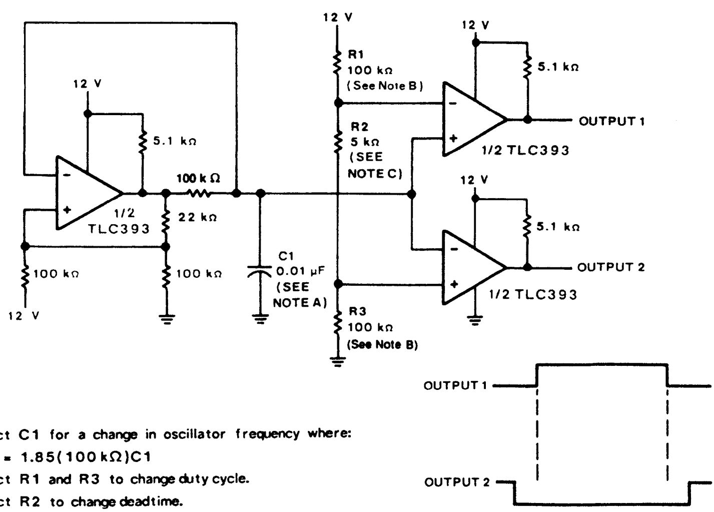
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1+R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 21. ENHANCED SUPPLY SUPERVISOR



NOTES: A. Select C1 for a change in oscillator frequency where:

$1/f = 1.85(100\,k\Omega)C1$

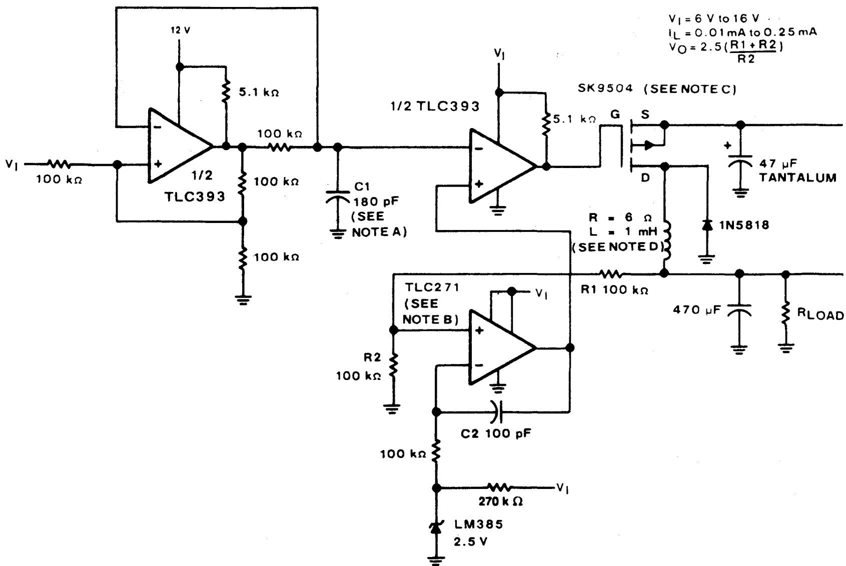
B. Select R1 and R3 to change duty cycle.

C. Select R2 to change deadtime.

FIGURE 22. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

4 Voltage Comparators

TYPICAL APPLICATION DATA



NOTES: A. Select C1 for a change in oscillator frequency.
B. TLC271 – Tie pin 8 to pin 7 for low bias operation.
C. SK9504 – V_{DS} = 40 V
I_{DS} = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

FIGURE 20. MICROPOWER SWITCHING REGULATOR

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

EXAMPLE: TL 062M JG /883B

1. Prefix

MUST CONTAIN TWO OR THREE LETTERS

- TL . . . . TI Linear Products (Excluding Interface)
- TLC . . . . TI Linear Silicon-Gate CMOS Products
- SN . . . . . . TI Special Function or Interface Products

STANDARD SECOND-SOURCE PREFIXES

ADC	National	OP	PMI
LM	National	RC, RM or RV	Raytheon
MC	Motorola	SG	Silicon General
NE, SA, or SE	Signetics	μA	Fairchild

2. Unique Circuit Designator Including Temperature Range (If not already specified by the prefix)

MUST CONTAIN THREE TO SEVEN CHARACTERS
(From Individual Data Sheets)

Examples: 062M, 594I, 532AI, 78L05AC

3. Package

MUST CONTAIN ONE OR TWO LETTERS

D, FK, FN, J, JD, JG, KC, LP, N, P, U, or W
(From Pin-Connection Diagram on Individual Data Sheet)

4. MIL-STD-883B, Method 5004, Class B

OMIT/883B WHEN NOT APPLICABLE

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specifed by the customer (with possible additional costs), circuits will be shipped on the most practical carrier.

Dual-In-Line (D, J, JD, JG, N, P)
- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier
- Sectioned Cardboard Box
- Individual Cardboard Box

Plug-In (LP)
- Barnes Carrier
- Sectional Cardboard Box
- Individual Cardboard Box

Chip Carriers (FK, FN)
- Anti-Static Plastic Tubing

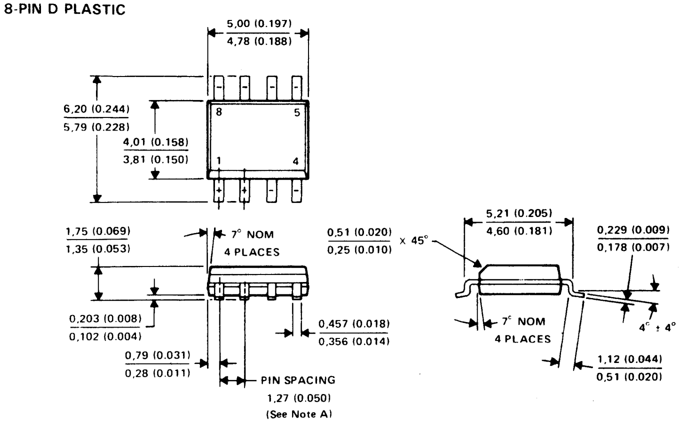
Flat (U, W)
- Barnes Carrier
- Milton Ross Carrier

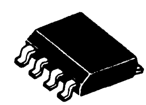
TO-220AB (KC)
- Sleeves

D plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

8-PIN D PLASTIC

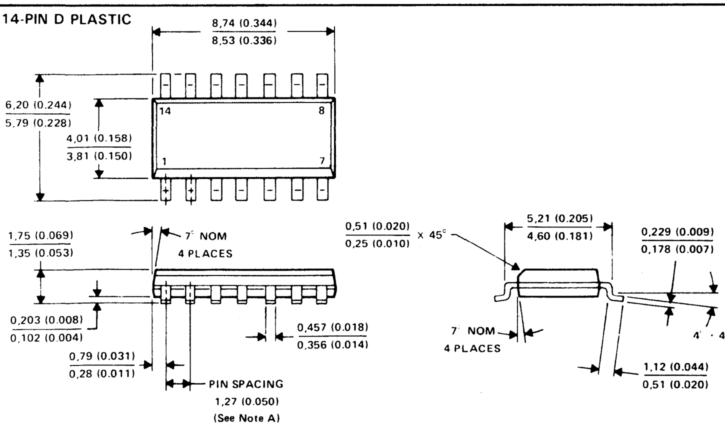


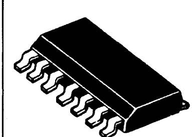


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

14-PIN D PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

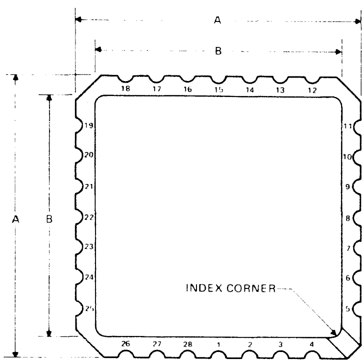
FK ceramic chip carrier package

This hermetically sealed chip carrier package has a ceramic base.
The FK package has a three-layer base with a metal lid and braze seal.

The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

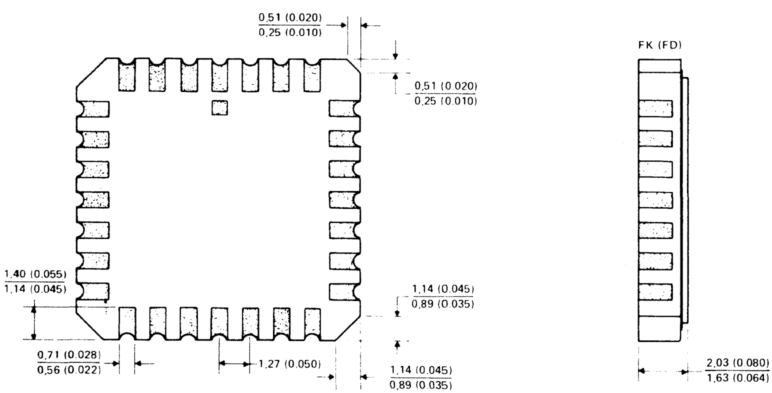
FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

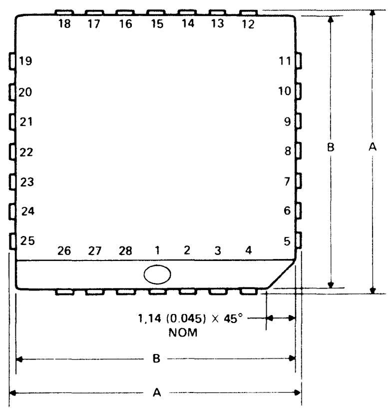
Appendix
A

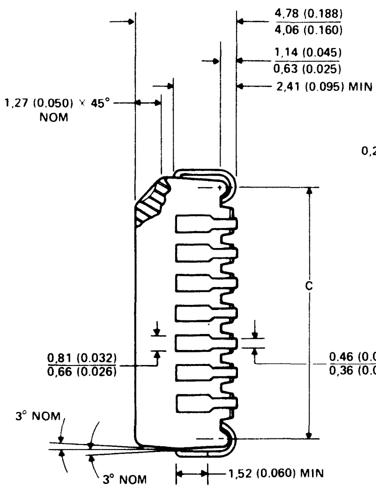
FN plastic chip carrier package

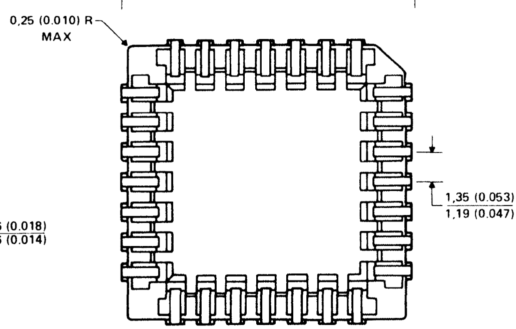
Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)





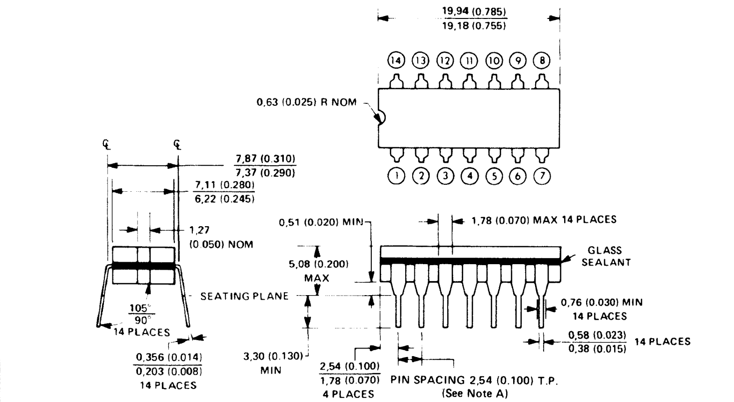


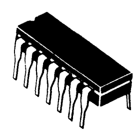
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

J ceramic dual-in-line packages

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldering assembly.

14-PIN J CERAMIC



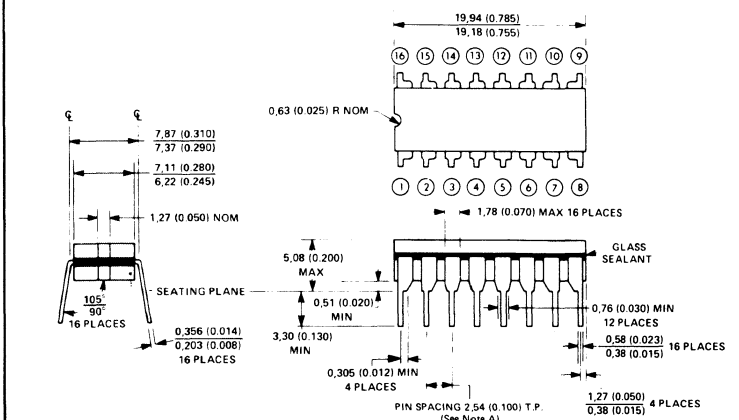


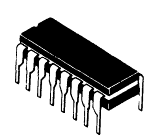
Falls Within JEDEC TO-116 and MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

16-PIN J CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

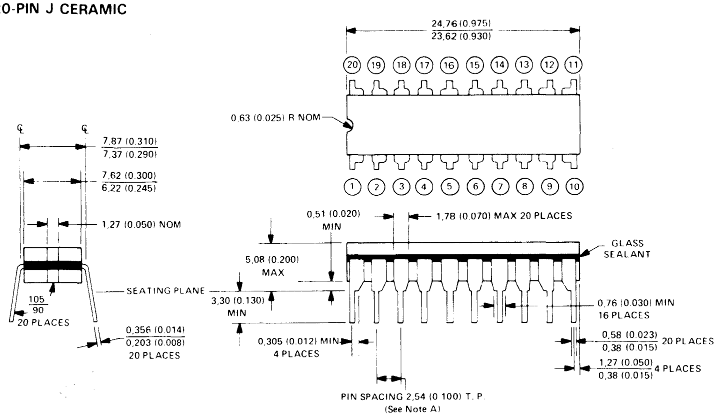
NOT TO SCALE

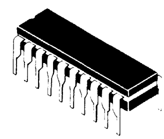
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Appendix

A

20-PIN J CERAMIC





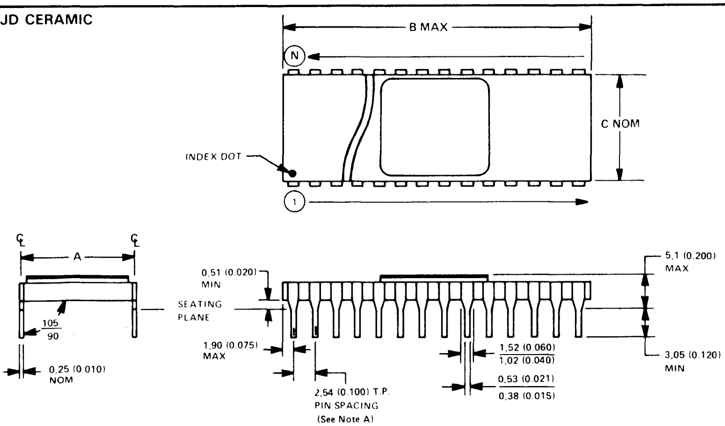
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

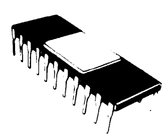
NOT TO SCALE

ceramic dual-in-line packages—side-braze (JD)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC





DIM \ PINS	28	40
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)
B MAX	36,8 (1.45)	52,1 (2.05)
C NOM	15,0 (0.590)	15.0 (0.590)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

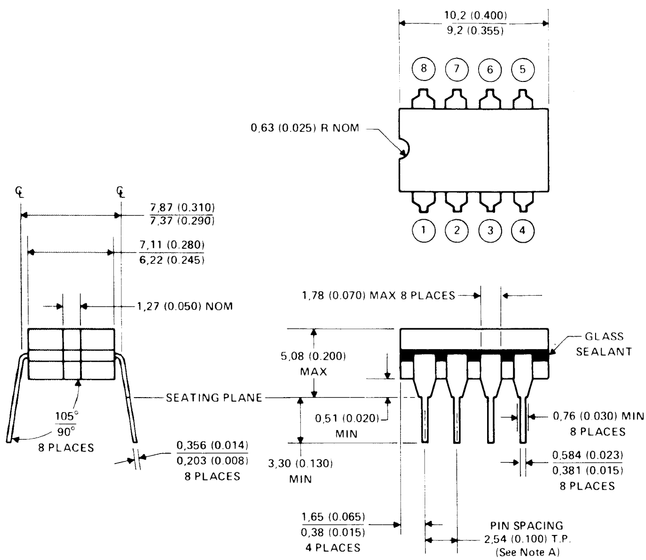
NOT TO SCALE

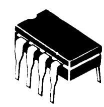
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. The package is intended for insertion in mounting-hole rows 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering.

8-PIN JG CERAMIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

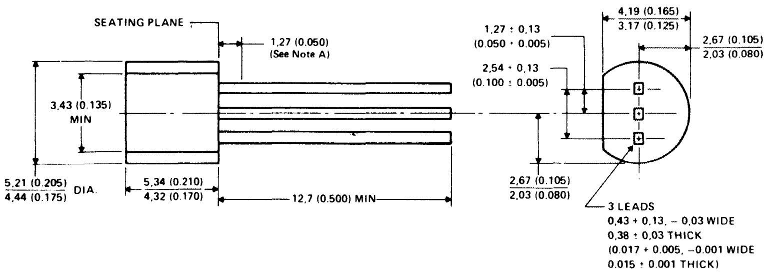
NOT TO SCALE

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

LP plastic package

These packages each consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LP PLASTIC



Falls Within JEDEC TO-226AA Dimensions
(TO-226AA Replaces TO-92)
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

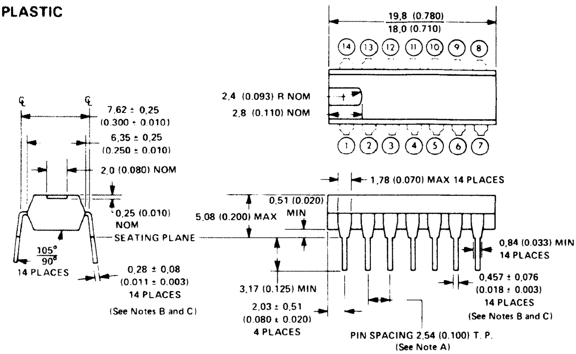
NOT TO SCALE

NOTE A: Lead dimensions are not controlled within this area.

N plastic dual-in-line package

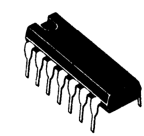
Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC



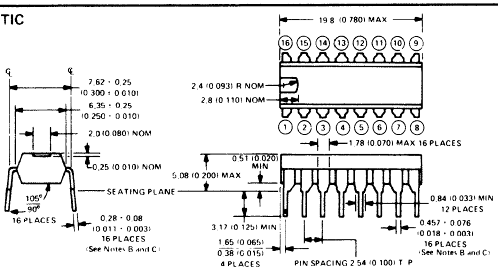
Falls Within JEDEC TO 116 and EIA MO 001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

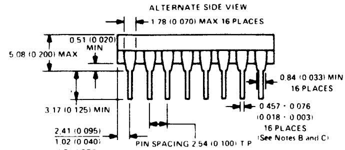


NOT TO SCALE

16-PIN N PLASTIC

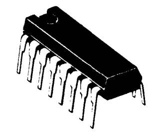


ALTERNATE SIDE VIEW



Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

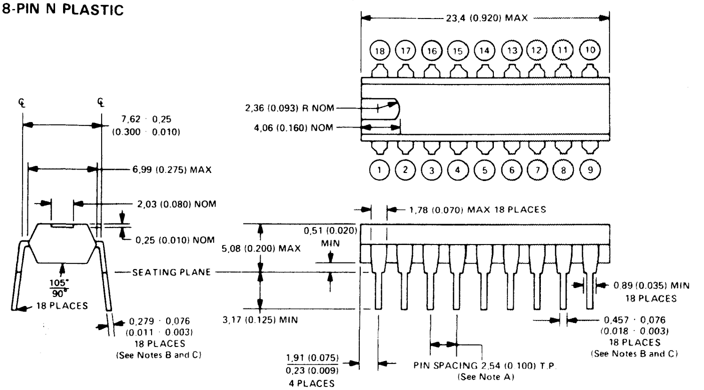


NOT TO SCALE

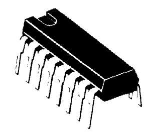
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

18-PIN N PLASTIC

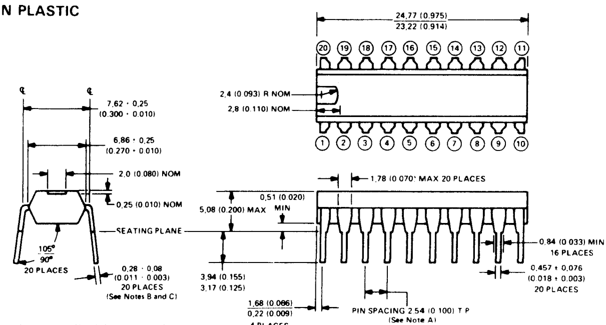


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



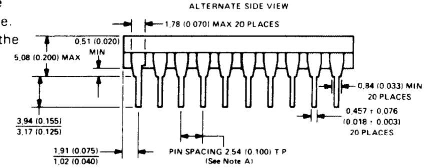
NOT TO SCALE

20-PIN N PLASTIC

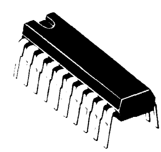


Parts may be supplied in accordance with the alternate side view at the option of TI plants locatd in Europe. In this case, the overall length of the package is 26,7 (1.050) max.

ALTERNATE SIDE VIEW



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

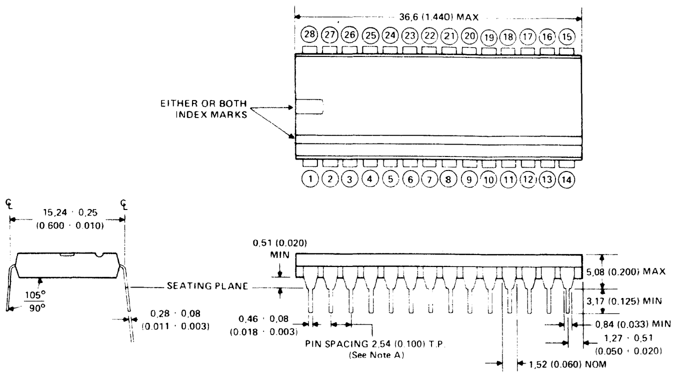


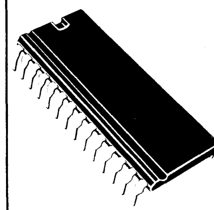
NOT TO SCALE

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic packages (continued)

28-PIN N PLASTIC

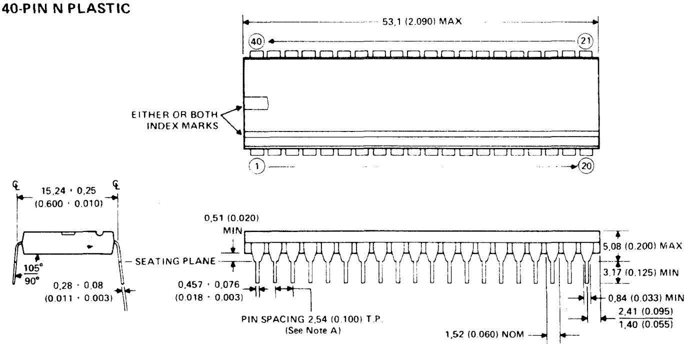


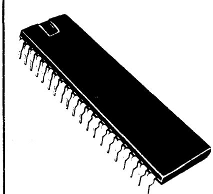


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

40-PIN N PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

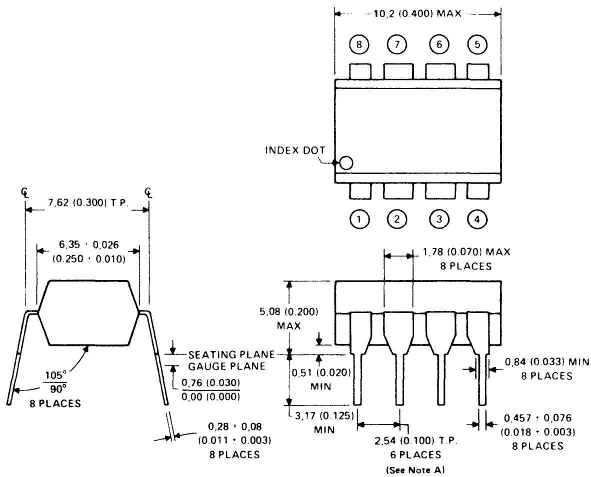
NOT TO SCALE

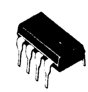
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics remain stable when operated under high-humidity conditions. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldering assembly.

8-PIN P PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

NOTE A: Each pin centerline is within 0,13 (0.005) radius of true position at the gauge plane with maximum material condition and unit installed.

Appendix

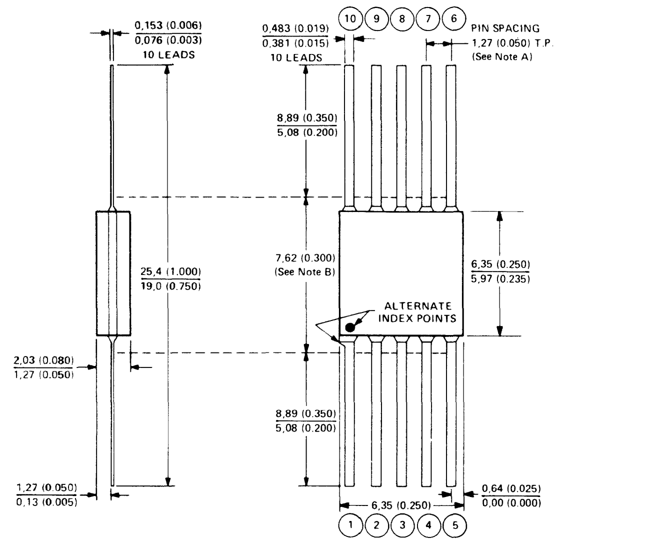
A

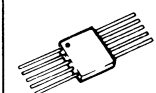
TEXAS INSTRUMENTS

U ceramic flat packages

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

10-PIN U CERAMIC





Falls Within JEDEC MO-004AE Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

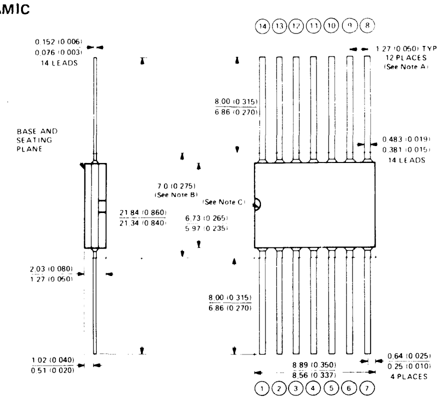
NOTES: A. Leads are within 0.005 radius of true position (TP) at maximum material condition.

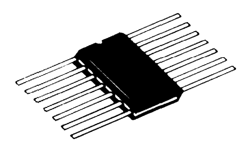
B. This dimension determines a zone within which all body and lead irregularities lie.

W ceramic flat packages

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC



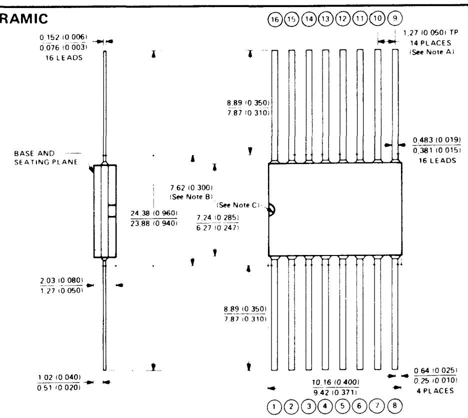


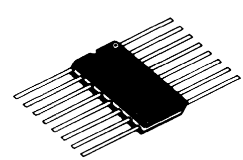
Falls Within JEDEC MO-004AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOT TO SCALE

16-PIN W CERAMIC





Falls Within JEDEC MO-004AG Dimensions

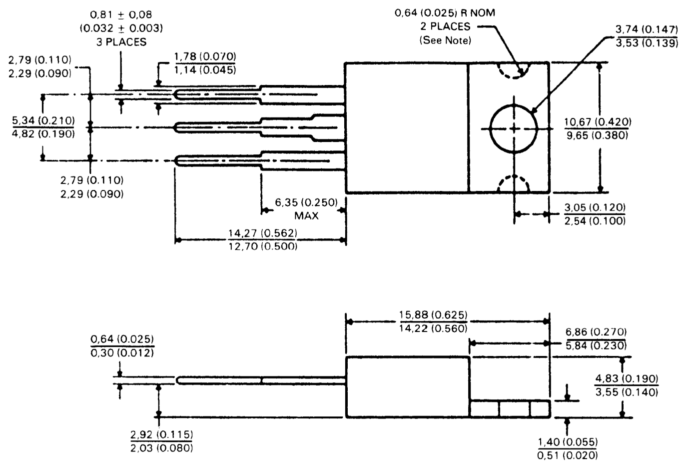
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

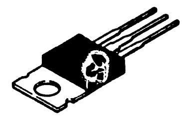
NOT TO SCALE

NOTES: A. Leads are within 0,13 (0.005) radius of true position (TP) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

KC (TO-220AB) package

THE CENTER TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB





Falls Within JEDEC TO-220AB Dimensions
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

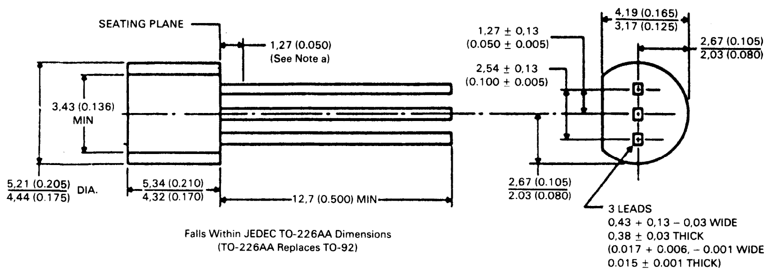
NOTE: Notches may or may not be present.

Appendix

A

LP plastic package

This package is an encapsulation in a plastic compound specifically designed for this purpose. The package will withstand soldering temperatures without deformation. The package exhibits stable characteristics under high-humidity conditions and is capable of meeting MIL-STD-202C, Method 106B.



Falls Within JEDEC TO-226AA Dimensions
(TO-226AA Replaces TO-92)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: a: Lead dimensions are not controlled in this area.

NOTES

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